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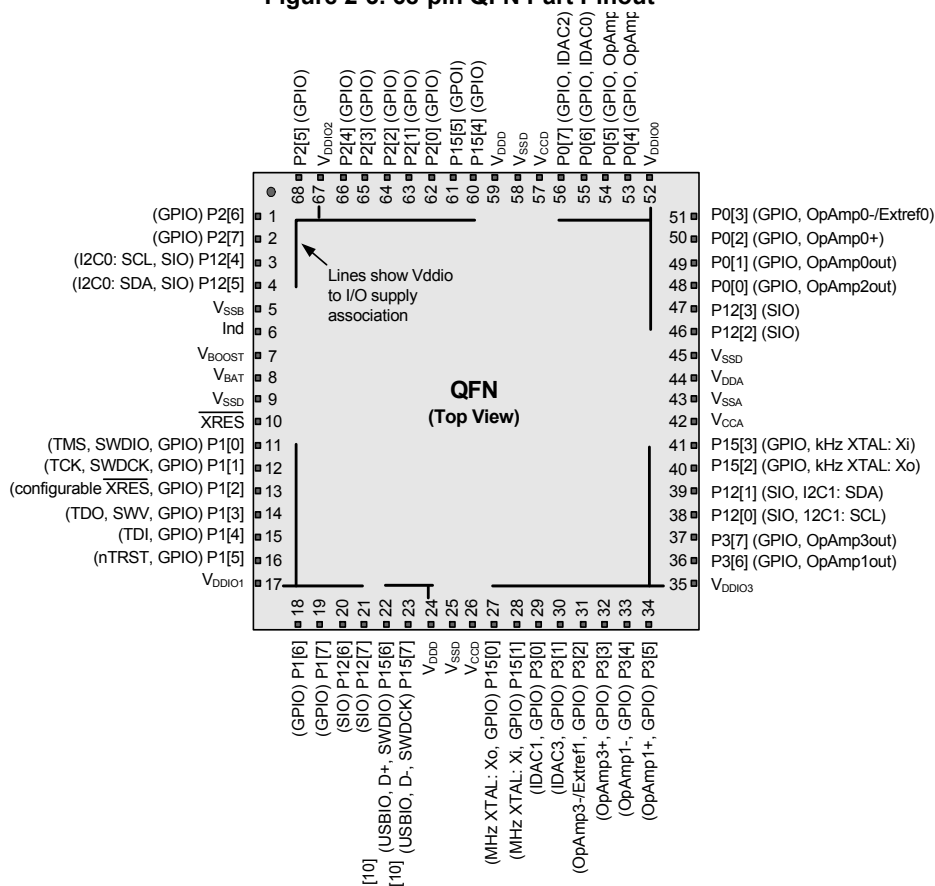
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, POR, PWM, WDT
Number of I/O	62
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x20b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3866axi-055

Figure 2-3. 68-pin QFN Part Pinout^[9]



Notes

9. The center pad on the QFN package should be connected to digital ground (V_{SSD}) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

10. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.

5.6.3.1 xdata Space

The 8051 xdata space is 24-bit, or 16 MB in size. The majority of this space is not 'external'—it is used by on-chip components. See [Table 5-3](#). External, that is, off-chip, memory can be accessed using the EMIF. See [External Memory Interface](#) on page 18.

Table 5-3. XDATA Data Address Map

Address Range	Purpose
0x00 0000 – 0x00 1FFF	SRAM
0x00 4000 – 0x00 42FF	Clocking, PLLs, and oscillators
0x00 4300 – 0x00 43FF	Power management
0x00 4400 – 0x00 44FF	Interrupt controller
0x00 4500 – 0x00 45FF	Ports interrupt control
0x00 4700 – 0x00 47FF	Flash programming interface
0x00 4900 – 0x00 49FF	I ² C controller
0x00 4E00 – 0x00 4EFF	Decimator
0x00 4F00 – 0x00 4FFF	Fixed timer/counter/PWMs
0x00 5000 – 0x00 51FF	I/O ports control
0x00 5400 – 0x00 54FF	EMIF control registers
0x00 5800 – 0x00 5FFF	Analog subsystem interface
0x00 6000 – 0x00 60FF	USB controller
0x00 6400 – 0x00 6FFF	UDB configuration
0x00 7000 – 0x00 7FFF	PHUB configuration
0x00 8000 – 0x00 8FFF	EEPROM
0x00 A000 – 0x00 A400	CAN
0x00 C000 – 0x00 C800	DFB
0x01 0000 – 0x01 FFFF	Digital Interconnect configuration
0x05 0220 – 0x05 02F0	Debug controller
0x08 0000 – 0x08 1FFF	Flash ECC bytes
0x80 0000 – 0xFF FFFF	External memory interface

6. System Integration

6.1 Clocking System

The clocking system generates, divides, and distributes clocks throughout the PSoC system. For the majority of systems, no external crystal is required. The IMO and PLL together can generate up to a 66 MHz clock, accurate to ± 1 percent over voltage and temperature. Additional internal and external clock sources allow each design to optimize accuracy, power, and cost. All of the system clock sources can be used to generate other clock frequencies in the 16-bit clock dividers and UDBs for anything the user wants, for example a UART baud rate generator.

Clock generation and distribution is automatically configured through the PSoC Creator IDE graphical interface. This is based on the complete system's requirements. It greatly speeds the design process. PSoC Creator allows you to build clocking systems with minimal input. You can specify desired clock frequencies and accuracies, and the software locates or builds a clock that meets the required specifications. This is possible because of the programmability inherent PSoC.

Key features of the clocking system include:

- Seven general purpose clock sources
 - 3- to 62-MHz IMO, $\pm 1\%$ at 3 MHz
 - 4- to 33-MHz external crystal oscillator (MHzECO)
 - Clock doubler provides a doubled clock frequency output for the USB block, see [USB Clock Domain](#) on page 23.
 - DSI signal from an external I/O pin or other logic
 - 24- to 67-MHz fractional PLL sourced from IMO, MHzECO, or DSI
 - Clock doubler
 - 1-kHz, 33-kHz, 100-kHz ILO for WDT and sleep timer
 - 32.768-kHz external crystal oscillator (kHzECO) for RTC
- IMO has a USB mode that auto locks to the USB bus clock requiring no external crystal for USB. (USB equipped parts only)
- Independently sourced clock in all clock dividers
- Eight 16-bit clock dividers for the digital system
- Four 16-bit clock dividers for the analog system
- Dedicated 16-bit divider for the bus clock
- Dedicated 4-bit divider for the CPU clock
- Automatic clock configuration in PSoC Creator

Table 6-1. Oscillator Summary

Source	Fmin	Tolerance at Fmin	Fmax	Tolerance at Fmax	Startup Time
IMO	3 MHz	$\pm 1\%$ over voltage and temperature	62 MHz	$\pm 7\%$	10 μ s max
MHzECO	4 MHz	Crystal dependent	33 MHz	Crystal dependent	5 ms typ, max is crystal dependent
DSI	0 MHz	Input dependent	66 MHz	Input dependent	Input dependent
PLL	24 MHz	Input dependent	67 MHz	Input dependent	250 μ s max
Doubler	12 MHz	Input dependent	48 MHz	Input dependent	1 μ s max
ILO	1 kHz	-50% , $+100\%$	100 kHz	-55% , $+100\%$	15 ms max in lowest power mode
kHzECO	32 kHz	Crystal dependent	32 kHz	Crystal dependent	500 ms typ, max is crystal dependent

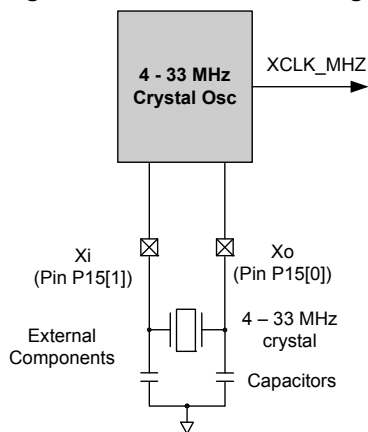
The 33-kHz clock (CLK33K) comes from a divide-by-3 operation on CLK100K. This output can be used as a reduced accuracy version of the 32.768-kHz ECO clock with no need for a crystal.

6.1.2 External Oscillators

6.1.2.1 MHz External Crystal Oscillator

The MHzECO provides high frequency, high precision clocking using an external crystal (see Figure 6-2). It supports a wide variety of crystal types, in the range of 4 to 33 MHz. When used in conjunction with the PLL, it can generate CPU and system clocks up to the device's maximum frequency (see PLL). The GPIO pins connecting to the external crystal and capacitors are fixed. MHzECO accuracy depends on the crystal chosen.

Figure 6-2. MHzECO Block Diagram

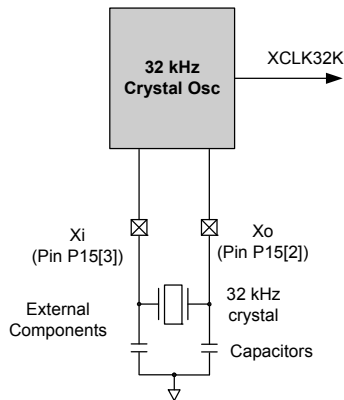


6.1.2.2 32.768-kHz ECO

The 32.768-kHz external crystal oscillator (32kHzECO) provides precision timing with minimal power consumption using an external 32.768-kHz watch crystal (see Figure 6-3). The 32kHzECO also connects directly to the sleep timer and provides the source for the RTC. The RTC uses a 1-second interrupt to implement the RTC functionality in firmware.

The oscillator works in two distinct power modes. This allows users to trade off power consumption with noise immunity from neighboring circuits. The GPIO pins connected to the external crystal and capacitors are fixed.

Figure 6-3. 32kHzECO Block Diagram



6.1.2.3 Digital System Interconnect

The DSI provides routing for clocks taken from external clock oscillators connected to I/O. The oscillators can also be generated within the device in the digital system and UDBs.

While the primary DSI clock input provides access to all clocking resources, up to eight other DSI clocks (internally or externally generated) may be routed directly to the eight digital clock dividers. This is only possible if there are multiple precision clock sources.

6.1.3 Clock Distribution

All seven clock sources are inputs to the central clock distribution system. The distribution system is designed to create multiple high precision clocks. These clocks are customized for the design's requirements and eliminate the common problems found with limited resolution prescalers attached to peripherals. The clock distribution system generates several types of clock trees.

- The system clock is used to select and supply the fastest clock in the system for general system clock requirements and clock synchronization of the PSoC device.
- Bus clock 16-bit divider uses the system clock to generate the system's bus clock used for data transfers. Bus clock is the source clock for the CPU clock divider.
- Eight fully programmable 16-bit clock dividers generate digital system clocks for general use in the digital system, as configured by the design's requirements. Digital system clocks can generate custom clocks derived from any of the seven clock sources for any purpose. Examples include baud rate generators, accurate PWM periods, and timer clocks, and many others. If more than eight digital clock dividers are required, the UDBs and fixed function timer/counter/PWMs can also generate clocks.
- Four 16-bit clock dividers generate clocks for the analog system components that require clocking, such as ADC and mixers. The analog clock dividers include skew control to ensure that critical analog events do not occur simultaneously with digital switching events. This is done to reduce analog system noise.

Each clock divider consists of an 8-input multiplexer, a 16-bit clock divider (divide by 2 and higher) that generates ~50 percent duty cycle clocks, system clock resynchronization logic, and deglitch logic. The outputs from each digital clock tree can be routed into the digital system interconnect and then brought back into the clock system as an input, allowing clock chaining of up to 32 bits.

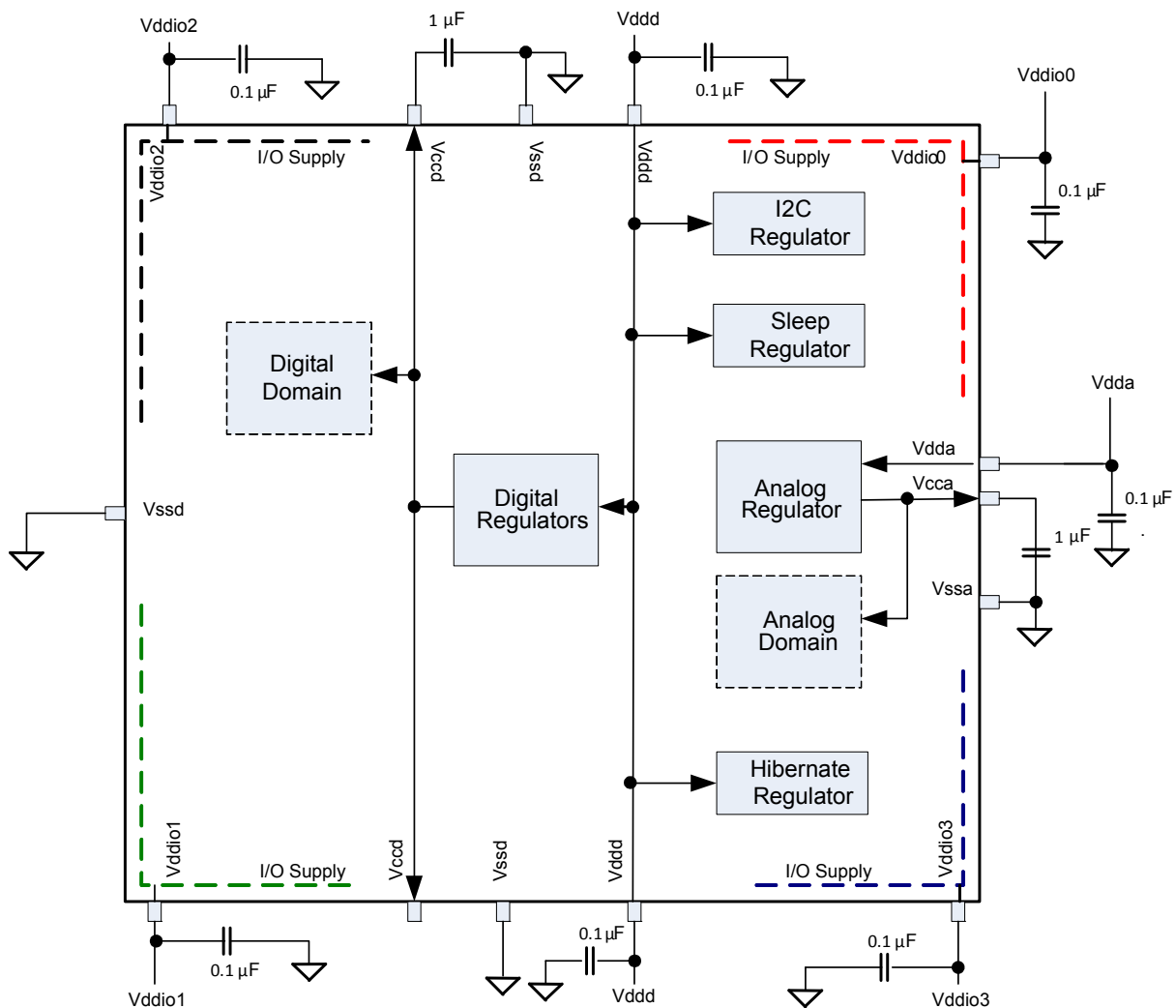
6.1.4 USB Clock Domain

The USB clock domain is unique in that it operates largely asynchronously from the main clock network. The USB logic contains a synchronous bus interface to the chip, while running on an asynchronous clock to process USB data. The USB logic requires a 48 MHz frequency. This frequency can be generated from different sources, including DSI clock at 48 MHz or doubled value of 24 MHz from internal oscillator, DSI signal, or crystal oscillator.

6.2 Power System

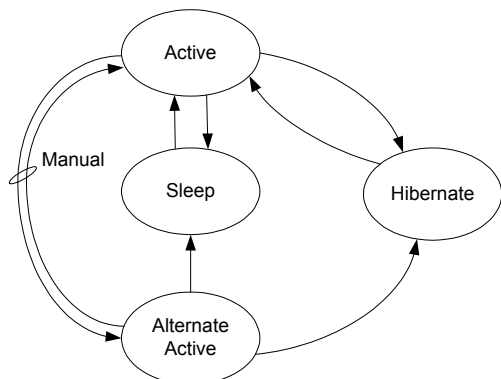
The power system consists of separate analog, digital, and I/O supply pins, labeled Vdda, Vddd, and Vddiox, respectively. It also includes two internal 1.8-V regulators that provide the digital (Vccd) and analog (Vcca) supplies for the internal core logic. The output pins of the regulators (Vccd and Vcca) and the Vddio pins must have capacitors connected as shown in [Figure 6-4](#). The two Vccd pins must be shorted together, with as short a trace as possible, and connected to a 1- μ F \pm 10-percent X5R capacitor. The power system also contains a sleep regulator, an I²C regulator, and a hibernate regulator.

Figure 6-4. PSoC Power System



Note The two Vccd pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in [Figure 2-6](#) on page 10.

Figure 6-5. Power Mode Transitions



6.2.1.1 Active Mode

Active mode is the primary operating mode of the device. When in active mode, the active configuration template bits control which available resources are enabled or disabled. When a resource is disabled, the digital clocks are gated, analog bias currents are disabled, and leakage currents are reduced as appropriate. User firmware can dynamically control subsystem power by setting and clearing bits in the active configuration template. The CPU can disable itself, in which case the CPU is automatically reenabled at the next wakeup event.

When a wakeup event occurs, the global mode is always returned to active, and the CPU is automatically enabled, regardless of its template settings. Active mode is the default global power mode upon boot.

6.2.1.2 Alternate Active Mode

Alternate Active mode is very similar to Active mode. In alternate active mode, fewer subsystems are enabled, to reduce power consumption. One possible configuration is to turn off the CPU and flash, and run peripherals at full speed.

6.2.1.3 Sleep Mode

Sleep mode reduces power consumption when a resume time of 15 μ s is acceptable. The wake time is used to ensure that the regulator outputs are stable enough to directly enter active mode.

6.2.1.4 Hibernate Mode

In hibernate mode nearly all of the internal functions are disabled. Internal voltages are reduced to the minimal level to keep vital systems alive. Configuration state is preserved in hibernate mode and SRAM memory is retained. GPIOs configured as digital outputs maintain their previous values and external GPIO pin interrupt settings are preserved. The device can only return from hibernate mode in response to an external I/O interrupt. The resume time from hibernate mode is less than 100 μ s.

6.2.1.5 Wakeup Events

Wakeup events are configurable and can come from an interrupt or device reset. A wakeup event restores the system to active mode. Firmware enabled interrupt sources include internally generated interrupts, power supervisor, central timewheel, and I/O interrupts. Internal interrupt sources can come from a variety of peripherals, such as analog comparators and UDBs. The

central timewheel provides periodic interrupts to allow the system to wake up, poll peripherals, or perform real-time functions. Reset event sources include the external reset I/O pin (XRES), WDT, and precision reset (PRES).

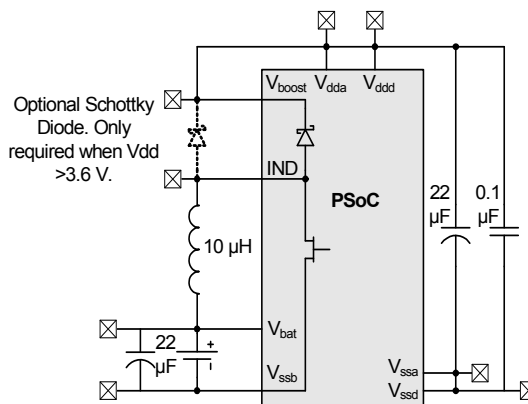
6.2.2 Boost Converter

Applications that use a supply voltage of less than 1.71 V, such as solar or single cell battery supplies, may use the on-chip boost converter. The boost converter may also be used in any system that requires a higher operating voltage than the supply provides. For instance, this includes driving 5.0 V LCD glass in a 3.3 V system. The boost converter accepts an input voltage as low as 0.5 V. With one low cost inductor it produces a selectable output voltage sourcing enough current to operate the PSoC and other on-board components.

The boost converter accepts an input voltage from 0.5 V to 5.5 V (V_{BAT}), and can start up with V_{bat} as low as 0.5 V. The converter provides a user configurable output voltage of 1.8 to 5.0 V (V_{boost}). V_{bat} is typically less than V_{boost} ; if V_{bat} is greater than or equal to V_{boost} , then V_{boost} will be the same as V_{bat} . The block can deliver up to 50 mA (I_{BOOST}) depending on configuration.

Four pins are associated with the boost converter: V_{bat} , V_{ssb} , V_{boost} , and IND . The boosted output voltage is sensed at the V_{boost} pin and must be connected directly to the chip's supply inputs. An inductor is connected between the V_{bat} and IND pins. You can optimize the inductor value to increase the boost converter efficiency based on input voltage, output voltage, current and switching frequency. The External Schottky diode shown in Figure 6-6 is required only in cases when $V_{boost} > 3.6$ V.

Figure 6-6. Application for Boost Converter



The switching frequency can be set to 100 kHz, 400 kHz, 2 MHz, or 32 kHz to optimize efficiency and component cost. The 100 kHz, 400 kHz, and 2 MHz switching frequencies are generated using oscillators internal to the boost converter block. When the 32-kHz switching frequency is selected, the clock is derived from a 32 kHz external crystal oscillator. The 32-kHz external clock is primarily intended for boost standby mode.

At 2 MHz the V_{boost} output is limited to $2 \times V_{bat}$, and at 400 kHz V_{boost} is limited to $4 \times V_{bat}$.

The boost converter can be operated in two different modes: active and standby. Active mode is the normal mode of operation where the boost regulator actively generates a regulated output

voltage. In standby mode, most boost functions are disabled, thus reducing power consumption of the boost circuit. The converter can be configured to provide low-power, low-current regulation in the standby mode. The external 32-kHz crystal can be used to generate inductor boost pulses on the rising and falling edge of the clock when the output voltage is less than the programmed value. This is called automatic thump mode (ATM).

The boost typically draws 200 μ A in active mode and 12 μ A in standby mode. The boost operating modes must be used in conjunction with chip power modes to minimize the total chip power consumption. Table 6-4 lists the boost power modes available in different chip power modes.

Table 6-4. Chip and Boost Power Modes Compatibility

Chip Power Modes	Boost Power Modes
Chip – Active mode	Boost can be operated in either active or standby mode.
Chip – Sleep mode	Boost can be operated in either active or standby mode. However, it is recommended to operate boost in standby mode for low-power consumption
Chip – Hibernate mode	Boost can only be operated in active mode. However, it is recommended not to use boost in chip hibernate mode due to high current consumption in boost active mode

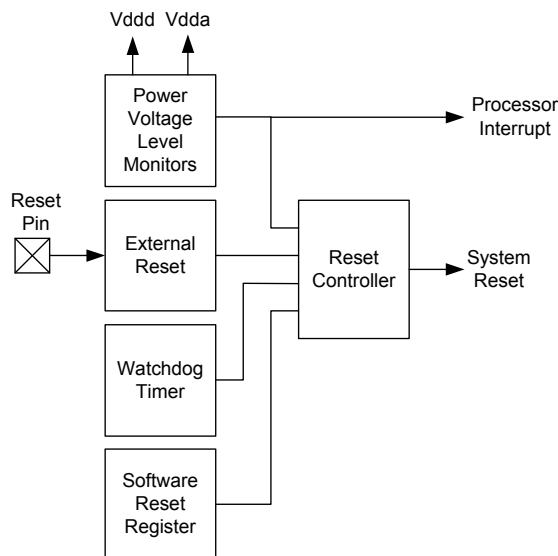
If the boost converter is not used in a given application, tie the Vbat, Vssb, and Vboost pins to ground and leave the Ind pin unconnected.

6.3 Reset

CY8C38 has multiple internal and external reset sources available. The reset sources are:

- **Power source monitoring** – The analog and digital power voltages, Vdda, Vddd, Vcca, and Vccd are monitored in several different modes during power up, active mode, and sleep mode (buzzing). If any of the voltages goes outside predetermined ranges then a reset is generated. The monitors are programmable to generate an interrupt to the processor under certain conditions before reaching the reset thresholds.
- **External** – The device can be reset from an external source by pulling the reset pin (XRES) low. The XRES pin includes an internal pull-up to Vddio1. Vddd, Vdda, and Vddio1 must all have voltage applied before the part comes out of reset.
- **Watchdog timer** – A watchdog timer monitors the execution of instructions by the processor. If the watchdog timer is not reset by firmware within a certain period of time, the watchdog timer generates a reset.
- **Software** – The device can be reset under program control.

Figure 6-7. Resets



The term **device reset** indicates that the processor as well as analog and digital peripherals and registers are reset.

A reset status register holds the source of the most recent reset or power voltage monitoring interrupt. The program may examine this register to detect and report exception conditions. This register is cleared after a power-on reset.

6.3.1 Reset Sources

6.3.1.1 Power Voltage Level Monitors

■ IPOR – Initial power-on reset

At initial power on, IPOR monitors the power voltages V_{DDP} and V_{DDA}, both directly at the pins and at the outputs of the corresponding internal regulators. The trip level is not precise. It is set to approximately 1 volt, which is below the lowest specified operating voltage but high enough for the internal circuits to be reset and to hold their reset state. The monitor generates a reset pulse that is at least 100 ns wide. It may be much wider if one or more of the voltages ramps up slowly.

To save power the IPOR circuit is disabled when the internal digital supply is stable. Voltage supervision is then handed off to the precise low voltage reset (PRES) circuit. When the voltage is high enough for PRES to release, the IMO starts.

■ PRES – Precise low voltage reset

This circuit monitors the outputs of the analog and digital internal regulators after power up. The regulator outputs are compared to a precise reference voltage. The response to a PRES trip is identical to an IPOR reset.

In normal operating mode, the program cannot disable the digital PRES circuit. The analog regulator can be disabled, which also disables the analog portion of the PRES. The PRES circuit is disabled automatically during sleep and hibernate modes, with one exception: During sleep mode the regulators are periodically activated (buzzed) to provide supervisory services and to reduce wakeup time. At these times the PRES circuit is also buzzed to allow periodic voltage monitoring.

7.1 Example Peripherals

The flexibility of the CY8C38 family's UDBs and analog blocks allow the user to create a wide range of components (peripherals). The most common peripherals were built and characterized by Cypress and are shown in the PSoC Creator component catalog, however, users may also create their own custom components using PSoC Creator. Using PSoC Creator, users may also create their own components for reuse within their organization, for example sensor interfaces, proprietary algorithms, and display interfaces.

The number of components available through PSoC Creator is too numerous to list in the datasheet, and the list is always growing. An example of a component available for use in CY8C38 family, but, not explicitly called out in this datasheet is the UART component.

7.1.1 Example Digital Components

The following is a sample of the digital components available in PSoC Creator for the CY8C38 family. The exact amount of hardware resources (UDBs, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- Communications
 - I²C
 - UART
 - SPI
- Functions
 - EMIF
 - PWMs
 - Timers
 - Counters
- Logic
 - NOT
 - OR
 - XOR
 - AND

7.1.2 Example Analog Components

The following is a sample of the analog components available in PSoC Creator for the CY8C38 family. The exact amount of hardware resources (SC/CT blocks, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- Amplifiers
 - TIA
 - PGA
 - opamp
- ADC
 - Delta-sigma
- DACs
 - Current

- Voltage
- PWM
- Comparators
- Mixers

7.1.3 Example System Function Components

The following is a sample of the system function components available in PSoC Creator for the CY8C38 family. The exact amount of hardware resources (UDBs, DFB taps, SC/CT blocks, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- CapSense
- LCD drive
- LCD control
- Filters

7.1.4 Designing with PSoC Creator

7.1.4.1 More Than a Typical IDE

A successful design tool allows for the rapid development and deployment of both simple and complex designs. It reduces or eliminates any learning curve. It makes the integration of a new design into the production stream straightforward.

PSoC Creator is that design tool.

PSoC Creator is a full featured Integrated Development Environment (IDE) for hardware and software design. It is optimized specifically for PSoC devices and combines a modern, powerful software development platform with a sophisticated graphical design tool. This unique combination of tools makes PSoC Creator the most flexible embedded design platform available.

Graphical design entry simplifies the task of configuring a particular part. You can select the required functionality from an extensive catalog of components and place it in your design. All components are parameterized and have an editor dialog that allows you to tailor functionality to your needs.

PSoC Creator automatically configures clocks and routes the I/O to the selected pins and then generates APIs to give the application complete control over the hardware. Changing the PSoC device configuration is as simple as adding a new component, setting its parameters, and rebuilding the project.

At any stage of development you are free to change the hardware configuration and even the target processor. To retarget your application (hardware and software) to new devices, even from 8- to 32-bit families, just select the new device and rebuild.

You also have the ability to change the C compiler and evaluate an alternative. Components are designed for portability and are validated against all devices, from all families, and against all supported tool chains. Switching compilers is as easy as editing the from the project options and rebuilding the application with no errors from the generated APIs or boot code.

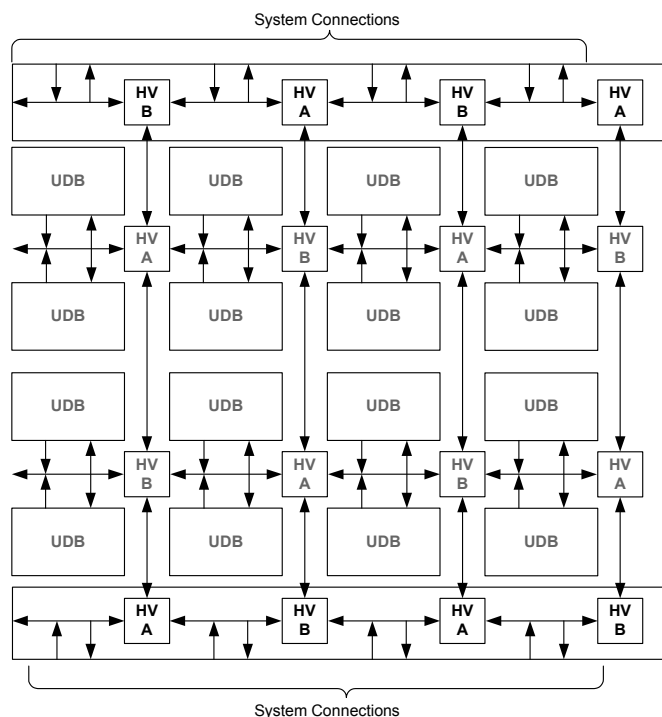
7.2.3.2 Clock Generation

Each subcomponent block of a UDB including the two PLDs, the datapath, and Status and Control, has a clock selection and control block. This promotes a fine granularity with respect to allocating clocking resources to UDB component blocks and allows unused UDB resources to be used by other functions for maximum system efficiency.

7.3 UDB Array Description

Figure 7-11 shows an example of a 16 UDB array. In addition to the array core, there are DSI routing interfaces at the top and bottom of the array. Other interfaces that are not explicitly shown include the system interfaces for bus and clock distribution. The UDB array includes multiple horizontal and vertical routing channels each comprised of 96 wires. The wire connections to UDBs, at horizontal/vertical intersection and at the DSI interface are highly permutable providing efficient automatic routing in PSoC Creator. Additionally the routing allows wire by wire segmentation along the vertical and horizontal routing to further increase routing flexibility and capability.

Figure 7-11. Digital System Interface Structure

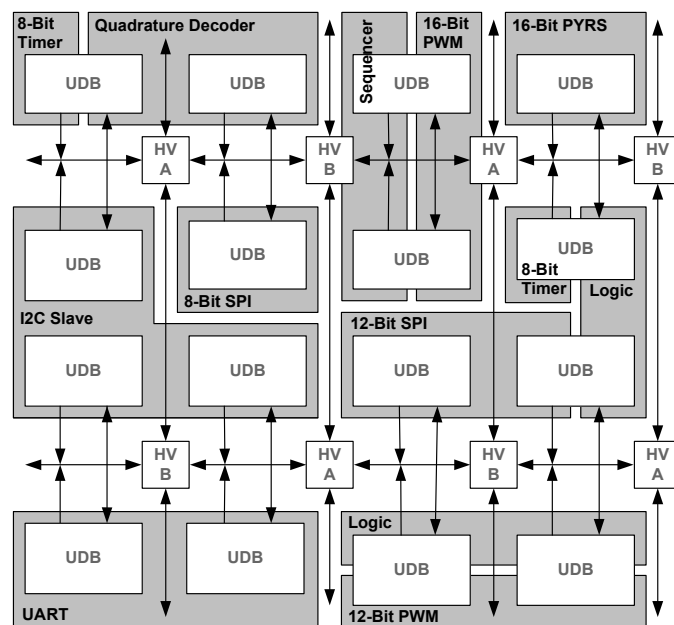


7.3.1 UDB Array Programmable Resources

Figure 7-12 shows an example of how functions are mapped into a bank of 16 UDBs. The primary programmable resources of the UDB are two PLDs, one datapath and one status/control register. These resources are allocated independently, because they have independently selectable clocks, and therefore unused blocks are allocated to other unrelated functions.

An example of this is the 8-bit timer in the upper left corner of the array. This function only requires one datapath in the UDB, and therefore the PLD resources may be allocated to another function. A function such as a Quadrature Decoder may require more PLD logic than one UDB can supply and in this case can utilize the unused PLD blocks in the 8-bit Timer UDB. Programmable resources in the UDB array are generally homogeneous so functions can be mapped to arbitrary boundaries in the array.

Figure 7-12. Function Mapping Example in a Bank of UDBs



7.4 DSI Routing Interface Description

The DSI routing interface is a continuation of the horizontal and vertical routing channels at the top and bottom of the UDB array core. It provides general purpose programmable routing between device peripherals, including UDBs, I/Os, analog peripherals, interrupts, DMA and fixed function peripherals.

Figure 7-13 illustrates the concept of the digital system interconnect, which connects the UDB array routing matrix with other device peripherals. Any digital core or fixed function peripheral that needs programmable routing is connected to this interface.

Signals in this category include:

- Interrupt requests from all digital peripherals in the system.
- DMA requests from all digital peripherals in the system.
- Digital peripheral data signals that need flexible routing to I/Os.
- Digital peripheral data signals that need connections to UDBs.
- Connections to the interrupt and DMA controllers.
- Connection to I/O pins.
- Connection to analog system digital signals.

7.7 Timers, Counters, and PWMs

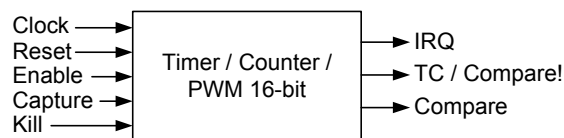
The timer/counter/PWM peripheral is a 16-bit dedicated peripheral providing three of the most common embedded peripheral features. As almost all embedded systems use some combination of timers, counters, and PWMs. Four of them have been included on this PSoC device family. Additional and more advanced functionality timers, counters, and PWMs can also be instantiated in UDBs as required. PSoC Creator allows you to choose the timer, counter, and PWM features that they require. The tool set utilizes the most optimal resources available.

The timer/counter/PWM peripheral can select from multiple clock sources, with input and output signals connected through the DSI routing. DSI routing allows input and output connections to any device pin and any internal digital signal accessible through the DSI. Each of the four instances has a compare output, terminal count output (optional complementary compare output), and programmable interrupt request line. The Timer/Counter/PWMs are configurable as free running, one shot, or Enable input controlled. The peripheral has timer reset and capture inputs, and a kill input for control of the comparator outputs. The peripheral supports full 16-bit capture.

Timer/Counter/PWM features include:

- 16-bit Timer/Counter/PWM (down count only)
- Selectable clock source
- PWM comparator (configurable for LT, LTE, EQ, GTE, GT)
- Period reload on start, reset, and terminal count
- Interrupt on terminal count, compare true, or capture
- Dynamic counter reads
- Timer capture mode
- Count while enable signal is asserted mode
- Free run mode
- One Shot mode (stop at end of period)
- Complementary PWM outputs with deadband
- PWM output kill

Figure 7-21. Timer/Counter/PWM



7.8 I²C

The I²C peripheral provides a synchronous two wire interface designed to interface the PSoC device with a two wire I²C serial communication bus. The bus is compliant with Philips 'The I²C Specification' version 2.1. Additional I²C interfaces can be instantiated using Universal Digital Blocks (UDBs) in PSoC Creator, as required.

To eliminate the need for excessive CPU intervention and overhead, I²C specific support is provided for status detection and generation of framing bits. I²C operates as a slave, a master, or multimaster (Slave and Master). In slave mode, the unit always listens for a start condition to begin sending or receiving data. Master mode supplies the ability to generate the Start and Stop conditions and initiate transactions. Multimaster mode provides clock synchronization and arbitration to allow multiple masters on the same bus. If Master mode is enabled and Slave mode is not enabled, the block does not generate interrupts on externally generated Start conditions. I²C interfaces through the DSI routing and allows direct connections to any GPIO or SIO pins.

I²C provides hardware address detect of a 7-bit address without CPU intervention. Additionally the device can wake from low-power modes on a 7-bit hardware address match. If wakeup functionality is required, I²C pin connections are limited to the two special sets of SIO pins.

I²C features include:

- Slave and master, transmitter, and receiver operation
- Byte processing for low CPU overhead
- Interrupt or polling CPU interface
- Support for bus speeds up to 1 Mbps (3.4 Mbps in UDBs)
- 7 or 10-bit addressing (10-bit addressing requires firmware support)
- SMBus operation (through firmware support - SMBus supported in hardware in UDBs)
- 7-bit hardware address compare
- Wake from low-power modes on address match

7.9 Digital Filter Block

Some devices in the CY8C38 family of devices have a dedicated HW accelerator block used for digital filtering. The DFB has a dedicated multiplier and accumulator that calculates a 24-bit by 24-bit multiply accumulate in one system clock cycle. This enables the mapping of a direct form FIR filter that approaches a computation rate of one FIR tap for each clock cycle. The MCU can implement any of the functions performed by this block, but at a slower rate that consumes MCU bandwidth.

The PSoC Creator interface provides a wizard to implement FIR and IIR digital filters with coefficients for LPF, BPF, HPF, Notch and arbitrary shape filters. 64 pairs of data and coefficients are stored. This enables a 64 tap FIR filter or up to 4 16 tap filters of either FIR or IIR formulation.

Pin Connection Diagram for STM32F769I-DT

Legend:

- Switch Resistance:
 - Small (~870 Ohms) - ○
 - Large (~200 Ohms) - ●

Notes:

- * Denotes pins on all packages
- LCD signals are not shown.

Rev #51

8.11.1 Down Mixer

The SC/CT block can be used as a mixer to down convert an input signal. This circuit is a high bandwidth passive sample network that can sample input signals up to 14 MHz. This sampled value is then held using the opamp with a maximum clock rate of 4 MHz. The output frequency is at the difference between the input frequency and the highest integer multiple of the Local Oscillator that is less than the input.

8.11.2 First Order Modulator – SC Mode

A first order modulator is constructed by placing the SC/CT block in an integrator mode and using a comparator to provide a 1-bit feedback to the input. Depending on this bit, a reference voltage is either subtracted or added to the input signal. The block output is the output of the comparator and not the integrator in the modulator case. The signal is downshifted and buffered and then processed by a decimator to make a delta-sigma converter or a counter to make an incremental converter. The accuracy of the sampled data from the first-order modulator is determined from several factors.

The main application for this modulator is for a low-frequency ADC with high accuracy. Applications include strain gauges, thermocouples, precision voltage, and current measurement.

9. Programming, Debug Interfaces, Resources

PSoC devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware. Three interfaces are available: JTAG, SWD, and SWV. JTAG and SWD support all programming and debug features of the device. JTAG also supports standard JTAG scan chains for board level test and chaining multiple JTAG devices to a single JTAG connection.

Complete Debug on Chip (DoC) functionality enables full device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE software provides fully integrated programming and debug support for PSoC devices. The low cost MiniProg3 programmer and debugger is designed to provide full programming and debug support of PSoC devices in conjunction with the PSoC Creator IDE. PSoC JTAG, SWD, and SWV interfaces are fully compatible with industry standard third party tools.

All DOC circuits are disabled by default and can only be enabled in firmware. If not enabled, the only way to reenale them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables DOC. Disabling DOC features, robust flash protection, and hiding custom analog and digital functionality inside the PSoC device provide a level of security not possible with multichip application solutions. Additionally, all device interfaces can be permanently disabled (Device Security) for applications concerned about phishing

attacks due to a maliciously reprogrammed device. Permanently disabling interfaces is not recommended in most applications because you cannot access the device later. Because all programming, debug, and test interfaces are disabled when device security is enabled, PSoCs with Device Security enabled may not be returned for failure analysis.

Table 9-1. Debug Configurations

Debug and Trace Configuration	GPIO Pins Used
All debug and trace disabled	0
JTAG	4 or 5
SWD	2
SWV	1
SWD + SWV	3

9.1 JTAG Interface

The IEEE 1149.1 compliant JTAG interface exists on four or five pins (the nTRST pin is optional). The JTAG clock frequency can be up to 8 MHz, or 1/3 of the CPU clock frequency for 8 and 16-bit transfers, or 1/5 of the CPU clock frequency for 32-bit transfers, whichever is least. By default, the JTAG pins are enabled on new devices but the JTAG interface can be disabled, allowing these pins to be used as General Purpose I/O (GPIO) instead. The JTAG interface is used for programming the flash memory, debugging, I/O scan chains, and JTAG device chaining.

9.2 Serial Wire Debug Interface

The SWD interface is the preferred alternative to the JTAG interface. It requires only two pins instead of the four or five needed by JTAG. SWD provides all of the programming and debugging features of JTAG at the same speed. SWD does not provide access to scan chains or device chaining. The SWD clock frequency can be up to 1/3 of the CPU clock frequency.

SWD uses two pins, either two of the JTAG pins (TMS and TCK) or the USBIO D+ and D– pins. The USBIO pins are useful for in system programming of USB solutions that would otherwise require a separate programming connector. One pin is used for the data clock and the other is used for data input and output. SWD can be enabled on only one of the pin pairs at a time. This only happens if, within 8 μ s (key window) after reset, that pin pair (JTAG or USB) receives a predetermined sequence of 1s and 0s. SWD is used for debugging or for programming the flash memory.

The SWD interface can be enabled from the JTAG interface or disabled, allowing its pins to be used as GPIO. Unlike JTAG, the SWD interface can always be reacquired on any device during the key window. It can then be used to reenale the JTAG interface, if desired. When using SWD or JTAG pins as standard GPIO, make sure that the GPIO functionality and PCB circuits do not interfere with SWD or JTAG use.

11. Electrical Specifications

Specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted. The unique flexibility of the PSoC UDBs and analog blocks enable many functions to be implemented in PSoC Creator components, see the component datasheets for full AC/DC specifications of individual functions. See the [“Example Peripherals”](#) section on page 35 for further explanation of PSoC Creator components.

11.1 Absolute Maximum Ratings

Table 11-1. Absolute Maximum Ratings DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{STG}	Storage temperature	Higher storage temperatures reduce NVL data retention time. Recommended storage temperature is $+25\text{ }^{\circ}\text{C} \pm 25\text{ }^{\circ}\text{C}$. Extended duration storage temperatures above $85\text{ }^{\circ}\text{C}$ degrade reliability.	-55	25	100	$^{\circ}\text{C}$
V_{DDA}	Analog supply voltage relative to V_{SSA}		-0.5	–	6	V
V_{DDD}	Digital supply voltage relative to V_{SSD}		-0.5	–	6	V
V_{DDIO}	I/O supply voltage relative to V_{SSD}		-0.5	–	6	V
V_{CCA}	Direct analog core voltage input		-0.5	–	1.95	V
V_{CCD}	Direct digital core voltage input		-0.5	–	1.95	V
V_{SSA}	Analog ground voltage		$V_{SSD} - 0.5$	–	$V_{SSD} + 0.5$	V
$V_{GPIO}^{[17]}$	DC input voltage on GPIO	Includes signals sourced by V_{DDA} and routed internal to the pin	$V_{SSD} - 0.5$	–	$V_{DDIO} + 0.5$	V
V_{SIO}	DC input voltage on SIO	Output disabled	$V_{SSD} - 0.5$	–	7	V
		Output enabled	$V_{SSD} - 0.5$	–	6	V
V_{IND}	Voltage at boost converter input		0.5	–	5.5	V
V_{BAT}	Boost converter supply		$V_{SSD} - 0.5$	–	5.5	V
I_{VDDIO}	Current per V_{DDIO} supply pin		–	–	100	mA
V_{extref}	ADC external reference inputs	Pins P0[3], P3[2]	–	–	2	V
I_{LU}	Latch up current ^[18]		-140	–	140	mA
ESD_{HBM}	Electrostatic discharge voltage	Human body model	750	–	–	V
ESD_{CDM}	Electrostatic discharge voltage	Charge device model	500	–	–	V

Note Usage above the absolute maximum conditions listed in [Table 11-1](#) may cause permanent damage to the device. Exposure to maximum conditions for extended periods of time may affect device reliability. When used below maximum conditions but above normal operating conditions the device may not operate to specification.

Notes

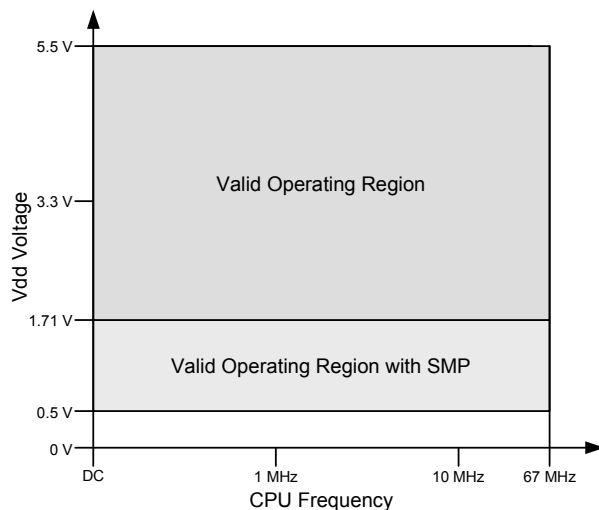
17. The V_{DDIO} supply voltage must be greater than the maximum analog voltage on the associated GPIO pins. Maximum analog voltage on GPIO pin $\leq V_{DDIO} \leq V_{DDA}$.

18. Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch-up Test.

Table 11-3. AC Specifications^[24]

Parameter	Description	Conditions	Min	Typ	Max	Units
F _{CPU}	CPU frequency	$1.71\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	DC	–	67	MHz
F _{BUSCLK}	Bus frequency	$1.71\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	DC	–	67	MHz
Svdd	V _{DD} ramp rate		–	–	1	V/ns
T _{IO_INIT}	Time from V _{DDD} /V _{DDA} /V _{CCD} /V _{CCA} ≥ IPOR to I/O ports set to their reset states		–	–	10	μs
T _{STARTUP}	Time from V _{DDD} /V _{DDA} /V _{CCD} /V _{CCA} ≥ PRES to CPU executing code at reset vector	V _{CCA} /V _{DDA} = regulated from V _{DDA} /V _{DDD} , no PLL used, fast IMO boot mode (48 MHz typ.)	–	–	33	μs
		V _{CCA} /V _{CCD} = regulated from V _{DDA} /V _{DDD} , no PLL used, slow IMO boot mode (12 MHz typ.)	–	–	66	μs
T _{SLEEP}	Wakeup from sleep mode – Application of non-LVD interrupt to beginning of execution of next CPU instruction		–	–	15	μs
T _{HIBERNATE}	Wakeup from hibernate mode – Application of external interrupt to beginning of execution of next CPU instruction		–	–	100	μs

Figure 11-1. F_{CPU} vs. V_{DD}



Note

24. Based on device characterization (Not production tested).

11.4 Inputs and Outputs

Specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.4.1 GPIO

Table 11-9. GPIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input voltage high threshold	CMOS Input, PRT[x]CTL = 0	$0.7 \times V_{DDIO}$	—	—	V
V_{IL}	Input voltage low threshold	CMOS Input, PRT[x]CTL = 0	—	—	$0.3 \times V_{DDIO}$	V
V_{IH}	Input voltage high threshold	LVTTL Input, PRT[x]CTL = 1, $V_{DDIO} < 2.7\text{ V}$	$0.7 \times V_{DDIO}$	—	—	V
V_{IH}	Input voltage high threshold	LVTTL Input, PRT[x]CTL = 1, $V_{DDIO} \geq 2.7\text{ V}$	2.0	—	—	V
V_{IL}	Input voltage low threshold	LVTTL Input, PRT[x]CTL = 1, $V_{DDIO} < 2.7\text{ V}$	—	—	$0.3 \times V_{DDIO}$	V
V_{IL}	Input voltage low threshold	LVTTL Input, PRT[x]CTL = 1, $V_{DDIO} \geq 2.7\text{ V}$	—	—	0.8	V
V_{OH}	Output voltage high	$I_{OH} = 4\text{ mA}$ at 3.3 V_{DDIO}	$V_{DDIO} - 0.6$	—	—	V
		$I_{OH} = 1\text{ mA}$ at 1.8 V_{DDIO}	$V_{DDIO} - 0.5$	—	—	V
V_{OL}	Output voltage low	$I_{OL} = 8\text{ mA}$ at 3.3 V_{DDIO}	—	—	0.6	V
		$I_{OL} = 4\text{ mA}$ at 1.8 V_{DDIO}	—	—	0.6	V
Rpullup	Pull-up resistor		3.5	5.6	8.5	k Ω
Rpulldown	Pull-down resistor		3.5	5.6	8.5	k Ω
I_{IL}	Input leakage current (absolute value) ^[29]	25 $^{\circ}\text{C}$, $V_{DDIO} = 3.0\text{ V}$	—	—	2	nA
C_{IN}	Input capacitance ^[29]	GPIOs without opamp outputs	—	—	7	pF
		GPIOs with opamp outputs	—	—	18	pF
V_H	Input voltage hysteresis (Schmitt-Trigger) ^[29]		—	40	—	mV
Idiode	Current through protection diode to V_{DDIO} and V_{SSIO}		—	—	100	μA
Rglobal	Resistance pin to analog global bus	25 $^{\circ}\text{C}$, $V_{DDIO} = 3.0\text{ V}$	—	320	—	Ω
Rmux	Resistance pin to analog mux bus	25 $^{\circ}\text{C}$, $V_{DDIO} = 3.0\text{ V}$	—	220	—	Ω

Table 11-10. GPIO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
TriseF	Rise time in Fast Strong Mode ^[29]	3.3 V V_{DDIO} Cload = 25 pF	—	—	12	ns
TfallF	Fall time in Fast Strong Mode ^[29]	3.3 V V_{DDIO} Cload = 25 pF	—	—	12	ns
TriseS	Rise time in Slow Strong Mode ^[29]	3.3 V V_{DDIO} Cload = 25 pF	—	—	60	ns
TfallS	Fall time in Slow Strong Mode ^[29]	3.3 V V_{DDIO} Cload = 25 pF	—	—	60	ns
Fgpioout	GPIO output operating frequency					
	3.3 V $\leq V_{DDIO} \leq 5.5\text{ V}$, fast strong drive mode	90/10% V_{DDIO} into 25 pF	—	—	33	MHz
	1.71 V $\leq V_{DDIO} < 3.3\text{ V}$, fast strong drive mode	90/10% V_{DDIO} into 25 pF	—	—	20	MHz
	3.3 V $\leq V_{DDIO} \leq 5.5\text{ V}$, slow strong drive mode	90/10% V_{DDIO} into 25 pF	—	—	7	MHz
	1.71 V $\leq V_{DDIO} < 3.3\text{ V}$, slow strong drive mode	90/10% V_{DDIO} into 25 pF	—	—	3.5	MHz
Fgpioin	GPIO input operating frequency					
	1.71 V $\leq V_{DDIO} \leq 5.5\text{ V}$	90/10% V_{DDIO}	—	—	66	MHz

Note

29. Based on device characterization (Not production tested).

Table 11-12. SIO AC Specifications (continued)

Parameter	Description	Conditions	Min	Typ	Max	Units
Fsioout	SIO output operating frequency					
	3.3 V < V _{DDIO} < 5.5 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% V _{DDIO} into 25 pF	–	–	33	MHz
	1.71 V < V _{DDIO} < 3.3 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% V _{DDIO} into 25 pF	–	–	16	MHz
	3.3 V < V _{DDIO} < 5.5 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V _{DDIO} into 25 pF	–	–	5	MHz
	1.71 V < V _{DDIO} < 3.3 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V _{DDIO} into 25 pF	–	–	4	MHz
	3.3 V < V _{DDIO} < 5.5 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	–	–	20	MHz
	1.71 V < V _{DDIO} < 3.3 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	–	–	10	MHz
	1.71 V < V _{DDIO} < 5.5 V, Regulated output mode, slow strong drive mode	Output continuously switching into 25 pF	–	–	2.5	MHz
Fsioin	SIO input operating frequency					
	1.71 V ≤ V _{DDIO} ≤ 5.5 V	90/10% V _{DDIO}	–	–	66	MHz

11.4.3 USBIO

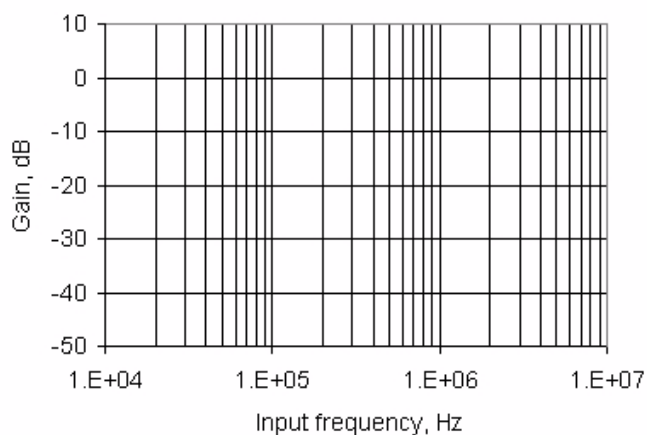
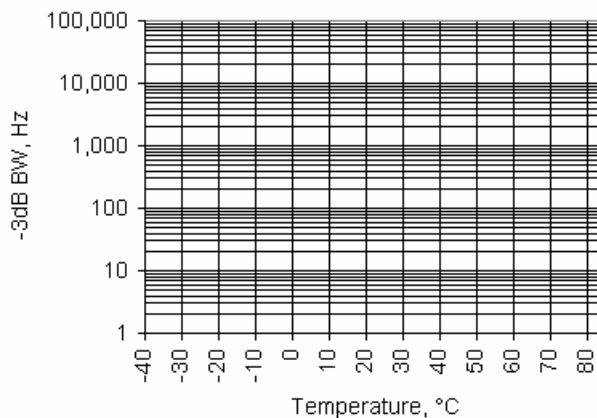
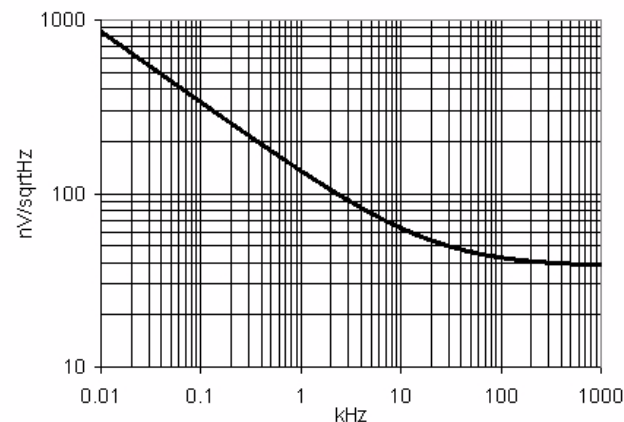
For operation in GPIO mode, the standard range for V_{DD} applies, see [Device Level Specifications](#) on page 60.

Table 11-13. USBIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ pull-up resistance	With idle bus	0.900	–	1.575	kΩ
Rusba	USB D+ pull-up resistance	While receiving traffic	1.425	–	3.090	kΩ
Vohusb	Static output high	15 kΩ ±5% to V _{ss} , internal pull-up enabled	2.8	–	3.6	V
Volusb	Static output low	15 kΩ ±5% to V _{ss} , internal pull-up enabled	–	–	0.3	V
Vohgpio	Output voltage high, GPIO mode	I _{OH} = 4 mA, V _{DD} ≥ 3 V	2.4	–	–	V
Volgpio	Output voltage low, GPIO mode	I _{OL} = 4 mA, V _{DD} ≥ 3 V	–	–	0.3	V
Vdi	Differential input sensitivity	[(D+) – (D–)]	–	–	0.2	V
Vcm	Differential input common mode range	–	0.8	–	2.5	V
Vse	Single ended receiver threshold	–	0.8	–	2	V
Rps2	PS/2 pull-up resistance	In PS/2 mode, with PS/2 pull-up enabled	3	–	7	kΩ
Rext	External USB series resistor	In series with each USB pin	21.78 (–1%)	22	22.22 (+1%)	Ω
Zo	USB driver output impedance	Including Rext	28	–	44	Ω
C _{IN}	USB transceiver input capacitance	–	–	–	20	pF
I _{IL}	Input leakage current (absolute value)	25 °C, V _{DD} = 3.0 V	–	–	2	nA

Table 11-38. PGA AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
BW1	–3 dB bandwidth	Power mode = high, gain = 1, input = 100 mV peak-to-peak	6.7	8	–	MHz
SR1	Slew rate	Power mode = high, gain = 1, 20% to 80%	3	–	–	V/μs
e _n	Input noise density	Power mode = high, Vdda = 5 V, at 100 kHz	–	43	–	nV/sqrtHz

Figure 11-44. Gain vs. Frequency, at Different Gain Settings, Vdda = 3.3 V, Power Mode = High

Figure 11-45. Bandwidth vs. Temperature, at Different Gain Settings, Power Mode = High

Figure 11-46. Noise vs. Frequency, Vdda = 5 V, Power Mode = High


11.5.11 Temperature Sensor

Table 11-39. Temperature Sensor Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Temp sensor accuracy	Range: –40 °C to +85 °C	–	±5	–	°C

11.7 Memory

Specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.7.1 Flash

Table 11-55. Flash DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	V_{DD} pin	1.71	–	5.5	V

Table 11-56. Flash AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{WRITE}	Row write time (erase + program)		–	–	15	ms
T_{ERASE}	Row erase time		–	–	10	ms
	Row program time		–	–	5	ms
T_{BULK}	Bulk erase time (16 KB to 64 KB)		–	–	35	ms
	Sector erase time (8 KB to 16 KB)		–	–	15	ms
	Total device program time (including JTAG, and so on)		–	–	5	seconds
	Flash endurance		100 k	–	–	program/erase cycles
	Flash data retention time, retention period measured from last erase cycle	Average ambient temp. $T_A \leq 55\text{ }^{\circ}\text{C}$, 100 K erase/program cycles	20	–	–	years

11.7.2 EEPROM

Table 11-57. EEPROM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage		1.71	–	5.5	V

Table 11-58. EEPROM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{WRITE}	Single row erase/write cycle time		–	2	15	ms
	EEPROM data retention time, retention period measured from last erase cycle (up to 100 K cycles)	Average ambient temp, $T_A \leq 25\text{ }^{\circ}\text{C}$, 1M erase/program cycles	20	–	–	years
		Average ambient temp, $T_A \leq 55\text{ }^{\circ}\text{C}$, 100 K erase/program cycles	20	–	–	

11.7.3 Nonvolatile Latches (NVL)

Table 11-59. NVL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	V_{DD} pin	1.71	–	5.5	V

Table 11-60. NVL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	NVL endurance	Programmed at $25\text{ }^{\circ}\text{C}$	1K	–	–	program/erase cycles
		Programmed at $0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$	100	–	–	program/erase cycles
	NVL data retention time	Programmed at $25\text{ }^{\circ}\text{C}$	20	–	–	years
		Programmed at $0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$	20	–	–	years

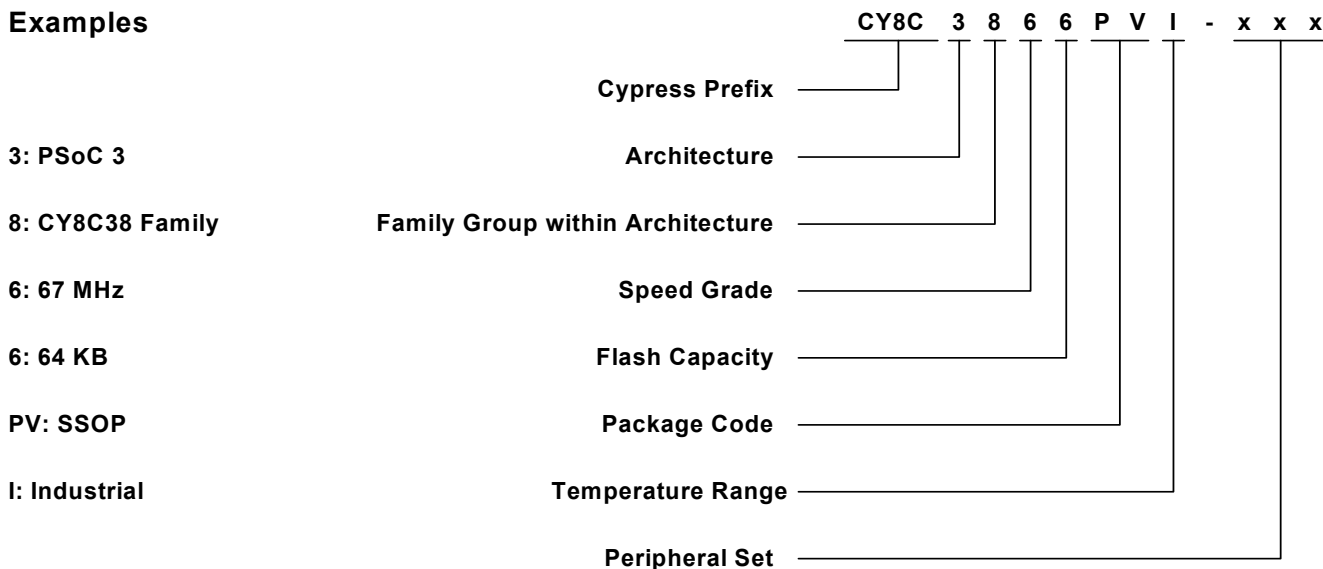
12.1 Part Numbering Conventions

PSoC 3 devices follow the part numbering convention described here. All fields are single character alphanumeric (0, 1, 2, ..., 9, A, B, ..., Z) unless stated otherwise.

CY8Cabcdefg-xxx

- **a:** Architecture
 - 3: PSoC 3
 - 5: PSoC 5
- **b:** Family group within architecture
 - 4: CY8C34 family
 - 6: CY8C36 family
 - 8: CY8C38 family
- **c:** Speed grade
 - 4: 48 MHz
 - 6: 67 MHz
- **d:** Flash capacity
 - 4: 16 KB
 - 5: 32 KB
 - 6: 64 KB
- **ef:** Package code
 - Two character alphanumeric
 - AX: TQFP
 - LT: QFN
 - PV: SSOP
- **g:** Temperature range
 - C: commercial
 - I: industrial
 - A: automotive
- **xxx:** Peripheral set
 - Three character numeric
 - No meaning is associated with these three characters.

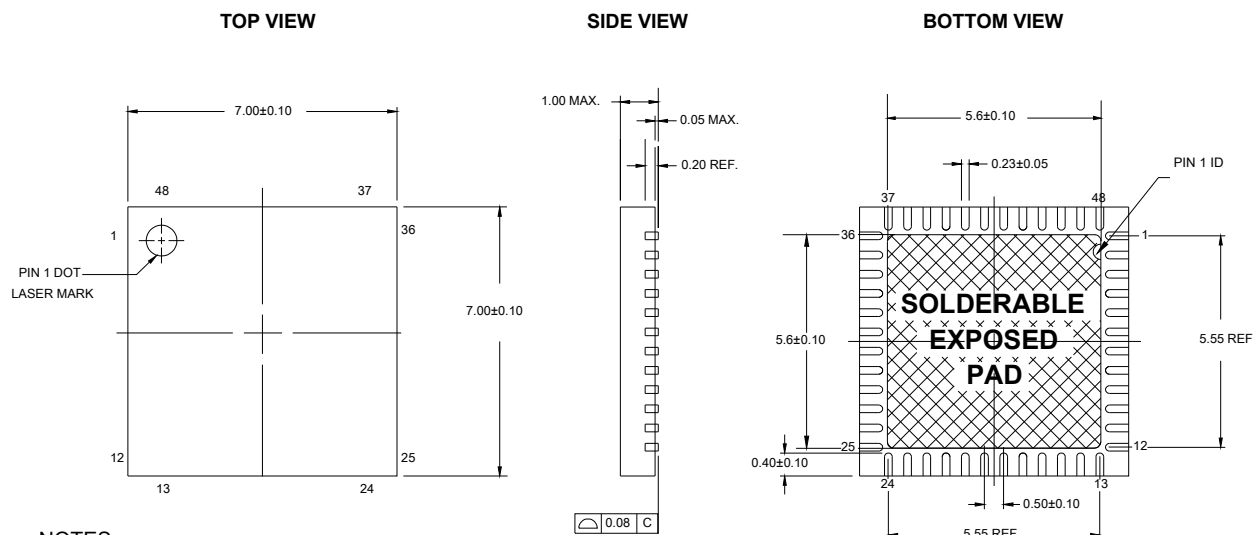
Examples




All devices in the PSoC 3 CY8C38 family comply to RoHS-6 specifications, demonstrating the commitment by Cypress to lead-free products. Lead (Pb) is an alloying element in solders that has resulted in environmental concerns due to potential toxicity. Cypress uses nickel-palladium-gold (NiPdAu) technology for the majority of leadframe-based packages.

A high-level review of the Cypress Pb-free position is available on our website. Specific package information is also available. Package Material Declaration Datasheets (PMDDs) identify all substances contained within Cypress packages. PMDDs also confirm the absence of many banned substances. The information in the PMDDs will help Cypress customers plan for recycling or other “end of life” requirements.

Figure 13-2. 48-pin QFN Package Outline



NOTES:

- 1.  HATCH AREA IS SOLDERABLE EXPOSED METAL.
- 2. REFERENCE JEDEC#: MO-220
- 3. PACKAGE WEIGHT: 0.13g
- 4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
- 5. PACKAGE CODE

PART #	DESCRIPTION
LT48D	LEAD FREE

001- 45616 *B

Description Title: PSoC® 3: CY8C38 Family Datasheet Programmable System-on-Chip (PSoC®)
Document Number: 001-11729

*K	2903576	04/01/2010	MKEA	<p>Updated Vb pin in PCB Schematic.</p> <p>Updated Tstartup parameter in AC Specifications table.</p> <p>Added Load regulation and Line regulation parameters to Inductive Boost Regulator DC Specifications table.</p> <p>Updated I_{CC} parameter in LCD Direct Drive DC Specs table.</p> <p>In page 1, updated internal oscillator range under Precision programmable clocking to start from 3 MHz.</p> <p>Updated I_{OUT} parameter in LCD Direct Drive DC Specs table.</p> <p>Updated Table 6-2 and Table 6-3.</p> <p>Added bullets on CapSense in page 1; added CapSense column in Section 12.</p> <p>Removed some references to footnote [1].</p> <p>Changed INC_Rn cycles from 3 to 2 (Table 4-1).</p> <p>Added footnote in PLL AC Specification table.</p> <p>Added PLL intermediate frequency row with footnote in PLL AC Specs table.</p> <p>Added UDBs subsection under 11.6 Digital Peripherals.</p> <p>Updated Figure 2-6 (PCB Layout). Updated Pin Descriptions section and modified Figures 6-6, 6-8, 6-9.</p> <p>Updated LVD in Tables 6-2 and 6-3; modified Low-power modes bullet in page 1.</p> <p>Added note to Figures 2-5 and 6-2; Updated Figure 6-2 to add capacitors for V_{DDA} and V_{DD} pins.</p> <p>Updated boost converter section (6.2.2).</p> <p>Updated Tstartup values in Table 11-3.</p> <p>Removed IPOR rows from Table 11-68.</p> <p>Updated 6.3.1.1, Power Voltage Level Monitors.</p> <p>Updated section 5.2 and Table 11-2 to correct suggestion of execution from flash.</p> <p>Updated V_{REF} specs in Table 11-21.</p> <p>Updated IDAC uncompensated gain error in Table 11-25.</p> <p>Updated Delay from Interrupt signal input to ISR code execution from ISR code in Table 11-72. Removed other line in table.</p> <p>Added sentence to last paragraph of section 6.1.1.3.</p> <p>Updated T_{RESP}, high and low-power modes, in Table 11-24.</p> <p>Updated f_{TCK} values in Table 11-73 and f_{SWDCK} values in Table 11-74.</p> <p>Updated SNR condition in Table 11-20.</p> <p>Corrected unit of measurement in Table 11-21.</p> <p>Updated sleep wakeup time in Table 6-3 and Tsleep in Table 11-3.</p> <p>Added 1.71 V ≤ V_{DD} < 3.3 V, SWD over USBIO pins value to Table 11-74.</p> <p>Removed mention of hibernate reset (HRES) from page 1 features, Table 6-3, Section 6.2.1.4, Section 6.3, and Section 6.3.1.1.</p> <p>Changed PPOR/PRES to TBDs in Section 6.3.1.1, Section 6.4.1.6 (changed PPOR to reset), Table 11-3 (changed PPOR to PRES), Table 11-68 (changed title, values TBD), and Table 11-69 (changed PPOR_TR to PRES_TR).</p> <p>Added sentence saying that LVD circuits can generate a reset to Section 6.3.1.1.</p> <p>Changed I_{DD} values on page 1, page 5, and Table 11-2.</p> <p>Changed resume time value in Section 6.2.1.3.</p> <p>Changed ESD HBM value in Table 11-1.</p> <p>Changed SNR in 16-bit resolution mode value and sample rate row in Table 11-20.</p> <p>Removed V_{DDA} = 1.65 V rows and changed BWag value in Table 11-22.</p> <p>Changed V_{IOFF} values and changed CMRR value in Table 11-23.</p> <p>Changed INL max value in Table 11-27.</p> <p>Added max value to the Quiescent current specs in Tables 11-29 and 11-31.</p> <p>Changed occurrences of "Block" to "Row" and deleted the "ECC not included" footnote in Table 11-57.</p> <p>Changed max response time value in Tables 11-69 and 11-71.</p> <p>Changed the Startup time in Table 11-79.</p> <p>Added condition to intermediate frequency row in Table 11-85.</p> <p>Added row to Table 11-69.</p> <p>Added brown out note to Section 11.8.1.</p>
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