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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	EBI/EMI, I ² C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x20b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3866lti-020

Table 4-3. Data Transfer Instructions *(continued)*

Mnemonic	Description	Bytes	Cycles
MOV Direct, Direct	Move direct byte to direct byte	3	3
MOV Direct, @Ri	Move indirect RAM to direct byte	2	3
MOV Direct, #data	Move immediate data to direct byte	3	3
MOV @Ri, A	Move accumulator to indirect RAM	1	2
MOV @Ri, Direct	Move direct byte to indirect RAM	2	3
MOV @Ri, #data	Move immediate data to indirect RAM	2	2
MOV DPTR, #data16	Load data pointer with 16 bit constant	3	3
MOVC A, @A+DPTR	Move code byte relative to DPTR to accumulator	1	5
MOVC A, @A + PC	Move code byte relative to PC to accumulator	1	4
MOVX A,@Ri	Move external RAM (8-bit) to accumulator	1	4
MOVX A, @DPTR	Move external RAM (16-bit) to accumulator	1	3
MOVX @Ri, A	Move accumulator to external RAM (8-bit)	1	5
MOVX @DPTR, A	Move accumulator to external RAM (16-bit)	1	4
PUSH Direct	Push direct byte onto stack	2	3
POP Direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange register with accumulator	1	2
XCH A, Direct	Exchange direct byte with accumulator	2	3
XCH A, @Ri	Exchange indirect RAM with accumulator	1	3
XCHD A, @Ri	Exchange low order indirect digit RAM with accumulator	1	3

Table 4-4. Boolean Instructions

Mnemonic	Description	Bytes	Cycles
CLR C	Clear carry	1	1
CLR bit	Clear direct bit	2	3
SETB C	Set carry	1	1
SETB bit	Set direct bit	2	3
CPL C	Complement carry	1	1
CPL bit	Complement direct bit	2	3
ANL C, bit	AND direct bit to carry	2	2
ANL C, /bit	AND complement of direct bit to carry	2	2
ORL C, bit	OR direct bit to carry	2	2
ORL C, /bit	OR complement of direct bit to carry	2	2
MOV C, bit	Move direct bit to carry	2	2
MOV bit, C	Move carry to direct bit	2	3
JC rel	Jump if carry is set	2	3
JNC rel	Jump if no carry is set	2	3
JB bit, rel	Jump if direct bit is set	3	5
JNB bit, rel	Jump if direct bit is not set	3	5
JBC bit, rel	Jump if direct bit is set and clear bit	3	5

4.4.2 DMA Features

- 24 DMA channels
- Each channel has one or more transaction descriptors (TD) to configure channel behavior. Up to 128 total TDs can be defined
- TDs can be dynamically updated
- Eight levels of priority per channel
- Any digitally routable signal, the CPU, or another DMA channel, can trigger a transaction
- Each channel can generate up to two interrupts per transfer
- Transactions can be stalled or canceled
- Supports transaction size of infinite or 1 to 64 KB
- TDs may be nested and/or chained for complex transactions

4.4.3 Priority Levels

The CPU always has higher priority than the DMA controller when their accesses require the same bus resources. Due to the system architecture, the CPU can never starve the DMA. DMA channels of higher priority (lower priority number) may interrupt current DMA transfers. In the case of an interrupt, the current transfer is allowed to complete its current transaction. To ensure latency limits when multiple DMA accesses are requested simultaneously, a fairness algorithm guarantees an interleaved minimum percentage of bus bandwidth for priority levels 2 through 7. Priority levels 0 and 1 do not take part in the fairness algorithm and may use 100 percent of the bus bandwidth. If a tie occurs on two DMA requests of the same priority level, a simple round robin method is used to evenly share the allocated bandwidth. The round robin allocation can be disabled for each DMA channel, allowing it to always be at the head of the line. Priority levels 2 to 7 are guaranteed the minimum bus bandwidth shown in Table 4-7 after the CPU and DMA priority levels 0 and 1 have satisfied their requirements.

Table 4-7. Priority Levels

Priority Level	% Bus Bandwidth
0	100.0
1	100.0
2	50.0
3	25.0
4	12.5
5	6.2
6	3.1
7	1.5

When the fairness algorithm is disabled, DMA access is granted based solely on the priority level; no bus bandwidth guarantees are made.

4.4.4 Transaction Modes Supported

The flexible configuration of each DMA channel and the ability to chain multiple channels allow the creation of both simple and complex use cases. General use cases include, but are not limited to:

4.4.4.1 Simple DMA

In a simple DMA case, a single TD transfers data between a source and sink (peripherals or memory location).

4.4.4.2 Auto Repeat DMA

Auto repeat DMA is typically used when a static pattern is repetitively read from system memory and written to a peripheral. This is done with a single TD that chains to itself.

4.4.4.3 Ping Pong DMA

A ping pong DMA case uses double buffering to allow one buffer to be filled by one client while another client is consuming the data previously received in the other buffer. In its simplest form, this is done by chaining two TDs together so that each TD calls the opposite TD when complete.

4.4.4.4 Circular DMA

Circular DMA is similar to ping pong DMA except it contains more than two buffers. In this case there are multiple TDs; after the last TD is complete it chains back to the first TD.

4.4.4.5 Scatter Gather DMA

In the case of scatter gather DMA, there are multiple noncontiguous sources or destinations that are required to effectively carry out an overall DMA transaction. For example, a packet may need to be transmitted off of the device and the packet elements, including the header, payload, and trailer, exist in various noncontiguous locations in memory. Scatter gather DMA allows the segments to be concatenated together by using multiple TDs in a chain. The chain gathers the data from the multiple locations. A similar concept applies for the reception of data onto the device. Certain parts of the received data may need to be scattered to various locations in memory for software processing convenience. Each TD in the chain specifies the location for each discrete element in the chain.

4.4.4.6 Packet Queuing DMA

Packet queuing DMA is similar to scatter gather DMA but specifically refers to packet protocols. With these protocols, there may be separate configuration, data, and status phases associated with sending or receiving a packet.

For instance, to transmit a packet, a memory mapped configuration register can be written inside a peripheral, specifying the overall length of the ensuing data phase. The CPU can set up this configuration information anywhere in system memory and copy it with a simple TD to the peripheral. After the configuration phase, a data phase TD (or a series of data phase TDs) can begin (potentially using scatter gather). When the data phase TD(s) finish, a status phase TD can be invoked that reads some memory mapped status information from the peripheral and copies it to a location in system memory specified by the CPU for later inspection. Multiple sets of configuration, data, and status phase 'subchains' can be strung together to create larger chains that transmit multiple packets in this way. A similar concept exists in the opposite direction to receive the packets.

4.4.4.7 Nested DMA

One TD may modify another TD, as the TD configuration space is memory mapped similar to any other peripheral. For example, a first TD loads a second TD's configuration and then calls the second TD. The second TD moves data as required by the application. When complete, the second TD calls the first TD, which again updates the second TD's configuration. This process repeats as often as necessary.

4.5 Interrupt Controller

The interrupt controller provides a mechanism for hardware resources to change program execution to a new address, independent of the current task being executed by the main code. The interrupt controller provides enhanced features not found on original 8051 interrupt controllers:

- Thirty-two interrupt vectors
- Jumps directly to ISR anywhere in code space with dynamic vector addresses
- Multiple sources for each vector
- Flexible interrupt to vector matching
- Each interrupt vector is independently enabled or disabled
- Each interrupt can be dynamically assigned one of eight priorities
- Eight level nestable interrupts
- Multiple I/O interrupt vectors
- Software can send interrupts
- Software can clear pending interrupts

When an interrupt is pending, the current instruction is completed and the program counter is pushed onto the stack. Code execution then jumps to the program address provided by the vector. After the ISR is completed, a RETI instruction is executed and returns execution to the instruction following the previously interrupted instruction. To do this the RETI instruction pops the program counter from the stack.

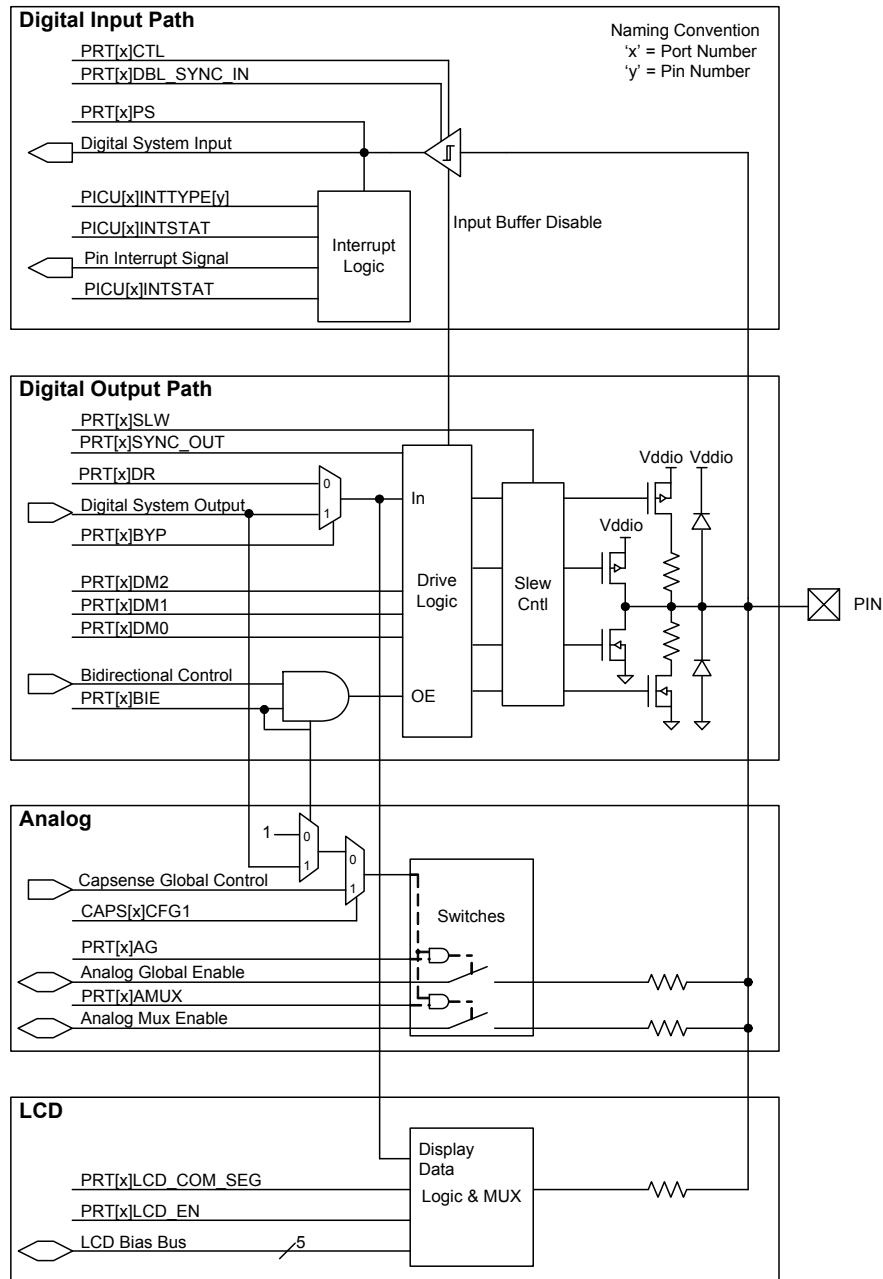
If the same priority level is assigned to two or more interrupts, the interrupt with the lower vector number is executed first. Each interrupt vector may choose from three interrupt sources: Fixed Function, DMA, and UDB. The fixed function interrupts are direct connections to the most common interrupt sources and provide the lowest resource cost connection. The DMA interrupt sources provide direct connections to the two DMA interrupt sources provided per DMA channel. The third interrupt source for vectors is from the UDB digital routing array. This allows any digital signal available to the UDB array to be used as an interrupt source.

Fixed function interrupts and all interrupt sources may be routed to any interrupt vector using the UDB interrupt source connections.

Table 4-8. Interrupt Vector Table

#	Fixed Function	DMA	UDB
0	LVD	phub_termout0[0]	udb_intr[0]
1	ECC	phub_termout0[1]	udb_intr[1]
2	Reserved	phub_termout0[2]	udb_intr[2]
3	Sleep (Pwr Mgr)	phub_termout0[3]	udb_intr[3]
4	PICU[0]	phub_termout0[4]	udb_intr[4]
5	PICU[1]	phub_termout0[5]	udb_intr[5]
6	PICU[2]	phub_termout0[6]	udb_intr[6]
7	PICU[3]	phub_termout0[7]	udb_intr[7]
8	PICU[4]	phub_termout0[8]	udb_intr[8]
9	PICU[5]	phub_termout0[9]	udb_intr[9]
10	PICU[6]	phub_termout0[10]	udb_intr[10]
11	PICU[12]	phub_termout0[11]	udb_intr[11]
12	PICU[15]	phub_termout0[12]	udb_intr[12]
13	Comparators Combined	phub_termout0[13]	udb_intr[13]
14	Switched Caps Combined	phub_termout0[14]	udb_intr[14]
15	I ² C	phub_termout0[15]	udb_intr[15]
16	CAN	phub_termout1[0]	udb_intr[16]
17	Timer/Counter0	phub_termout1[1]	udb_intr[17]
18	Timer/Counter1	phub_termout1[2]	udb_intr[18]
19	Timer/Counter2	phub_termout1[3]	udb_intr[19]
20	Timer/Counter3	phub_termout1[4]	udb_intr[20]
21	USB SOF Int	phub_termout1[5]	udb_intr[21]
22	USB Arb Int	phub_termout1[6]	udb_intr[22]
23	USB Bus Int	phub_termout1[7]	udb_intr[23]
24	USB Endpoint[0]	phub_termout1[8]	udb_intr[24]
25	USB Endpoint Data	phub_termout1[9]	udb_intr[25]
26	Reserved	phub_termout1[10]	udb_intr[26]
27	Reserved	phub_termout1[11]	udb_intr[27]
28	DFB Int	phub_termout1[12]	udb_intr[28]
29	Decimator Int	phub_termout1[13]	udb_intr[29]
30	PHUB Error Int	phub_termout1[14]	udb_intr[30]

Figure 6-8. GPIO Block Diagram



6.4.1 Drive Modes

Each GPIO and SIO pin is individually configurable into one of the eight drive modes listed in Table 6-6. Three configuration bits are used for each pin (DM[2:0]) and set in the PRTxDM[2:0] registers. Figure 6-11 depicts a simplified pin view based on each of the eight drive modes. Table 6-6 shows the I/O pin's drive state based on the port data register value or digital array signal if bypass mode is selected. Note that the actual I/O pin voltage is determined by a combination of the selected drive mode and the load at the pin. For example, if a GPIO pin is configured for resistive pull-up mode and driven high while the pin is floating, the voltage measured at the pin is a high logic state. If the same GPIO pin is externally tied to ground then the voltage unmeasured at the pin is a low logic state.

Figure 6-11. Drive Mode

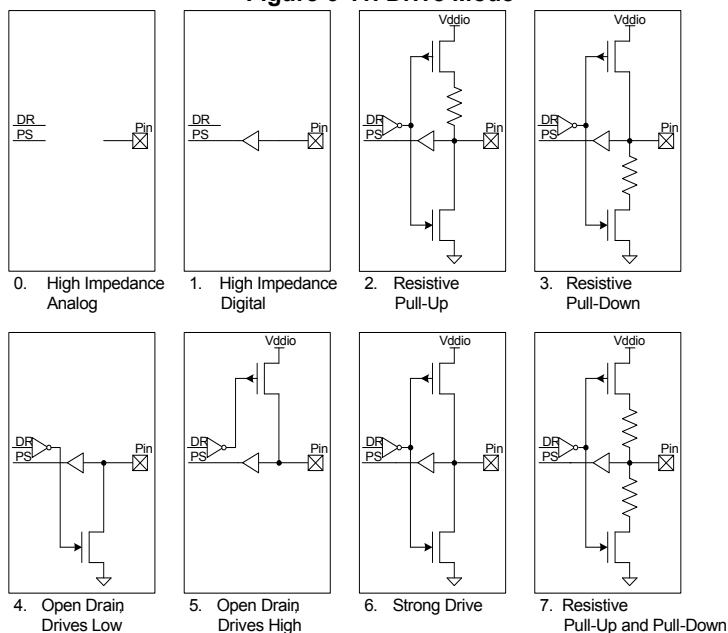


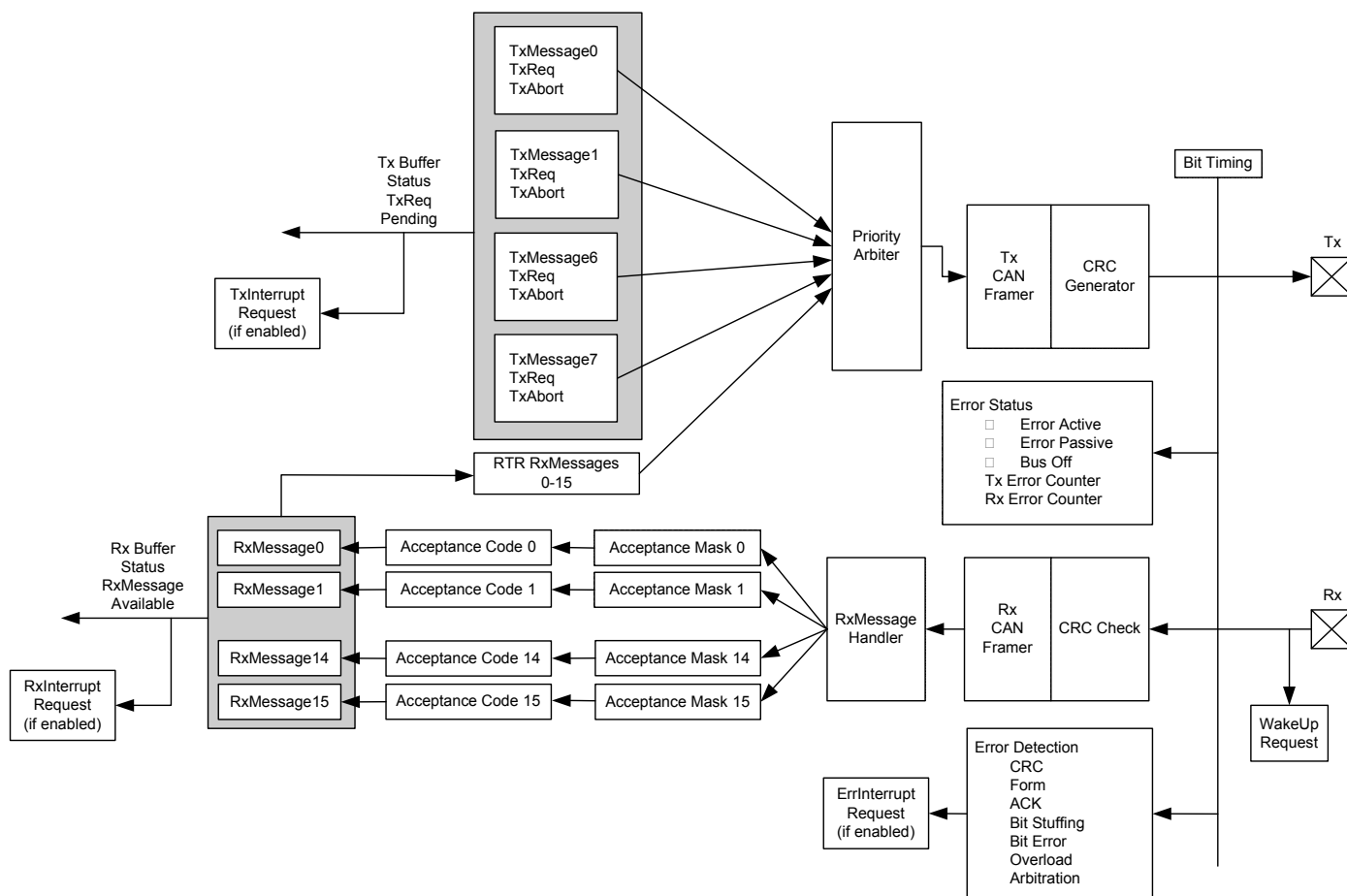
Table 6-6. Drive Modes

Diagram	Drive Mode	PRTxDM2	PRTxDM1	PRTxDM0	PRTxDR = 1	PRTxDR = 0
0	High impedance analog	0	0	0	High Z	High Z
1	High Impedance digital	0	0	1	High Z	High Z
2	Resistive pull-up ^[15]	0	1	0	Res High (5K)	Strong Low
3	Resistive pull-down ^[15]	0	1	1	Strong High	Res Low (5K)
4	Open drain, drives low	1	0	0	High Z	Strong Low
5	Open drain, drive high	1	0	1	Strong High	High Z
6	Strong drive	1	1	0	Strong High	Strong Low
7	Resistive pull-up and pull-down ^[15]	1	1	1	Res High (5K)	Res Low (5K)

Note

¹⁵ Resistive pull-up and pull-down are not available with SIO in regulated output mode.

Figure 7-19. CAN Controller Block Diagram



7.6 USB

PSoC includes a dedicated Full-Speed (12 Mbps) USB 2.0 transceiver supporting all four USB transfer types: control, interrupt, bulk, and isochronous. PSoC Creator provides full configuration support. USB interfaces to hosts through two dedicated USBIO pins, which are detailed in the “[I/O System and Routing](#)” section on page 28.

USB includes the following features:

- Eight unidirectional data endpoints
- One bidirectional control endpoint 0 (EP0)
- Shared 512-byte buffer for the eight data endpoints
- Dedicated 8-byte buffer for EP0
- Three memory modes
 - Manual memory management with no DMA access
 - Manual memory management with manual DMA access
 - Automatic memory management with automatic DMA access
- Internal 3.3-V regulator for transceiver

- Internal 48-MHz main oscillator mode that auto locks to USB bus clock, requiring no external crystal for USB (USB equipped parts only)
- Interrupts on bus and each endpoint event, with device wakeup
- USB reset, suspend, and resume operations
- Bus-powered and self-powered modes

Figure 7-20. USB

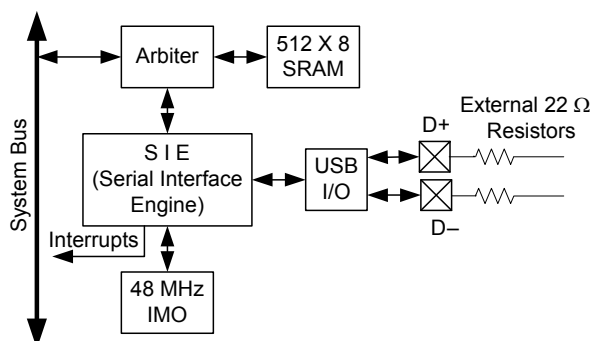
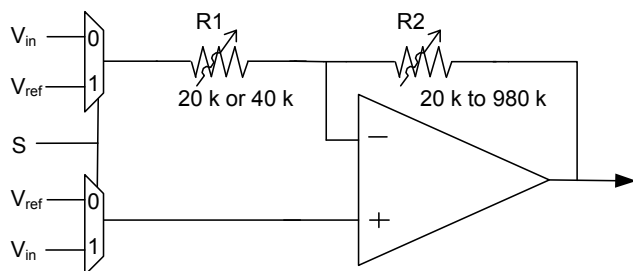


Table 8-3. Bandwidth

Gain	Bandwidth
1	6.0 MHz
24	340 kHz
48	220 kHz
50	215 kHz

Figure 8-9. PGA Resistor Settings


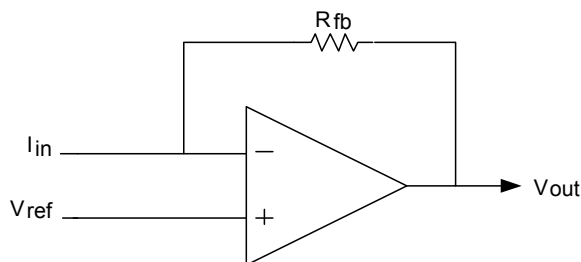
The PGA is used in applications where the input signal may not be large enough to achieve the desired resolution in the ADC, or dynamic range of another SC/CT block such as a mixer. The gain is adjustable at runtime, including changing the gain of the PGA prior to each ADC sample.

8.5.4 TIA

The Transimpedance Amplifier (TIA) converts an internal or external current to an output voltage. The TIA uses an internal feedback resistor in a continuous time configuration to convert input current to output voltage. For an input current I_{in} , the output voltage is $I_{in} \times R_{fb} + V_{REF}$, where V_{REF} is the value placed on the non inverting input. The feedback resistor R_{fb} is programmable between 20 K Ω and 1 M Ω through a configuration register. [Table 8-4](#) shows the possible values of R_{fb} and associated configuration settings.

Table 8-4. Feedback Resistor Settings

Configuration Word	Nominal R_{fb} (K Ω)
000b	20
001b	30
010b	40
011b	60
100b	120
101b	250
110b	500
111b	1000

Figure 8-10. Continuous Time TIA Schematic


The TIA configuration is used for applications where an external sensor's output is current as a function of some type of stimulus such as temperature, light, magnetic flux etc. In a common application, the voltage DAC output can be connected to the V_{REF} TIA input to allow calibration of the external sensor bias current by adjusting the voltage DAC output voltage.

8.6 LCD Direct Drive

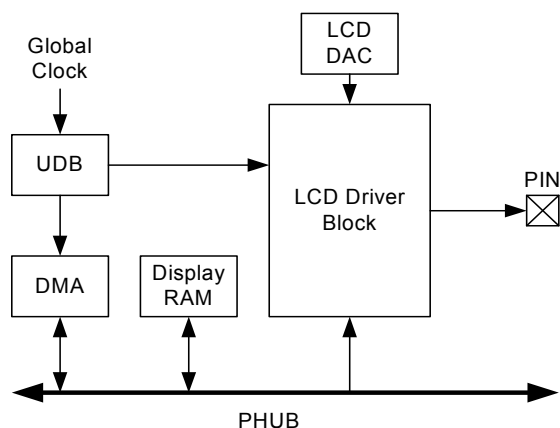
The PSoC LCD driver system is a highly configurable peripheral designed to allow PSoC to directly drive a broad range of LCD glass. All voltages are generated on chip, eliminating the need for external components. With a high multiplex ratio of up to 1/16, the CY8C38 family LCD driver system can drive a maximum of 736 segments. The PSoC LCD driver module was also designed with the conservative power budget of portable devices in mind, enabling different LCD drive modes and power down modes to conserve power.

PSoC Creator provides an LCD segment drive component. The component wizard provides easy and flexible configuration of LCD resources. You can specify pins for segments and commons along with other options. The software configures the device to meet the required specifications. This is possible because of the programmability inherent to PSoC devices.

Key features of the PSoC LCD segment system are:

- LCD panel direct driving
- Type A (standard) and Type B (low-power) waveform support
- Wide operating voltage range support (2 V to 5 V) for LCD panels
- Static, 1/2, 1/3, 1/4, 1/5 bias voltage levels
- Internal bias voltage generation through internal resistor ladder
- Up to 62 total common and segment outputs
- Up to 1/16 multiplex for a maximum of 16 backplane/common outputs
- Up to 62 front plane/segment outputs for direct drive
- Drives up to 736 total segments (16 backplane \times 46 front plane)
- Up to 64 levels of software controlled contrast
- Ability to move display data from memory buffer to LCD driver through DMA (without CPU intervention)
- Adjustable LCD refresh rate from 10 Hz to 150 Hz
- Ability to invert LCD display for negative image
- Three LCD driver drive modes, allowing power optimization

Figure 8-11. LCD System



8.6.1 LCD Segment Pin Driver

Each GPIO pin contains an LCD driver circuit. The LCD driver buffers the appropriate output of the LCD DAC to directly drive the glass of the LCD. A register setting determines whether the pin is a common or segment. The pin's LCD driver then selects one of the six bias voltages to drive the I/O pin, as appropriate for the display data.

8.6.2 Display Data Flow

The LCD segment driver system reads display data and generates the proper output voltages to the LCD glass to produce the desired image. Display data resides in a memory buffer in the system SRAM. Each time you need to change the common and segment driver voltages, the next set of pixel data moves from the memory buffer into the Port Data Registers through the DMA.

8.6.3 UDB and LCD Segment Control

A UDB is configured to generate the global LCD control signals and clocking. This set of signals is routed to each LCD pin driver through a set of dedicated LCD global routing channels. In addition to generating the global LCD control signals, the UDB also produces a DMA request to initiate the transfer of the next frame of LCD data.

8.6.4 LCD DAC

The LCD DAC generates the contrast control and bias voltage for the LCD system. The LCD DAC produces up to five LCD drive voltages plus ground, based on the selected bias ratio. The bias voltages are driven out to GPIO pins on a dedicated LCD bias bus, as required.

8.7 CapSense

The CapSense system provides a versatile and efficient means for measuring capacitance in applications such as touch sense buttons, sliders, proximity detection, etc. The CapSense system uses a configuration of system resources, including a few hardware functions primarily targeted for CapSense. Specific resource usage is detailed in the CapSense component in PSoc Creator.

A capacitive sensing method using a Delta-sigma Modulator (CSD) is used. It provides capacitance sensing using a switched capacitor technique with a delta-sigma modulator to convert the sensing current to a digital code.

8.8 Temp Sensor

Die temperature is used to establish programming parameters for writing flash. Die temperature is measured using a dedicated sensor based on a forward biased transistor. The temperature sensor has its own auxiliary ADC.

8.9 DAC

The CY8C38 parts contain up to four Digital to Analog Convertors (DACs). Each DAC is 8-bit and can be configured for either voltage or current output. The DACs support CapSense, power supply regulation, and waveform generation. Each DAC has the following features:

- Adjustable voltage or current output in 255 steps
- Programmable step size (range selection)
- Eight bits of calibration to correct ± 25 percent of gain error
- Source and sink option for current output
- 8 Msps conversion rate for current output
- 1 Msps conversion rate for voltage output
- Monotonic in nature
- Data and strobe inputs can be provided by the CPU or DMA, or routed directly from the DSI
- Dedicated low-resistance output pin for high-current mode

10. Development Support

The CY8C38 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit psoc.cypress.com/getting-started to find out more.

10.1 Documentation

A suite of documentation, supports the CY8C38 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component datasheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers.

10.2 Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

10.3 Tools

With industry standard cores, programming, and debugging interfaces, the CY8C38 family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Table 11-6. Inductive Boost Regulator DC Specifications (continued)

Unless otherwise specified, operating conditions are: $V_{BAT} = 2.4\text{ V}$, $V_{OUT} = 2.7\text{ V}$, $I_{OUT} = 40\text{ mA}$, $F_{SW} = 400\text{ kHz}$, $L_{BOOST} = 22\text{ }\mu\text{H}$, $C_{BOOST} = 22\text{ }\mu\text{F} \parallel 0.1\text{ }\mu\text{F}$

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OUT}	Boost voltage range ^[27, 28]					
	1.8 V		1.71	1.80	1.89	V
	1.9 V		1.81	1.90	2.00	V
	2.0 V		1.90	2.00	2.10	V
	2.4 V		2.28	2.40	2.52	V
	2.7 V		2.57	2.70	2.84	V
	3.0 V		2.85	3.00	3.15	V
	3.3 V		3.14	3.30	3.47	V
	3.6 V		3.42	3.60	3.78	V
	5.0 V	External diode required	4.75	5.00	5.25	V
Reg_{LOAD}	Load regulation		–	–	3.8	%
Reg_{LINE}	Line regulation		–	–	4.1	%
η_{OUT}	Efficiency	$L_{BOOST} = 10\text{ }\mu\text{H}$	70	85	–	%
		$L_{BOOST} = 22\text{ }\mu\text{H}$	82	90	–	%

Table 11-7. Inductive Boost Regulator AC Specifications

Unless otherwise specified, operating conditions are: $V_{BAT} = 2.4\text{ V}$, $V_{OUT} = 2.7\text{ V}$, $I_{OUT} = 40\text{ mA}$, $F_{SW} = 400\text{ kHz}$, $L_{BOOST} = 22\text{ }\mu\text{H}$, $C_{BOOST} = 22\text{ }\mu\text{F} \parallel 0.1\text{ }\mu\text{F}$.

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{RIPPLE}	Ripple voltage (peak-to-peak)	$V_{OUT} = 1.8\text{ V}$, $F_{SW} = 400\text{ kHz}$, $I_{OUT} = 10\text{ mA}$	–	–	100	mV
F_{SW}	Switching frequency		–	0.1, 0.4, or 2	–	MHz

Table 11-8. Recommended External Components for Boost Circuit

Parameter	Description	Conditions	Min	Typ	Max	Units
L_{BOOST}	Boost inductor		4.7	10	47	μH
C_{BOOST}	Filter capacitor ^[27]		10	22	47	μF
I_F	External Schottky diode average forward current	External Schottky diode is required for $V_{OUT} > 3.6\text{ V}$	1	–	–	A
V_R			20	–	–	V

Notes

27. Based on device characterization (Not production tested).

28. At boost frequency of 2 MHz, V_{boost} is limited to $2 \times V_{bat}$. At 400 kHz, V_{boost} is limited to $4 \times V_{bat}$.

11.5 Analog Peripherals

Specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.5.1 Opamp

Table 11-18. Opamp DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_i	Input voltage range		V_{SSA}	–	V_{DDA}	V
V_{os}	Input offset voltage		–	–	2.5	mV
		Operating temperature $-40\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$	–	–	2	mV
TCV_{os}	Input offset voltage drift with temperature	Power mode = high	–	± 12	–	$\mu\text{V}/^{\circ}\text{C}$
Ge_1	Gain error, unity gain buffer mode	$R_{load} = 1\text{ k}\Omega$	–	–	± 0.1	%
C_{in}	Input capacitance	Routing from pin	–	–	18	pF
V_o	Output voltage range	1 mA, source or sink, power mode = high	$V_{SSA} + 0.05$	–	$V_{DDA} - 0.05$	V
I_{out}	Output current, source or sink	$V_{SSA} + 500\text{ mV} \leq V_{out} \leq V_{DDA}$ $-500\text{ mV}, V_{DDA} > 2.7\text{ V}$	25	–	–	mA
		$V_{SSA} + 500\text{ mV} \leq V_{out} \leq V_{DDA}$ $-500\text{ mV}, 1.7\text{ V} = V_{DDA} \leq 2.7\text{ V}$	16	–	–	mA
I_{dd}	Quiescent current	Power mode = min	–	200	270	μA
		Power mode = low	–	250	400	μA
		Power mode = med	–	330	950	μA
		Power mode = high	–	1000	2500	μA
CMRR	Common mode rejection ratio		80	–	–	dB
PSRR	Power supply rejection ratio	$V_{dda} \geq 2.7\text{ V}$	85	–	–	dB
		$V_{dda} < 2.7\text{ V}$	70	–	–	dB

Figure 11-2. Opamp Voffset Histogram, 60 samples / 15 parts, $25\text{ }^{\circ}\text{C}$, $V_{dda} = 5\text{ V}$

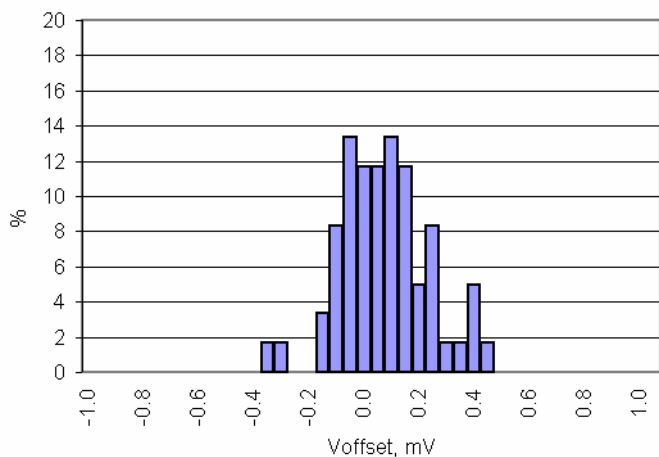


Figure 11-3. Opamp Voffset vs Temperature, $V_{dda} = 5\text{ V}$

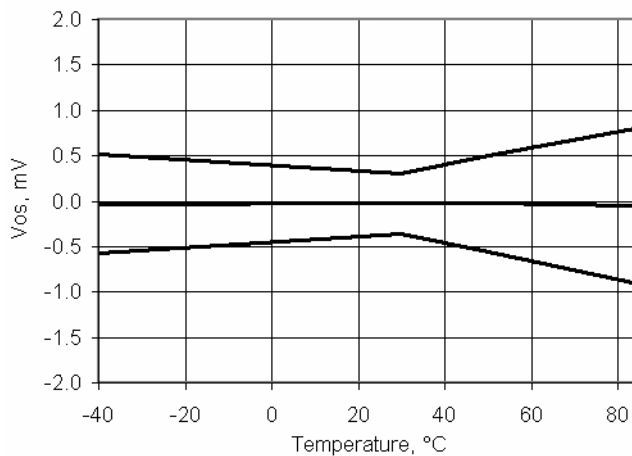


Figure 11-4. Opamp Voffset vs Common Mode Voltage and Temperature, Power Mode = High

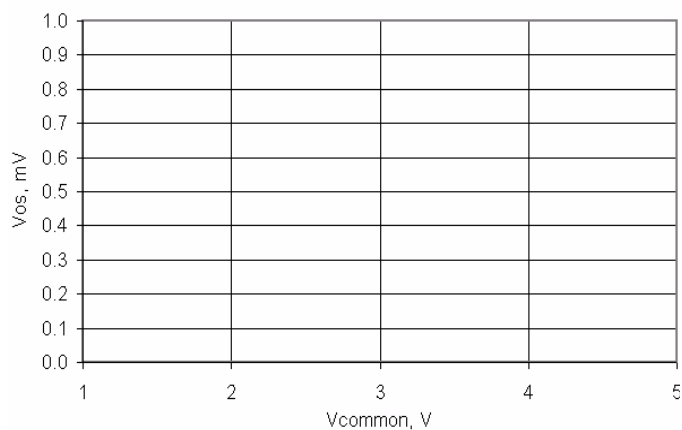


Figure 11-5. Opamp Output Voltage vs Load Current and Temperature, 25 °C, Vdda = 5V

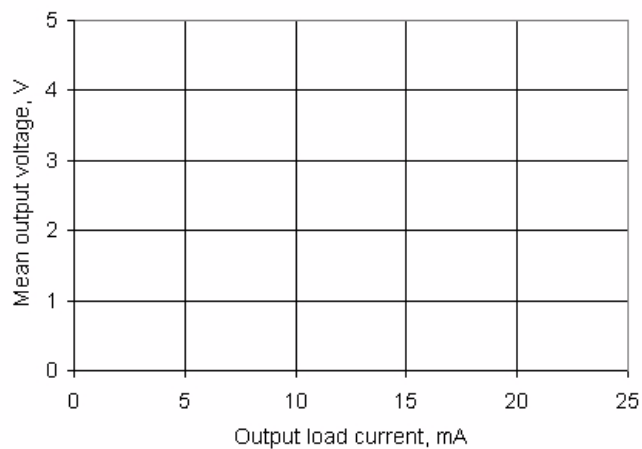


Figure 11-16. Opamp PSRR vs Frequency

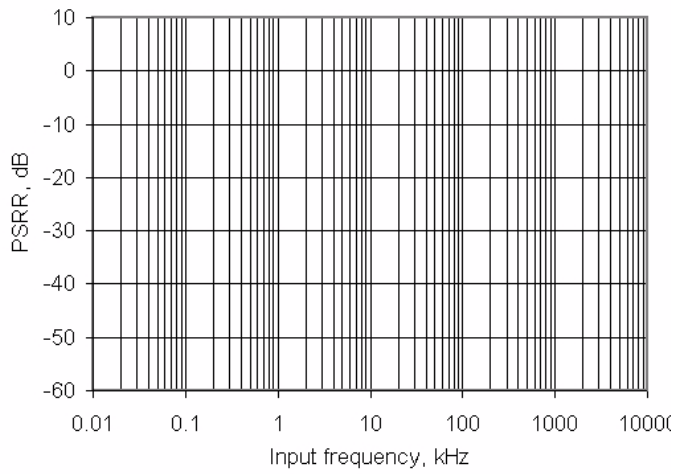


Table 11-22. Delta-sigma ADC Sample Rates, Range = ± 1.024 V

Resolution, Bits	Continuous		Multi-Sample		Multi-Sample Turbo	
	Min	Max	Min	Max	Min	Max
8	8000	384000	1911	91701	1829	87771
9	6400	307200	1543	74024	1489	71441
10	5566	267130	1348	64673	1307	62693
11	4741	227555	1154	55351	1123	53894
12	4000	192000	978	46900	956	45850
13	3283	157538	806	38641	791	37925
14	2783	133565	685	32855	674	32336
15	2371	113777	585	28054	577	27675
16	2000	48000	495	11861	489	11725
17	500	12000	124	2965	282	6766
18	125	3000	31	741	105	2513
19	16	375	4	93	15	357
20	8	187.5	2	46	8	183

Figure 11-17. Delta-sigma ADC I_{DD} vs sps, Range = ± 1.024 V

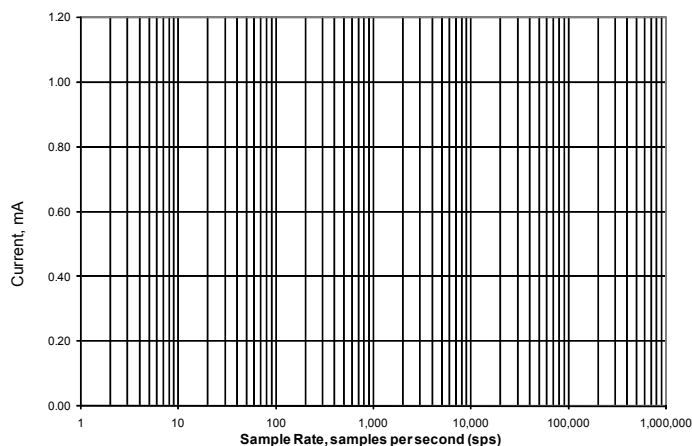


Figure 11-18. Delta-sigma ADC INL at Maximum Sample Rate

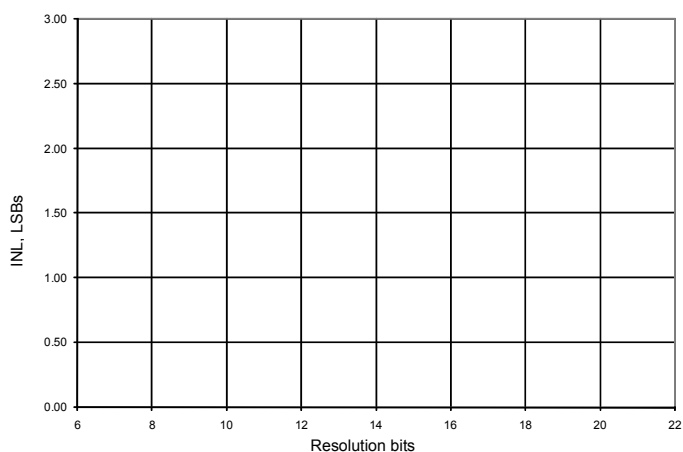


Figure 11-19. Delta-sigma ADC Noise Histogram, 1000 Samples, 20-Bit, 187 sps, Ext Ref, $V_{IN} = V_{REF}/2$, Range = ± 1.024 V

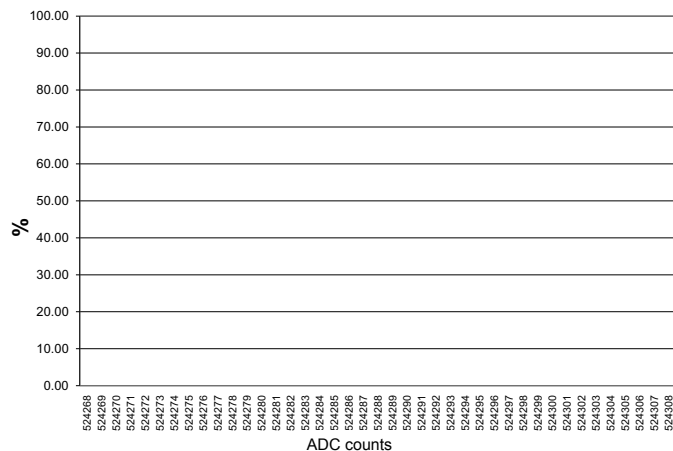


Figure 11-20. Delta-sigma ADC Noise Histogram, 1000 samples, 16-bit, 48 ksps, Ext Ref, $V_{IN} = V_{REF}/2$, Range = ± 1.024 V

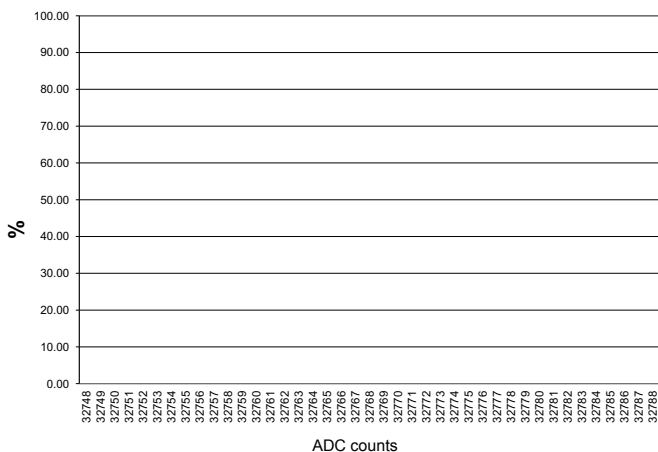


Figure 11-21. Delta-sigma ADC Noise Histogram, 1000 samples, 16-bit, 48 ksps, Int Ref, $V_{IN} = V_{REF}/2$, Range = ± 1.024 V

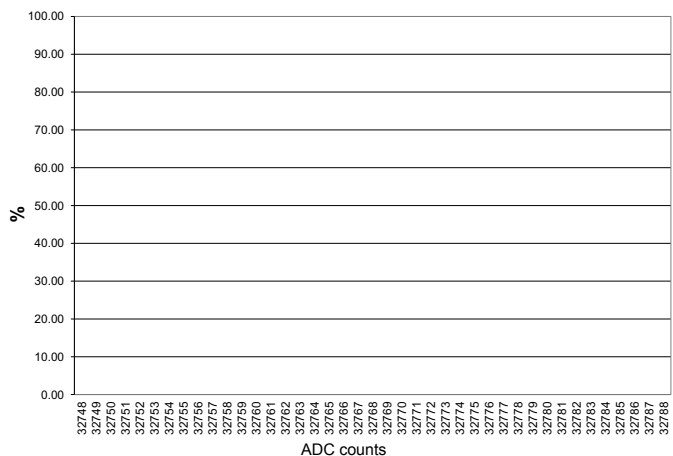


Figure 11-22. Delta-sigma ADC Noise Histogram, 1000 samples, 12-bit, 192 ksps, Int Ref, $V_{IN} = V_{REF}/2$, Range = ± 1.024 V

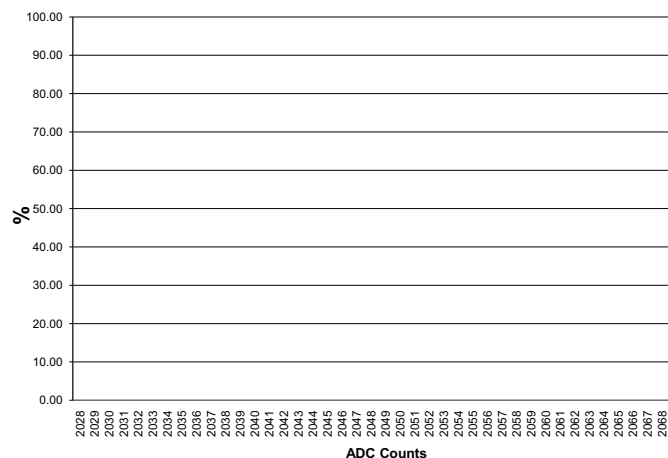


Table 11-23. Delta-sigma ADC RMS Noise vs. Input Range and Sample Rate, 20-bit, External Reference

RMS Noise, Counts	Input Voltage Range								
	Single-Ended				Differential				
Sample rate, sps	0 to V_{REF}	0 to $V_{REF} \times 2$	V_{SSA} to V_{DDA}	0 to $V_{REF} \times 6$	$\pm V_{REF}$	$\pm V_{REF}/2$	$\pm V_{REF}/4$	$\pm V_{REF}/8$	$\pm V_{REF}/16$
2.8									
5.6									
11.3									
22.5									
45									
90									
187.5									

Table 11-28. Comparator AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T _{RESP}	Response time, high current mode ^[39]	50 mV overdrive, measured pin-to-pin	–	75	110	ns
	Response time, low current mode ^[39]	50 mV overdrive, measured pin-to-pin	–	155	200	ns
	Response time, ultra low-power mode ^[39]	50 mV overdrive, measured pin-to-pin	–	55	–	μs

11.5.6 Current Digital-to-analog Converter(IDAC)

See the IDAC component datasheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, all charts and graphs show typical values.

Table 11-29. IDAC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		–	–	8	bits
I _{OUT}	Output current at code = 255	Range = 2.048 mA, code = 255, V _{DDA} ≥ 2.7 V, Rload = 600 Ω	–	2.048	–	mA
		Range = 2.048 mA, High mode, code = 255, V _{DDA} ≤ 2.7 V, Rload = 300 Ω	–	2.048	–	mA
		Range = 255 μA, code = 255, Rload = 600 Ω	–	255	–	μA
		Range = 31.875 μA, code = 255, Rload = 600 Ω	–	31.875	–	μA
	Monotonicity		–	–	Yes	
E _{zs}	Zero scale error		–	0	±1	LSB
E _g	Gain error	Range = 2.048 mA, 25 °C	–	–	±2.5	%
		Range = 255 μA, 25 °C	–	–	±2.5	%
		Range = 31.875 μA, 25 °C	–	–	±3.5	%
TC _{Eg}	Temperature coefficient of gain error	Range = 2.048 mA	–	–	0.04	% / °C
		Range = 255 μA	–	–	0.04	% / °C
		Range = 31.875 μA	–	–	0.05	% / °C
INL	Integral nonlinearity	Sink mode, range = 255 μA, Codes 8 – 255, Rload = 2.4 kΩ, Cload = 15 pF	–	±0.9	±1	LSB
		Source mode, range = 255 μA, Codes 8 – 255, Rload = 2.4 kΩ, Cload = 15 pF	–	±1.2	±1.5	LSB
DNL	Differential nonlinearity	Sink mode, range = 255 μA, Rload = 2.4 kΩ, Cload = 15 pF	–	±0.3	±1	LSB
		Source mode, range = 255 μA, Rload = 2.4 kΩ, Cload = 15 pF	–	±0.3	±1	LSB
V _{compliance}	Dropout voltage, source or sink mode	Voltage headroom at max current, Rload to Vdda or Rload to Vssa, Vdiff from Vdda	1	–	–	V

Note

39. Based on device characterization (Not production tested).

Figure 11-39. VDAC Full Scale Error vs Temperature, 1 V Mode

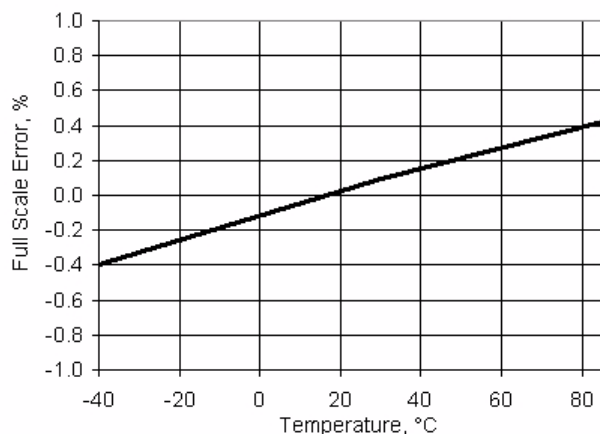


Figure 11-40. VDAC Full Scale Error vs Temperature, 4 V Mode

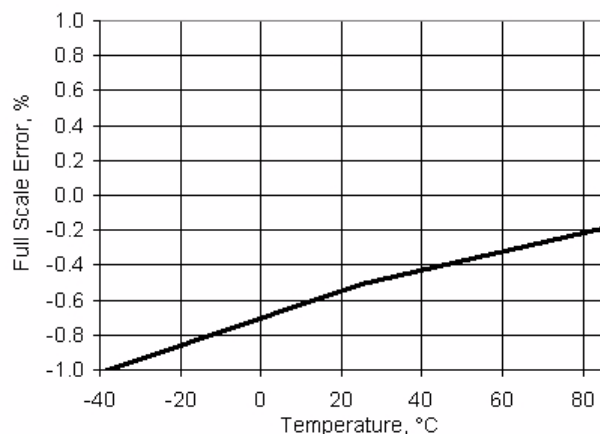


Figure 11-41. VDAC Operating Current vs Temperature, 1V Mode, Slow Mode

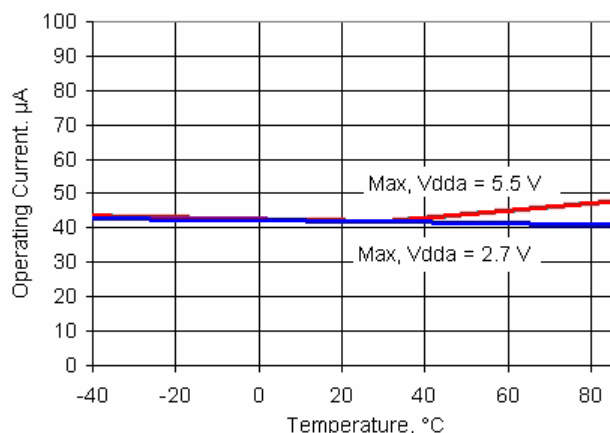


Figure 11-42. VDAC Operating Current vs Temperature, 1 V Mode, Fast Mode

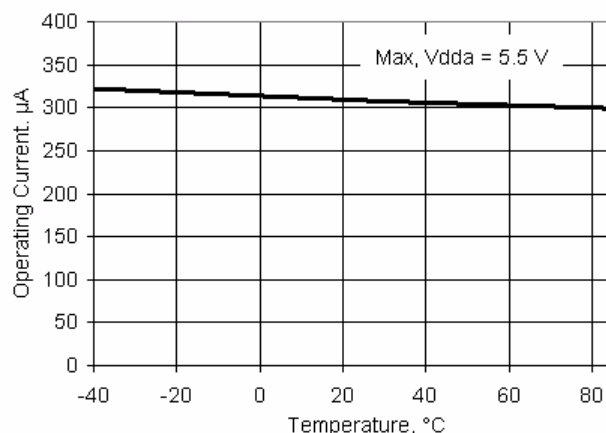


Table 11-32. VDAC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F _{DAC}	Update rate	1 V scale	–	–	1000	ksps
		4 V scale	–	–	250	ksps
T _{settleP}	Settling time to 0.1%, step 25% to 75%	1 V scale, Cload = 15 pF	–	0.45	1	µs
		4 V scale, Cload = 15 pF	–	0.8	3.2	µs
T _{settleN}	Settling time to 0.1%, step 75% to 25%	1 V scale, Cload = 15 pF	–	0.45	1	µs
		4 V scale, Cload = 15 pF	–	0.7	3	µs

11.6 Digital Peripherals

Specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.6.1 Timer

The following specifications apply to the Timer/Counter/PWM peripheral in timer mode. Timers can also be implemented in UDBs; for more information, see the Timer component datasheet in PSoC Creator.

Table 11-42. Timer DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit timer, at listed input clock frequency	–	–	–	μA
	3 MHz		–	15	–	μA
	12 MHz		–	60	–	μA
	48 MHz		–	260	–	μA
	67 MHz		–	350	–	μA

Table 11-43. Timer AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	67	MHz
	Capture pulse width (Internal)		15	–	–	ns
	Capture pulse width (external)		30	–	–	ns
	Timer resolution		15	–	–	ns
	Enable pulse width		15	–	–	ns
	Enable pulse width (external)		30	–	–	ns
	Reset pulse width		15	–	–	ns
	Reset pulse width (external)		30	–	–	ns

11.6.2 Counter

The following specifications apply to the Timer/Counter/PWM peripheral, in counter mode. Counters can also be implemented in UDBs; for more information, see the Counter component datasheet in PSoC Creator.

Table 11-44. Counter DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit counter, at listed input clock frequency	–	–	–	μA
	3 MHz		–	15	–	μA
	12 MHz		–	60	–	μA
	48 MHz		–	260	–	μA
	67 MHz		–	350	–	μA

Table 11-45. Counter AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	67	MHz
	Capture pulse		15	–	–	ns
	Resolution		15	–	–	ns
	Pulse width		15	–	–	ns
	Pulse width (external)		30	–	–	ns
	Enable pulse width		15	–	–	ns
	Enable pulse width (external)		30	–	–	ns
	Reset pulse width		15	–	–	ns
	Reset pulse width (external)		30	–	–	ns

11.7.4 SRAM

Table 11-61. SRAM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V _{SRAM}	SRAM retention voltage		1.2	–	–	V

Table 11-62. SRAM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F _{SRAM}	SRAM operating frequency		DC	–	67	MHz

11.7.5 External Memory Interface

Figure 11-48. Asynchronous Read Cycle Timing

