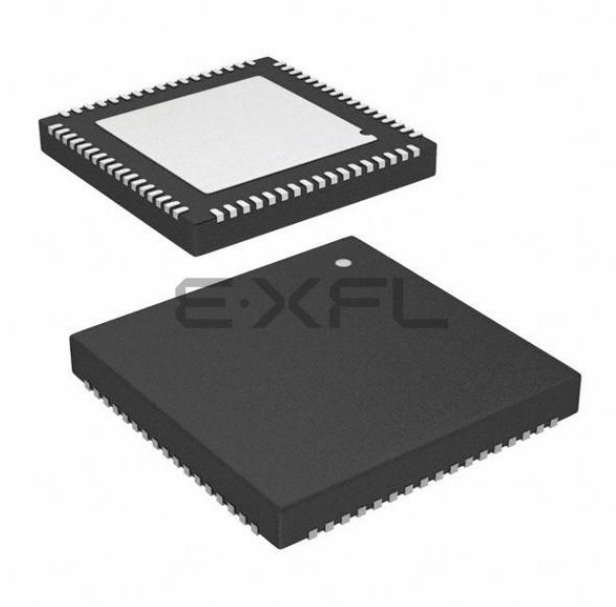

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x20b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3866lti-023

Table 4-3. Data Transfer Instructions *(continued)*

Mnemonic	Description	Bytes	Cycles
MOV Direct, Direct	Move direct byte to direct byte	3	3
MOV Direct, @Ri	Move indirect RAM to direct byte	2	3
MOV Direct, #data	Move immediate data to direct byte	3	3
MOV @Ri, A	Move accumulator to indirect RAM	1	2
MOV @Ri, Direct	Move direct byte to indirect RAM	2	3
MOV @Ri, #data	Move immediate data to indirect RAM	2	2
MOV DPTR, #data16	Load data pointer with 16 bit constant	3	3
MOVC A, @A+DPTR	Move code byte relative to DPTR to accumulator	1	5
MOVC A, @A + PC	Move code byte relative to PC to accumulator	1	4
MOVX A,@Ri	Move external RAM (8-bit) to accumulator	1	4
MOVX A, @DPTR	Move external RAM (16-bit) to accumulator	1	3
MOVX @Ri, A	Move accumulator to external RAM (8-bit)	1	5
MOVX @DPTR, A	Move accumulator to external RAM (16-bit)	1	4
PUSH Direct	Push direct byte onto stack	2	3
POP Direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange register with accumulator	1	2
XCH A, Direct	Exchange direct byte with accumulator	2	3
XCH A, @Ri	Exchange indirect RAM with accumulator	1	3
XCHD A, @Ri	Exchange low order indirect digit RAM with accumulator	1	3

Table 4-4. Boolean Instructions

Mnemonic	Description	Bytes	Cycles
CLR C	Clear carry	1	1
CLR bit	Clear direct bit	2	3
SETB C	Set carry	1	1
SETB bit	Set direct bit	2	3
CPL C	Complement carry	1	1
CPL bit	Complement direct bit	2	3
ANL C, bit	AND direct bit to carry	2	2
ANL C, /bit	AND complement of direct bit to carry	2	2
ORL C, bit	OR direct bit to carry	2	2
ORL C, /bit	OR complement of direct bit to carry	2	2
MOV C, bit	Move direct bit to carry	2	2
MOV bit, C	Move carry to direct bit	2	3
JC rel	Jump if carry is set	2	3
JNC rel	Jump if no carry is set	2	3
JB bit, rel	Jump if direct bit is set	3	5
JNB bit, rel	Jump if direct bit is not set	3	5
JBC bit, rel	Jump if direct bit is set and clear bit	3	5

5. Memory

5.1 Static RAM

CY8C38 SRAM is used for temporary data storage. Up to 8 KB of SRAM is provided and can be accessed by the 8051 or the DMA controller. See Memory Map on page 19. Simultaneous access of SRAM by the 8051 and the DMA controller is possible if different 4-KB blocks are accessed.

5.2 Flash Program Memory

Flash memory in PSoC devices provides nonvolatile storage for user firmware, user configuration data, bulk data storage, and optional ECC data. The main flash memory area contains up to 64 KB of user program space.

Up to an additional 8 KB of flash space is available for ECC. If ECC is not used this space can store device configuration data and bulk user data. User code may not be run out of the ECC flash memory section. ECC can correct one bit error and detect two bit errors per 8 bytes of firmware memory; an interrupt can be generated when an error is detected.

Flash is read in units of rows; each row is 9 bytes wide with 8 bytes of data and 1 byte of ECC data. When a row is read, the data bytes are copied into an 8-byte instruction buffer. The CPU fetches its instructions from this buffer, for improved CPU performance.

Flash programming is performed through a special interface and preempts code execution out of flash. The flash programming interface performs flash erasing, programming and setting code protection levels. Flash in-system serial programming (ISSP), typically used for production programming, is possible through both the SWD and JTAG interfaces. In-system programming, typically used for bootloaders, is also possible using serial interfaces such as I^2C, USB, UART, and SPI, or any communications protocol.

5.3 Flash Security

All PSoC devices include a flexible flash-protection model that prevents access and visibility to on-chip flash memory. This prevents duplication or reverse engineering of proprietary code. Flash memory is organized in blocks, where each block contains 256 bytes of program or data and 32 bytes of ECC or configuration data. A total of up to 256 blocks is provided on 64-KB flash devices.

The device offers the ability to assign one of four protection levels to each row of flash. Table 5-1 lists the protection modes available. Flash protection levels can only be changed by performing a complete flash erase. The Full Protection and Field Upgrade settings disable external access (through a debugging tool such as PSoC Creator, for example). If your application requires code update through a bootloader, then use the Field Upgrade setting. Use the Unprotected setting only when no security is needed in your application. The PSoC device also offers an advanced security feature called Device Security which permanently disables all test, programming, and debug ports, protecting your application from external access (see the "Device Security" section on page 57). For more information about how to take full advantage of the security features in PSoC, see the PSoC 3 TRM.

Table 5-1. Flash Protection

Protection Setting	Allowed	Not Allowed
Unprotected	External read and write + internal read and write	–
Factory Upgrade	External write + internal read and write	External read
Field Upgrade	Internal read and write	External read and write
Full Protection	Internal read	External read and write + internal write

Disclaimer

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress datasheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as 'unbreakable'. Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

5.4 EEPROM

PSoC EEPROM memory is a byte-addressable nonvolatile memory. The CY8C38 has up to 2 KB of EEPROM memory to store user data. Reads from EEPROM are random access at the byte level. Reads are done directly; writes are done by sending write commands to an EEPROM programming interface. CPU code execution can continue from flash during EEPROM writes. EEPROM is erasable and writeable at the row level. The EEPROM is divided into 128 rows of 16 bytes each. The CPU can not execute out of EEPROM. There is no ECC hardware associated with EEPROM. If ECC is required it must be handled in firmware.

5.5 External Memory Interface

CY8C38 provides an EMIF for connecting to external memory devices. The connection allows read and write accesses to external memories. The EMIF operates in conjunction with UDBs, I/O ports, and other hardware to generate external memory address and control signals. At 33 MHz, each memory access cycle takes four bus clock cycles. Figure 5-1 is the EMIF block diagram. The EMIF supports synchronous and asynchronous memories. The CY8C38 supports only one type of external memory device at a time. External memory can be accessed through the 8051 xdata space; up to 24 address bits can be used. See "xdata Space" section on page 21. The memory can be 8 or 16 bits wide.

6.4.1 Drive Modes

Each GPIO and SIO pin is individually configurable into one of the eight drive modes listed in Table 6-6. Three configuration bits are used for each pin (DM[2:0]) and set in the PRTxDM[2:0] registers. Figure 6-11 depicts a simplified pin view based on each of the eight drive modes. Table 6-6 shows the I/O pin's drive state based on the port data register value or digital array signal if bypass mode is selected. Note that the actual I/O pin voltage is determined by a combination of the selected drive mode and the load at the pin. For example, if a GPIO pin is configured for resistive pull-up mode and driven high while the pin is floating, the voltage measured at the pin is a high logic state. If the same GPIO pin is externally tied to ground then the voltage unmeasured at the pin is a low logic state.

Figure 6-11. Drive Mode

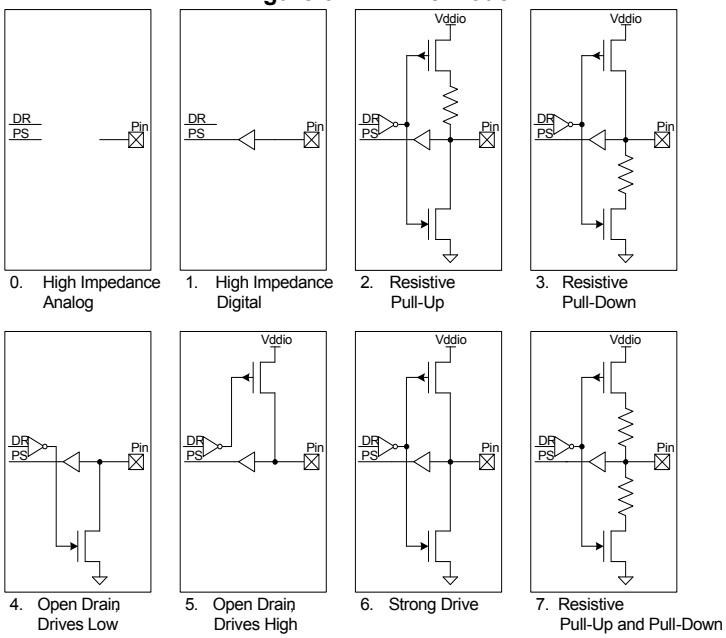


Table 6-6. Drive Modes

Diagram	Drive Mode	PRTxDM2	PRTxDM1	PRTxDM0	PRTxDR = 1	PRTxDR = 0
0	High impedence analog	0	0	0	High Z	High Z
1	High Impedance digital	0	0	1	High Z	High Z
2	Resistive pull-up[15]	0	1	0	Res High (5K)	Strong Low
3	Resistive pull-down[15]	0	1	1	Strong High	Res Low (5K)
4	Open drain, drives low	1	0	0	High Z	Strong Low
5	Open drain, drive high	1	0	1	Strong High	High Z
6	Strong drive	1	1	0	Strong High	Strong Low
7	Resistive pull-up and pull-down[15]	1	1	1	Res High (5K)	Res Low (5K)

Note
15. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

6.4.15 Over Voltage Tolerance

All I/O pins provide an over voltage tolerance feature at any operating V_{DD}.

- There are no current limitations for the SIO pins as they present a high impedance load to the external circuit where Vddio ≤ V_{IN} ≤ 5.5 V.
- The GPIO pins must be limited to 100 µA using a current limiting resistor. GPIO pins clamp the pin voltage to approximately one diode above the Vddio supply where Vddio ≤ V_{IN} ≤ V_{DDA}.
- In case of a GPIO pin configured for analog input/output, the analog voltage on the pin must not exceed the Vddio supply voltage to which the GPIO belongs.

A common application for this feature is connection to a bus such as I^2C where different devices are running from different supply voltages. In the I^2C case, the PSoC chip is configured into the Open Drain, Drives Low mode for the SIO pin. This allows an external pull-up to pull the I^2C bus voltage above the PSoC pin supply. For example, the PSoC chip could operate at 1.8 V, and an external device could run from 5 V. Note that the SIO pin's V_{IH} and V_{IL} levels are determined by the associated Vddio supply pin. The I/O pin must be configured into a high impedance drive mode, open drain low drive mode, or pull-down drive mode, for over voltage tolerance to work properly. Absolute maximum ratings for the device must be observed for all I/O pins.

6.4.16 Reset Configuration

While reset is active all I/Os are reset to and held in the High Impedance Analog state. After reset is released, the state can be reprogrammed on a port-by-port basis to pull-down or pull-up. To ensure correct reset operation, the port reset configuration data is stored in special nonvolatile registers. The stored reset data is automatically transferred to the port reset configuration registers at reset release.

6.4.17 Low-Power Functionality

In all low-power modes the I/O pins retain their state until the part is awakened and changed or reset. To awaken the part, use a pin interrupt, because the port interrupt logic continues to function in all low-power modes.

6.4.18 Special Pin Functionality

Some pins on the device include additional special functionality in addition to their GPIO or SIO functionality. The specific special function pins are listed in Pinouts on page 5. The special features are:

- Digital
  - 4- to 33-MHz crystal oscillator
  - 32.768-kHz crystal oscillator
  - Wake from sleep on I^2C address match. Any pin can be used for I^2C if wake from sleep is not required.
  - JTAG interface pins
  - SWD interface pins
  - SWV interface pins
  - External reset
- Analog
  - Opamp inputs and outputs
  - High current IDAC outputs
  - External reference inputs

6.4.19 JTAG Boundary Scan

The device supports standard JTAG boundary scan chains on all I/O pins for board level test.

7. Digital Subsystem

The digital programmable system creates application specific combinations of both standard and advanced digital peripherals and custom logic functions. These peripherals and logic are then interconnected to each other and to any pin on the device, providing a high level of design flexibility and IP security.

The features of the digital programmable system are outlined here to provide an overview of capabilities and architecture. You do not need to interact directly with the programmable digital system at the hardware and register level. PSoC Creator provides a high level schematic capture graphical interface to automatically place and route resources similar to PLDs.

The main components of the digital programmable system are:

- UDB – These form the core functionality of the digital programmable system. UDBs are a collection of uncommitted logic (PLD) and structural logic (Datapath) optimized to create all common embedded peripherals and customized functionality that are application or design specific.
- Universal digital block array – UDB blocks are arrayed within a matrix of programmable interconnect. The UDB array structure is homogeneous and allows for flexible mapping of digital functions onto the array. The array supports extensive and flexible routing interconnects between UDBs and the Digital System Interconnect.
- Digital system interconnect (DSI) – Digital signals from UDBs, fixed function peripherals, I/O pins, interrupts, DMA, and other system core signals are attached to the digital system interconnect to implement full featured device connectivity. The DSI allows any digital function to any pin or other feature routability when used with the universal digital block array.

Figure 7-1. CY8C38 Digital Programmable Architecture

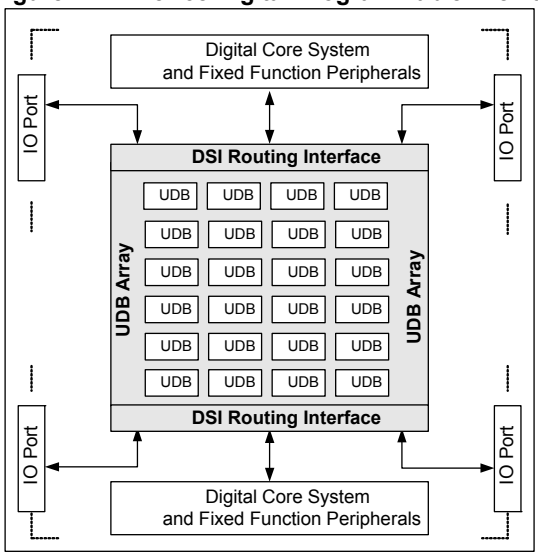
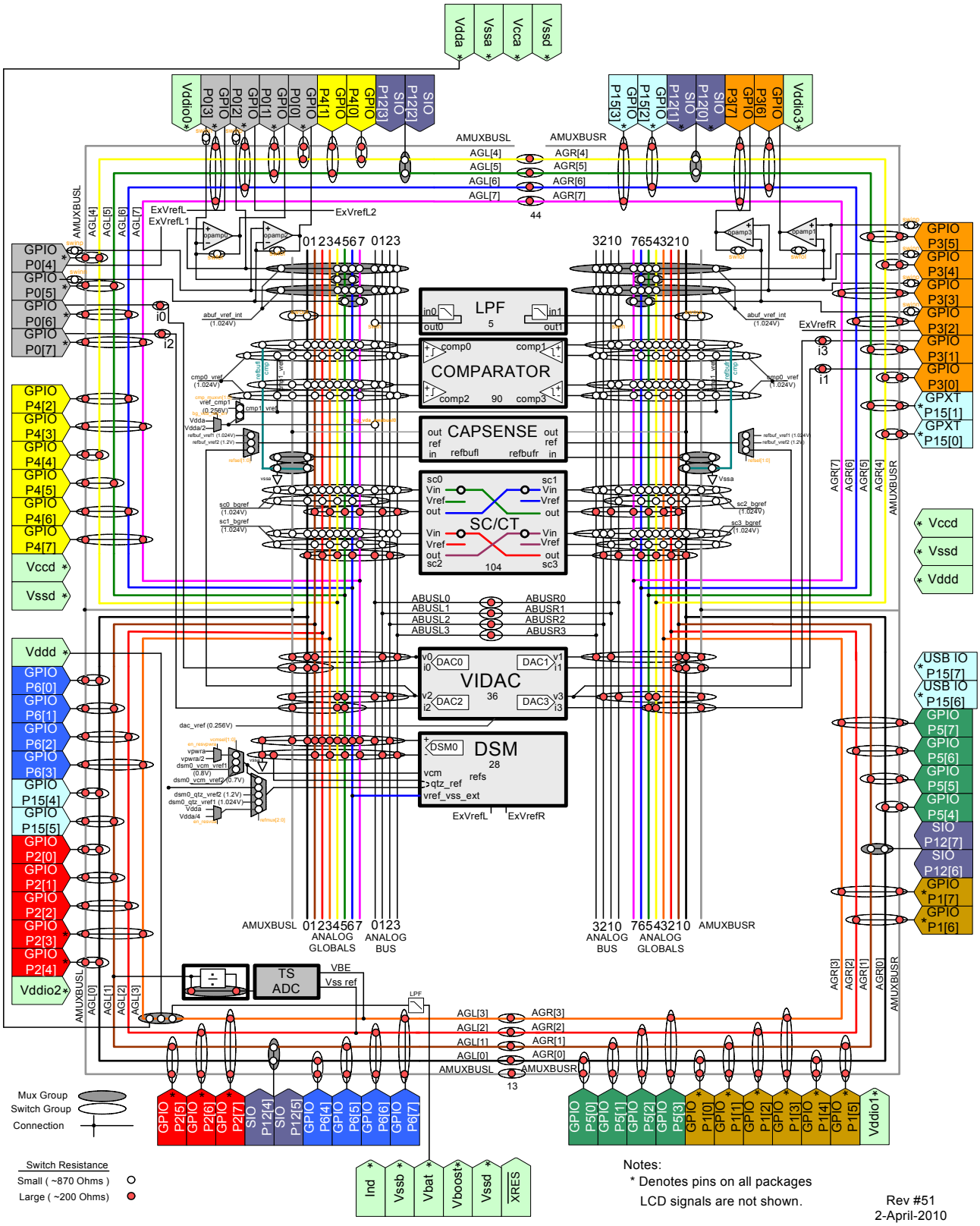


Figure 8-2. CY8C38 Analog Interconnect



asserts high and remains high until the value is read by either the DMA controller or the CPU.

8.2.2.1 Single Sample

In Single Sample mode, the ADC performs one sample conversion on a trigger. In this mode, the ADC stays in standby state waiting for the SoC signal to be asserted. When SoC is signaled the ADC performs four successive conversions. The first three conversions prime the decimator. The ADC result is valid and available after the fourth conversion, at which time the EoC signal is generated. To detect the end of conversion, the system may poll a control register for status or configure the external EoC signal to generate an interrupt or invoke a DMA request. When the transfer is done the ADC reenters the standby state where it stays until another SoC event.

8.2.2.2 Continuous

Continuous sample mode is used to take multiple successive samples of a single input signal. Multiplexing multiple inputs should not be done with this mode. There is a latency of three conversion times before the first conversion result is available. This is the time required to prime the decimator. After the first result, successive conversions are available at the selected sample rate.

8.2.2.3 Multi Sample

Multi sample mode is similar to continuous mode except that the ADC is reset between samples. This mode is useful when the input is switched between multiple signals. The decimator is re-primed between each sample so that previous samples do not affect the current conversion. Upon completion of a sample, the next sample is automatically initiated. The results can be transferred using either firmware polling, interrupt, or DMA.

8.2.2.4 Multi Sample (Turbo)

The multi sample (turbo) mode operates identical to the Multi-sample mode for resolutions of 8 to 16 bits. For resolutions of 17 to 20 bits, the performance is about four times faster than the multi sample mode, because the ADC is only reset once at the end of conversion.

More information on output formats is provided in the Technical Reference Manual.

8.2.3 Start of Conversion Input

The SoC signal is used to start an ADC conversion. A digital clock or UDB output can be used to drive this input. It can be used when the sampling period must be longer than the ADC conversion time or when the ADC must be synchronized to other hardware. This signal is optional and does not need to be connected if ADC is running in a continuous mode.

8.2.4 End of Conversion Output

The EoC signal goes high at the end of each ADC conversion. This signal may be used to trigger either an interrupt or DMA request.

8.3 Comparators

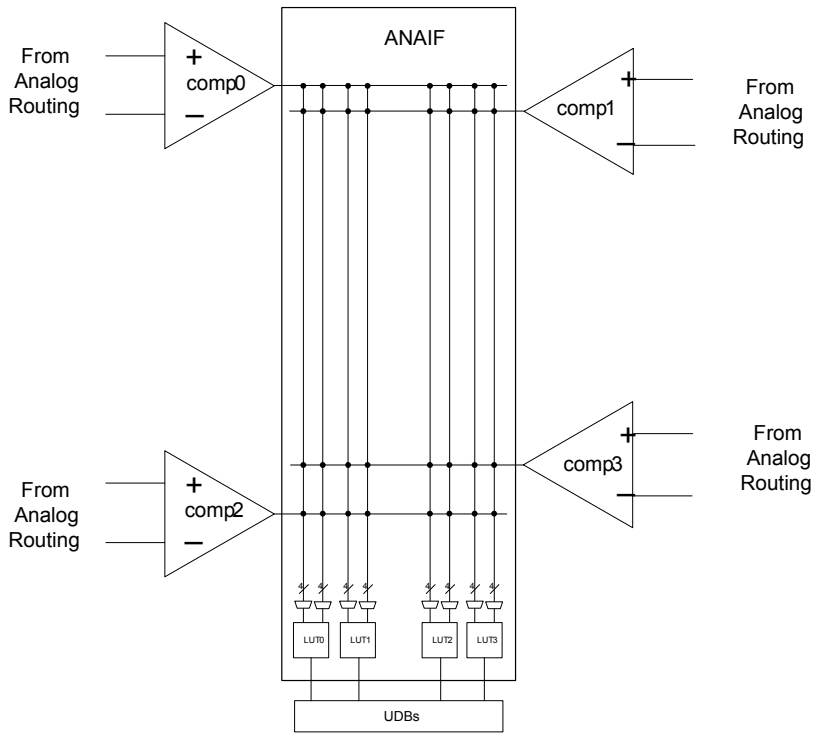
The CY8C38 family of devices contains four comparators in a device. Comparators have these features:

- Input offset factory trimmed to less than 5 mV
- Rail-to-rail common mode input range (V_{SSA} to V_{DDA})
- Speed and power can be traded off by using one of three modes: fast, slow, or ultra low-power
- Comparator outputs can be routed to lookup tables to perform simple logic functions and then can also be routed to digital blocks
- The positive input of the comparators may be optionally passed through a low pass filter. Two filters are provided
- Comparator inputs can be connections to GPIO, DAC outputs and SC block outputs

8.3.1 Input and Output Interface

The positive and negative inputs to the comparators come from the analog global buses, the analog mux line, the analog local bus and precision reference through multiplexers. The output from each comparator could be routed to any of the two input LUTs. The output of that LUT is routed to the UDB DSI.

Figure 8-6. Analog Comparator



8.3.2 LUT

The CY8C38 family of devices contains four LUTs. The LUT is a two input, one output lookup table that is driven by any one or two of the comparators in the chip. The output of any LUT is routed to the digital system interface of the UDB array. From the digital system interface of the UDB array, these signals can be connected to UDBs, DMA controller, I/O, or the interrupt controller.

The LUT control word written to a register sets the logic function on the output. The available LUT functions and the associated control word is shown in Table 8-2.

Table 8-2. LUT Function vs. Program Word and Inputs

Control Word	Output (A and B are LUT inputs)
0000b	**FALSE** (‘0’)
0001b	**A** AND **B**
0010b	**A** AND (NOT **B**)
0011b	A
0100b	(NOT **A**) AND **B**
0101b	B
0110b	**A** XOR **B**
0111b	**A** OR **B**
1000b	**A** NOR **B**
1001b	**A** XNOR **B**
1010b	NOT **B**
1011b	**A** OR (NOT **B**)
1100b	NOT **A**
1101b	(NOT **A**) OR **B**
1110b	**A** NAND **B**
1111b	**TRUE** (‘1’)

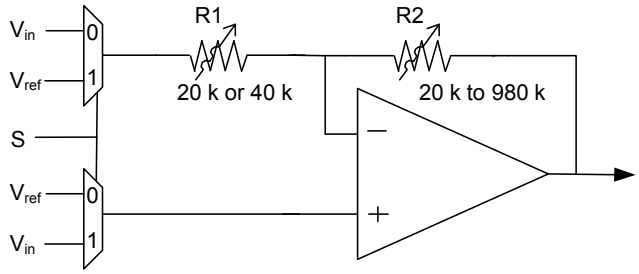
8.4 Opamps

The CY8C38 family of devices contain up to four general purpose opamps in a device.

Table 8-3. Bandwidth

Gain	Bandwidth
1	6.0 MHz
24	340 kHz
48	220 kHz
50	215 kHz

Figure 8-9. PGA Resistor Settings



The PGA is used in applications where the input signal may not be large enough to achieve the desired resolution in the ADC, or dynamic range of another SC/CT block such as a mixer. The gain is adjustable at runtime, including changing the gain of the PGA prior to each ADC sample.

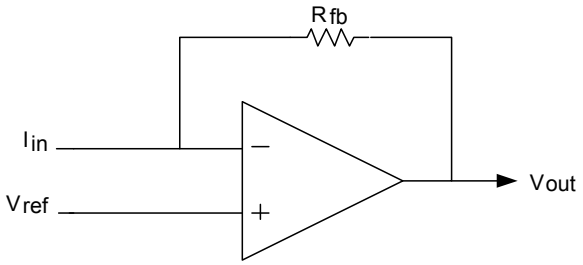
8.5.4 TIA

The Transimpedance Amplifier (TIA) converts an internal or external current to an output voltage. The TIA uses an internal feedback resistor in a continuous time configuration to convert input current to output voltage. For an input current Iin, the output voltage is Iin x Rfb +V_{REF}, where V_{REF} is the value placed on the non inverting input. The feedback resistor Rfb is programmable between 20 KΩ and 1 MΩ through a configuration register. Table 8-4 shows the possible values of Rfb and associated configuration settings.

Table 8-4. Feedback Resistor Settings

Configuration Word	Nominal R_{fb} (KΩ)
000b	20
001b	30
010b	40
011b	60
100b	120
101b	250
110b	500
111b	1000

Figure 8-10. Continuous Time TIA Schematic



The TIA configuration is used for applications where an external sensor's output is current as a function of some type of stimulus such as temperature, light, magnetic flux etc. In a common application, the voltage DAC output can be connected to the V_{REF} TIA input to allow calibration of the external sensor bias current by adjusting the voltage DAC output voltage.

8.6 LCD Direct Drive

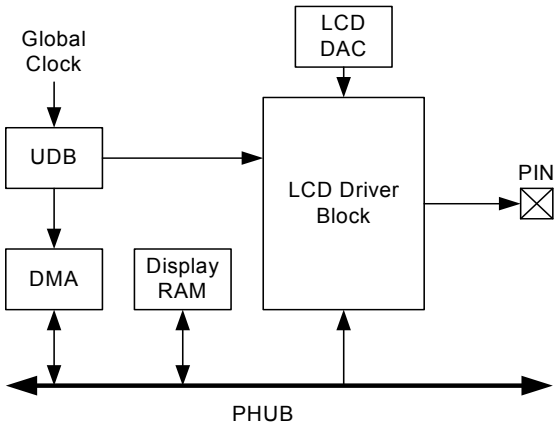
The PSoC LCD driver system is a highly configurable peripheral designed to allow PSoC to directly drive a broad range of LCD glass. All voltages are generated on chip, eliminating the need for external components. With a high multiplex ratio of up to 1/16, the CY8C38 family LCD driver system can drive a maximum of 736 segments. The PSoC LCD driver module was also designed with the conservative power budget of portable devices in mind, enabling different LCD drive modes and power down modes to conserve power.

PSoC Creator provides an LCD segment drive component. The component wizard provides easy and flexible configuration of LCD resources. You can specify pins for segments and commons along with other options. The software configures the device to meet the required specifications. This is possible because of the programmability inherent to PSoC devices.

Key features of the PSoC LCD segment system are:

- LCD panel direct driving
- Type A (standard) and Type B (low-power) waveform support
- Wide operating voltage range support (2 V to 5 V) for LCD panels
- Static, 1/2, 1/3, 1/4, 1/5 bias voltage levels
- Internal bias voltage generation through internal resistor ladder
- Up to 62 total common and segment outputs
- Up to 1/16 multiplex for a maximum of 16 backplane/common outputs
- Up to 62 front plane/segment outputs for direct drive
- Drives up to 736 total segments (16 backplane × 46 front plane)
- Up to 64 levels of software controlled contrast
- Ability to move display data from memory buffer to LCD driver through DMA (without CPU intervention)
- Adjustable LCD refresh rate from 10 Hz to 150 Hz
- Ability to invert LCD display for negative image
- Three LCD driver drive modes, allowing power optimization

Figure 8-11. LCD System



8.6.1 LCD Segment Pin Driver

Each GPIO pin contains an LCD driver circuit. The LCD driver buffers the appropriate output of the LCD DAC to directly drive the glass of the LCD. A register setting determines whether the pin is a common or segment. The pin's LCD driver then selects one of the six bias voltages to drive the I/O pin, as appropriate for the display data.

8.6.2 Display Data Flow

The LCD segment driver system reads display data and generates the proper output voltages to the LCD glass to produce the desired image. Display data resides in a memory buffer in the system SRAM. Each time you need to change the common and segment driver voltages, the next set of pixel data moves from the memory buffer into the Port Data Registers through the DMA.

8.6.3 UDB and LCD Segment Control

A UDB is configured to generate the global LCD control signals and clocking. This set of signals is routed to each LCD pin driver through a set of dedicated LCD global routing channels. In addition to generating the global LCD control signals, the UDB also produces a DMA request to initiate the transfer of the next frame of LCD data.

8.6.4 LCD DAC

The LCD DAC generates the contrast control and bias voltage for the LCD system. The LCD DAC produces up to five LCD drive voltages plus ground, based on the selected bias ratio. The bias voltages are driven out to GPIO pins on a dedicated LCD bias bus, as required.

8.7 CapSense

The CapSense system provides a versatile and efficient means for measuring capacitance in applications such as touch sense buttons, sliders, proximity detection, etc. The CapSense system uses a configuration of system resources, including a few hardware functions primarily targeted for CapSense. Specific resource usage is detailed in the CapSense component in PSoC Creator.

A capacitive sensing method using a Delta-sigma Modulator (CSD) is used. It provides capacitance sensing using a switched capacitor technique with a delta-sigma modulator to convert the sensing current to a digital code.

8.8 Temp Sensor

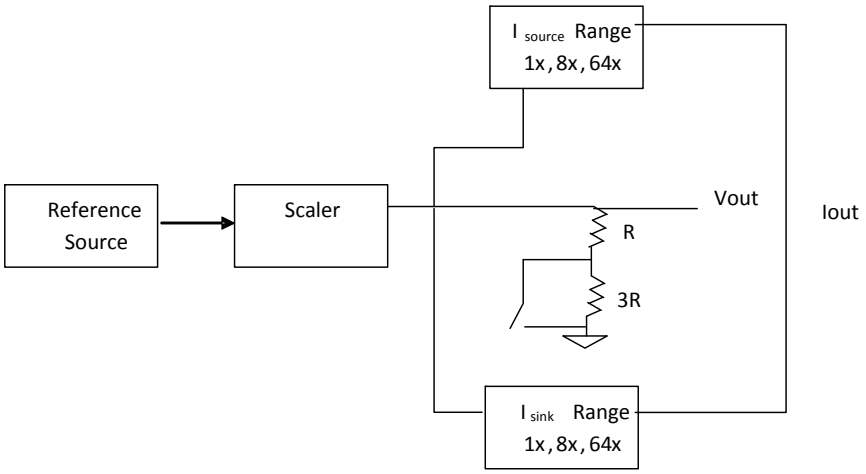
Die temperature is used to establish programming parameters for writing flash. Die temperature is measured using a dedicated sensor based on a forward biased transistor. The temperature sensor has its own auxiliary ADC.

8.9 DAC

The CY8C38 parts contain up to four Digital to Analog Convertors (DACs). Each DAC is 8-bit and can be configured for either voltage or current output. The DACs support CapSense, power supply regulation, and waveform generation. Each DAC has the following features:

- Adjustable voltage or current output in 255 steps
- Programmable step size (range selection)
- Eight bits of calibration to correct ± 25 percent of gain error
- Source and sink option for current output
- 8 Msps conversion rate for current output
- 1 Msps conversion rate for voltage output
- Monotonic in nature
- Data and strobe inputs can be provided by the CPU or DMA, or routed directly from the DSI
- Dedicated low-resistance output pin for high-current mode

Figure 8-12. DAC Block Diagram



8.9.1 Current DAC

The current DAC (IDAC) can be configured for the ranges 0 to 32 µA, 0 to 256 µA, and 0 to 2.048 mA. The IDAC can be configured to source or sink current.

8.9.2 Voltage DAC

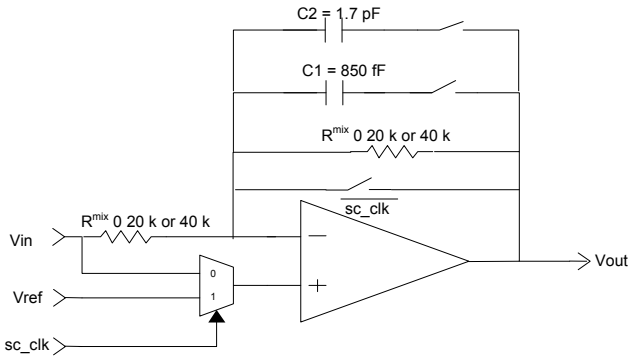
For the voltage DAC (VDAC), the current DAC output is routed through resistors. The two ranges available for the VDAC are 0 to 1.024 V and 0 to 4.096 V. In voltage mode any load connected to the output of a DAC should be purely capacitive (the output of the VDAC is not buffered).

8.10 Up/Down Mixer

In continuous time mode, the SC/CT block components are used to build an up or down mixer. Any mixing application contains an input signal frequency and a local oscillator frequency. The polarity of the clock, Fclk, switches the amplifier between inverting or noninverting gain. The output is the product of the input and the switching function from the local oscillator, with frequency components at the local oscillator plus and minus the signal frequency (Fclk + Fin and Fclk – Fin) and reduced-level frequency components at odd integer multiples of the local oscillator frequency. The local oscillator frequency is provided by the selected clock source for the mixer.

Continuous time up and down mixing works for applications with input signals and local oscillator frequencies up to 1 MHz.

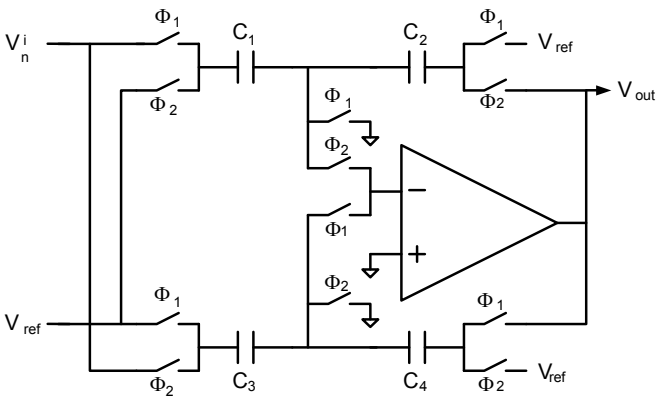
Figure 8-13. Mixer Configuration



8.11 Sample and Hold

The main application for a sample and hold, is to hold a value stable while an ADC is performing a conversion. Some applications require multiple signals to be sampled simultaneously, such as for power calculations (V and I).

Figure 8-14. Sample and Hold Topology (Φ1 and Φ2 are opposite phases of a clock)



8.11.1 Down Mixer

The SC/CT block can be used as a mixer to down convert an input signal. This circuit is a high bandwidth passive sample network that can sample input signals up to 14 MHz. This sampled value is then held using the opamp with a maximum clock rate of 4 MHz. The output frequency is at the difference between the input frequency and the highest integer multiple of the Local Oscillator that is less than the input.

8.11.2 First Order Modulator – SC Mode

A first order modulator is constructed by placing the SC/CT block in an integrator mode and using a comparator to provide a 1-bit feedback to the input. Depending on this bit, a reference voltage is either subtracted or added to the input signal. The block output is the output of the comparator and not the integrator in the modulator case. The signal is downshifted and buffered and then processed by a decimator to make a delta-sigma converter or a counter to make an incremental converter. The accuracy of the sampled data from the first-order modulator is determined from several factors.

The main application for this modulator is for a low-frequency ADC with high accuracy. Applications include strain gauges, thermocouples, precision voltage, and current measurement.

9. Programming, Debug Interfaces, Resources

PSoC devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware. Three interfaces are available: JTAG, SWD, and SWV. JTAG and SWD support all programming and debug features of the device. JTAG also supports standard JTAG scan chains for board level test and chaining multiple JTAG devices to a single JTAG connection.

Complete Debug on Chip (DoC) functionality enables full device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE software provides fully integrated programming and debug support for PSoC devices. The low cost MiniProg3 programmer and debugger is designed to provide full programming and debug support of PSoC devices in conjunction with the PSoC Creator IDE. PSoC JTAG, SWD, and SWV interfaces are fully compatible with industry standard third party tools.

All DOC circuits are disabled by default and can only be enabled in firmware. If not enabled, the only way to reenable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables DOC. Disabling DOC features, robust flash protection, and hiding custom analog and digital functionality inside the PSoC device provide a level of security not possible with multichip application solutions. Additionally, all device interfaces can be permanently disabled (Device Security) for applications concerned about phishing attacks due to a maliciously reprogrammed device. Permanently disabling interfaces is not recommended in most applications because you cannot access the device later. Because all programming, debug, and test interfaces are disabled when device security is enabled, PSoCs with Device Security enabled may not be returned for failure analysis.

Table 9-1. Debug Configurations

Debug and Trace Configuration	GPIO Pins Used
All debug and trace disabled	0
JTAG	4 or 5
SWD	2
SWV	1
SWD + SWV	3

9.1 JTAG Interface

The IEEE 1149.1 compliant JTAG interface exists on four or five pins (the nTRST pin is optional). The JTAG clock frequency can be up to 8 MHz, or 1/3 of the CPU clock frequency for 8 and 16-bit transfers, or 1/5 of the CPU clock frequency for 32-bit transfers, whichever is least. By default, the JTAG pins are enabled on new devices but the JTAG interface can be disabled, allowing these pins to be used as General Purpose I/O (GPIO) instead. The JTAG interface is used for programming the flash memory, debugging, I/O scan chains, and JTAG device chaining.

9.2 Serial Wire Debug Interface

The SWD interface is the preferred alternative to the JTAG interface. It requires only two pins instead of the four or five needed by JTAG. SWD provides all of the programming and debugging features of JTAG at the same speed. SWD does not provide access to scan chains or device chaining. The SWD clock frequency can be up to 1/3 of the CPU clock frequency.

SWD uses two pins, either two of the JTAG pins (TMS and TCK) or the USBIO D+ and D– pins. The USBIO pins are useful for in system programming of USB solutions that would otherwise require a separate programming connector. One pin is used for the data clock and the other is used for data input and output. SWD can be enabled on only one of the pin pairs at a time. This only happens if, within 8 µs (key window) after reset, that pin pair (JTAG or USB) receives a predetermined sequence of 1s and 0s. SWD is used for debugging or for programming the flash memory.

The SWD interface can be enabled from the JTAG interface or disabled, allowing its pins to be used as GPIO. Unlike JTAG, the SWD interface can always be reacquired on any device during the key window. It can then be used to reenable the JTAG interface, if desired. When using SWD or JTAG pins as standard GPIO, make sure that the GPIO functionality and PCB circuits do not interfere with SWD or JTAG use.

Table 11-2. DC Specifications *(continued)*

Parameter	Description	Conditions		Min	Typ	Max	Units
	Sleep Mode[22]						
	CPU = OFF RTC = ON (= ECO32K ON, in low-power mode) Sleep timer = ON (= ILO ON at 1 kHz)[23] WDT = OFF I^2C Wake = OFF Comparator = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 4.5–5.5 V	T = –40 °C	–	–	–	µA
			T = 25 °C	–	–	–	µA
			T = 85 °C	–	–	–	µA
		$V_{DD} = V_{DDIO}$ = 2.7–3.6 V	T = –40 °C	–	–	–	µA
			T = 25 °C	–	1	–	µA
			T = 85 °C	–	–	–	µA
		$V_{DD} = V_{DDIO}$ = 1.71–1.95 V	T = –40 °C	–	–	–	µA
			T = 25 °C	–	–	–	µA
			T = 85 °C	–	–	–	µA
	Comparator = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF I2C Wake = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 2.7–3.6V	T = 25 °C	–	–	–	µA
	I2C Wake = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF Comparator = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 2.7–3.6V	T = 25 °C	–	–	–	µA
	Hibernate Mode[22]						
	Hibernate mode current All regulators and oscillators off. SRAM retention GPIO interrupts are active Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 4.5–5.5 V	T = –40 °C	–	–	–	nA
			T = 25 °C	–	–	–	nA
			T = 85 °C	–	–	–	nA
		$V_{DD} = V_{DDIO}$ = 2.7–3.6 V	T = –40 °C	–	–	–	nA
			T = 25 °C	–	200	–	nA
			T = 85 °C	–	–	–	nA
		$V_{DD} = V_{DDIO}$ = 1.71–1.95 V	T = –40 °C	–	–	–	nA
			T = 25 °C	–	–	–	nA
			T = 85 °C	–	–	–	nA

Notes
22. If V_{CCD} and V_{CCA} are externally regulated, the voltage difference between V_{CCD} and V_{CCA} must be less than 50 mV.
23. Sleep timer generates periodic interrupts to wake up the CPU. This specification applies only to those times that the CPU is off.

11.4.2 SIO

Table 11-11. SIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vinmax	Maximum input voltage	All allowed values of Vddio and Vddd, see *Section 11.2.1*	–	–	5.5	V
Vinref	Input voltage reference (Differential input mode)		0.5	–	$0.52 \times V_{DDIO}$	V
Voutref	Output voltage reference (Regulated output mode)					
		$V_{DDIO} > 3.7$	1	–	$V_{DDIO} - 1$	V
		$V_{DDIO} < 3.7$	1	–	$V_{DDIO} - 0.5$	V
V_{IH}	Input voltage high threshold					
	GPIO mode	CMOS input	$0.7 \times V_{DDIO}$	–	–	V
	Differential input mode[30]	Hysteresis disabled	SIO_ref + 0.2	–	–	V
V_{IL}	Input voltage low threshold					
	GPIO mode	CMOS input	–	–	$0.3 \times V_{DDIO}$	V
	Differential input mode[30]	Hysteresis disabled	–	–	SIO_ref – 0.2	V
V_{OH}	Output voltage high					
	Unregulated mode	I_{OH} = 4 mA, V_{DDIO} = 3.3 V	$V_{DDIO} - 0.4$	–	–	V
	Regulated mode[30]	I_{OH} = 1 mA	SIO_ref – 0.65	–	SIO_ref + 0.2	V
	Regulated mode[30]	I_{OH} = 0.1 mA	SIO_ref – 0.3	–	SIO_ref + 0.2	V
V_{OL}	Output voltage low					
		V_{DDIO} = 3.30 V, I_{OL} = 25 mA	–	–	0.8	V
		V_{DDIO} = 1.80 V, I_{OL} = 4 mA	–	–	0.4	V
Rpullup	Pull-up resistor		3.5	5.6	8.5	kΩ
Rpulldown	Pull-down resistor		3.5	5.6	8.5	kΩ
I_{IL}	Input leakage current (Absolute value)[31]					
	$V_{IH} \leq$ Vddsio	25 °C, Vddsio = 3.0 V, V_{IH} = 3.0 V	–	–	14	nA
	V_{IH} > Vddsio	25 °C, Vddsio = 0 V, V_{IH} = 3.0 V	–	–	10	µA
C_{IN}	Input Capacitance[31]		–	–	7	pF
V_H	Input voltage hysteresis (Schmitt-Trigger)[31]	Single ended mode (GPIO mode)	–	40	–	mV
		Differential mode	–	35	–	mV
Idiode	Current through protection diode to V_{SSIO}		–	–	100	µA

Table 11-12. SIO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
TriseF	Rise time in fast strong mode (90/10%)[31]	Cload = 25 pF, V_{DDIO} = 3.3 V	–	–	12	ns
TfallF	Fall time in fast strong mode (90/10%)[31]	Cload = 25 pF, V_{DDIO} = 3.3 V	–	–	12	ns
TriseS	Rise time in slow strong mode (90/10%)[31]	Cload = 25 pF, V_{DDIO} = 3.0 V	–	–	75	ns
TfallS	Fall time in slow strong mode (90/10%)[31]	Cload = 25 pF, V_{DDIO} = 3.0 V	–	–	60	ns

Notes
30. See Figure 6-9 on page 30 and Figure 6-12 on page 33 for more information on SIO reference.
31. Based on device characterization (Not production tested).

Table 11-22. Delta-sigma ADC Sample Rates, Range = ±1.024 V

Resolution, Bits	Continuous		Multi-Sample		Multi-Sample Turbo	
	Min	Max	Min	Max	Min	Max
8	8000	384000	1911	91701	1829	87771
9	6400	307200	1543	74024	1489	71441
10	5566	267130	1348	64673	1307	62693
11	4741	227555	1154	55351	1123	53894
12	4000	192000	978	46900	956	45850
13	3283	157538	806	38641	791	37925
14	2783	133565	685	32855	674	32336
15	2371	113777	585	28054	577	27675
16	2000	48000	495	11861	489	11725
17	500	12000	124	2965	282	6766
18	125	3000	31	741	105	2513
19	16	375	4	93	15	357
20	8	187.5	2	46	8	183

Figure 11-17. Delta-sigma ADC I_{DD} vs sps, Range = ±1.024 V

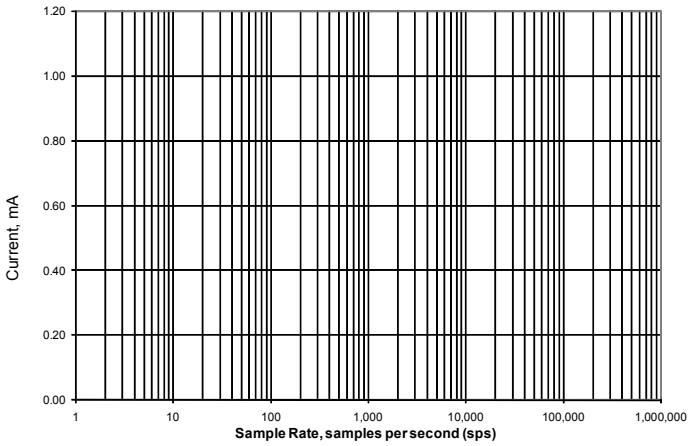
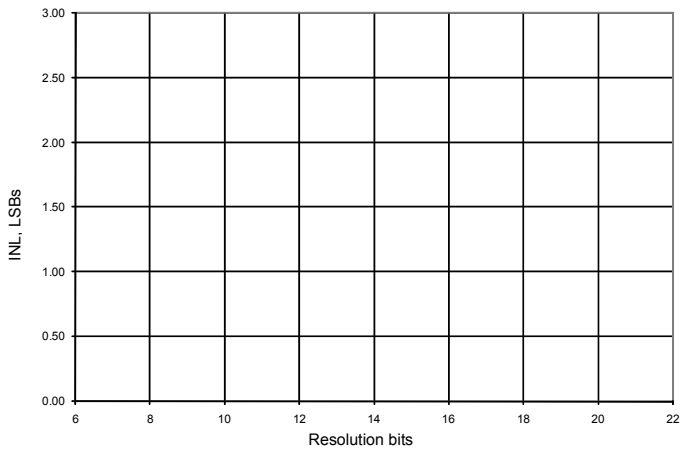


Figure 11-18. Delta-sigma ADC INL at Maximum Sample Rate



11.5.3 Voltage Reference

Table 11-25. Voltage Reference Specifications

See also ADC external reference specifications in *Section 11.5.2*.

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{REF}	Precision reference voltage	Initial trimming	1.023 (–0.1%)	1.024	1.025 (+0.1%)	V
	Temperature drift[36]		–	–	20	ppm/°C
	Long term drift		–	100	–	ppm/Khr
	Thermal cycling drift (stability)[36]		–	100	–	ppm

11.5.4 Analog Globals

Table 11-26. Analog Globals Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Rppag	Resistance pin-to-pin through analog global[37]	V_{DDA} = 3.0 V	–	939	1461	Ω
Rppmuxbus	Resistance pin-to-pin through analog mux bus[37]	V_{DDA} = 3.0 V	–	721	1135	Ω

11.5.5 Comparator

Table 11-27. Comparator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OS}	Input offset voltage in fast mode	Factory trim, Vdda > 2.7 V, Vin ≥ 0.5 V	–		10	mV
	Input offset voltage in slow mode	Factory trim, Vin ≥ 0.5 V	–		9	mV
V_{OS}	Input offset voltage in fast mode[38]	Custom trim	–	–	4	mV
	Input offset voltage in slow mode[38]	Custom trim	–	–	4	mV
V_{OS}	Input offset voltage in ultra low-power mode		–	±12	–	mV
V_{HYST}	Hysteresis	Hysteresis enable mode	–	10	32	mV
V_{ICM}	Input common mode voltage	High current / fast mode	V_{SSA}	–	V_{DDA} – 0.1	V
		Low current / slow mode	V_{SSA}	–	V_{DDA}	V
		Ultra low power mode	V_{SSA}	–	V_{DDA} – 0.9	V
CMRR	Common mode rejection ratio		–	50	–	dB
I_{CMP}	High current mode/fast mode[36]		–	–	400	µA
	Low current mode/slow mode[36]		–	–	100	µA
	Ultra low-power mode[36]		–	6	–	µA

Notes
36. Based on device characterization (Not production tested).
37. The resistance of the analog global and analog mux bus is high if $V_{DDA} \leq 2.7$ V, and the chip is in either sleep or hibernate mode. Use of analog global and analog mux bus under these conditions is not recommended.
38. The recommended procedure for using a custom trim value for the on-chip comparators can be found in the TRM.

11.5.12 LCD Direct Drive

Table 11-40. LCD Direct Drive DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{CC}	LCD system operating current	Device sleep mode with wakeup at 400-Hz rate to refresh LCDs, bus clock = 3 Mhz, Vddio = Vdda = 3 V, 4 commons, 16 segments, 1/4 duty cycle, 50 Hz frame rate, no glass connected	–	38	–	µA
I_{CC_SEG}	Current per segment driver	Strong drive mode	–	260	–	µA
V_{BIAS}	LCD bias range (V_{BIAS} refers to the main output voltage(V0) of LCD DAC)	$V_{DDA} \geq 3$ V and $V_{DDA} \geq V_{BIAS}$	2	–	5	V
	LCD bias step size	$V_{DDA} \geq 3$ V and $V_{DDA} \geq V_{BIAS}$	–	$9.1 \times V_{DDA}$	–	mV
	LCD capacitance per segment/common driver	Drivers may be combined	–	500	5000	pF
	Long term segment offset		–	–	20	mV
I_{OUT}	Output drive current per segment driver)	Vddio = 5.5V, strong drive mode	355	–	710	µA

Table 11-41. LCD Direct Drive AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
f_{LCD}	LCD frame rate		10	50	150	Hz

12. Ordering Information

In addition to the features listed in Table 12-1, every CY8C38 device includes: a precision on-chip voltage reference, precision oscillators, flash, ECC, DMA, a fixed function I²C, 4 KB trace RAM, JTAG/SWD programming and debug, external memory interface, and more. In addition to these features, the flexible UDBs and analog subsection support a wide range of peripherals. To assist you in selecting the ideal part, PSoC Creator makes a part recommendation after you choose the components required by your application. All CY8C38 derivatives incorporate device and flash security in user-selectable security levels; see the TRM for details.

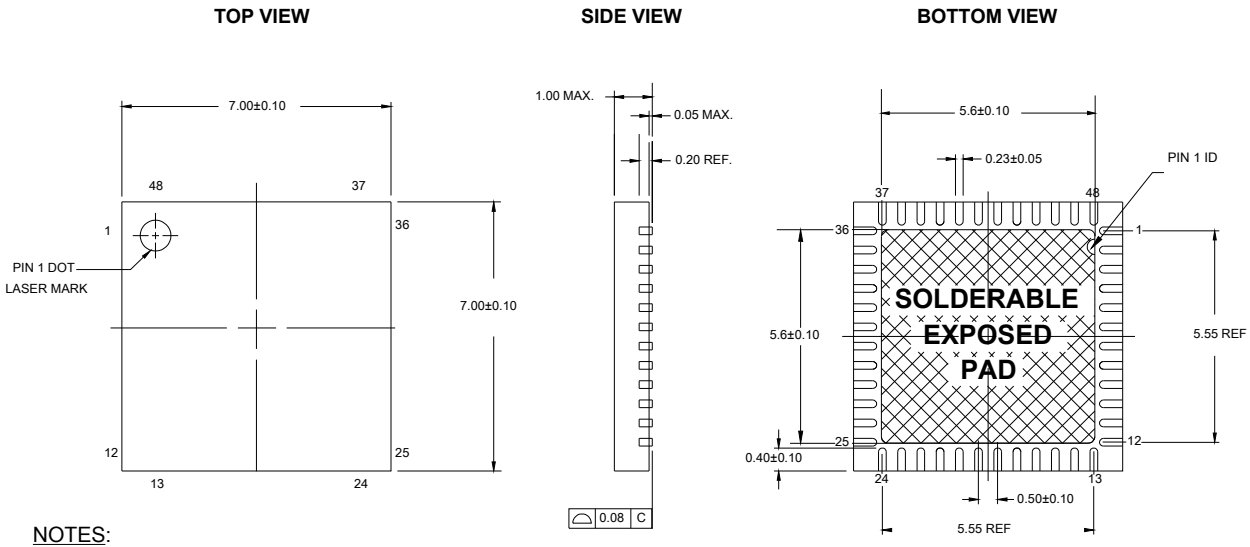
Table 12-1. CY8C38 Family with Single Cycle 8051

Part Number	MCU Core				Analog								Digital				I/O[56]				Package	JTAG ID[57]
	CPU Speed (MHz)	Flash (KB)	SRAM (KB)	EEPROM (KB)	LCD Segment Drive	ADC	DAC	Comparator	SC/CT Analog Blocks[54]	Opamps	DFB	CapSense	UDBs[55]	16-bit Timer/PWM	FS USB	CAN 2.0b	Total I/O	GPIO	SIO	USBIO		
32 KB Flash																						
CY8C3865AXI-056	67	32	4	1	–	20-bit Del-Sig	4	4	4	4	✔	✔	20	4	–	–	70	62	8	0	100-pin TQFP	0×0E038069
CY8C3865LTI-045	67	32	4	1	–	20-bit Del-Sig	4	4	4	4	✔	✔	20	4	–	–	46	38	8	0	68-pin QFN	0×0E02D069
CY8C3865LTI-058	67	32	4	1	–	20-bit Del-Sig	4	4	4	2	✔	✔	20	4	–	–	29	25	4	0	48-pin QFN	0×0E03A069
CY8C3865PVI-051	67	32	4	1	–	20-bit Del-Sig	4	4	4	2	✔	✔	20	4	–	–	29	25	4	0	48-pin SSOP	0×0E033069
CY8C3865AXI-015	67	32	4	1	–	20-bit Del-Sig	4	4	4	4	✔	✔	20	4	✔	–	72	62	8	2	100-pin TQFP	0×0E00F069
CY8C3865LTI-032	67	32	4	1	–	20-bit Del-Sig	4	4	4	4	✔	✔	20	4	✔	–	48	38	8	2	68-pin QFN	0×0E020069
CY8C3865LTI-061	67	32	4	1	–	20-bit Del-Sig	4	4	4	2	✔	✔	20	4	✔	–	31	25	4	2	48-pin QFN	0×0E03D069
CY8C3865PVI-053	67	32	4	1	–	20-bit Del-Sig	4	4	4	2	✔	✔	20	4	✔	–	31	25	4	2	48-pin SSOP	0×0E035069
CY8C3865AXI-018	67	32	4	1	✔	20-bit Del-Sig	4	4	4	4	✔	✔	20	4	–	–	70	62	8	0	100-pin TQFP	0×0E012069
CY8C3865LTI-024	67	32	4	1	✔	20-bit Del-Sig	4	4	4	4	✔	✔	20	4	–	–	46	38	8	0	68-pin QFN	0×0E018069
CY8C3865LTI-059	67	32	4	1	✔	20-bit Del-Sig	4	4	4	2	✔	✔	20	4	–	–	29	25	4	0	48-pin QFN	0×0E03B069
CY8C3865PVI-060	67	32	4	1	✔	20-bit Del-Sig	4	4	4	2	✔	✔	20	4	–	–	29	25	4	0	48-pin SSOP	0×0E03C069
CY8C3865AXI-019	67	32	4	1	✔	20-bit Del-Sig	4	4	4	4	✔	✔	20	4	✔	–	72	62	8	2	100-pin TQFP	0×0E013069
CY8C3865LTI-014	67	32	4	1	✔	20-bit Del-Sig	4	4	4	4	✔	✔	20	4	✔	–	48	38	8	2	68-pin QFN	0×0E00E069
CY8C3865LTI-062	67	32	4	1	✔	20-bit Del-Sig	4	4	4	2	✔	✔	20	4	✔	–	31	25	4	2	48-pin QFN	0×0E03E069
CY8C3865PVI-063	67	32	4	1	✔	20-bit Del-Sig	4	4	4	2	✔	✔	20	4	✔	–	31	25	4	2	48-pin SSOP	0×0E03F069
64 KB Flash																						
CY8C3866AXI-054	67	64	8	2	–	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	–	–	70	62	8	0	100-pin TQFP	0×0E036069
CY8C3866LTI-020	67	64	8	2	–	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	–	–	46	38	8	0	68-pin QFN	0×0E014069
CY8C3866LTI-064	67	64	8	2	–	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	–	–	29	25	4	0	48-pin QFN	0×0E040069
CY8C3866PVI-005	67	64	8	2	–	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	–	–	29	25	4	0	48-pin SSOP	0×0E005069
CY8C3866AXI-033	67	64	8	2	–	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	✔	–	72	62	8	2	100-pin TQFP	0×0E021069
CY8C3866LTI-023	67	64	8	2	–	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	✔	–	48	38	8	2	68-pin QFN	0×0E017069
CY8C3866LTI-067	67	64	8	2	–	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	✔	–	31	25	4	2	48-pin QFN	0×0E043069
CY8C3866PVI-021	67	64	8	2	–	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	✔	–	31	25	4	2	48-pin SSOP	0×0E015069
CY8C3866AXI-038	67	64	8	2	✔	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	–	–	70	62	8	0	100-pin TQFP	0×0E026069
CY8C3866LTI-029	67	64	8	2	✔	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	–	–	46	38	8	0	68-pin QFN	0×0E01D069
CY8C3866LTI-065	67	64	8	2	✔	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	–	–	29	25	4	0	48-pin QFN	0×0E041069
CY8C3866PVI-066	67	64	8	2	✔	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	–	–	29	25	4	0	48-pin SSOP	0×0E042069

Notes

54. Analog blocks support a variety of functionality including TIA, PGA, and mixers. See the Example Peripherals on page 35 for more information on how analog blocks can be used.
55. UDBs support a variety of functionality including SPI, LIN, UART, timer, counter, PWM, PRS, and others. Individual functions may use a fraction of a UDB or multiple UDBs. Multiple functions can share a single UDB. See the Example Peripherals on page 35 for more information on how UDBs can be used.
56. The I/O Count includes all types of digital I/O: GPIO, SIO, and the two USB I/O. See the I/O System and Routing on page 28 for details on the functionality of each of these types of I/O.
57. The JTAG ID has three major fields. The most significant nibble (left digit) is the version, followed by a 2 byte part number and a 3 nibble manufacturer ID.

Figure 13-2. 48-pin QFN Package Outline



NOTES:

HATCH AREA IS SOLDERABLE EXPOSED METAL.

2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.13g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LT48D	LEAD FREE

001- 45616 *B

Description Title: PSoC® 3: CY8C38 Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-11729				
*K	2903576	04/01/2010	MKEA	Updated Vb pin in PCB Schematic. Updated Tstartup parameter in AC Specifications table. Added Load regulation and Line regulation parameters to Inductive Boost Regulator DC Specifications table. Updated I_{CC} parameter in LCD Direct Drive DC Specs table. In page 1, updated internal oscillator range under Precision programmable clocking to start from 3 MHz. Updated I_{OUT} parameter in LCD Direct Drive DC Specs table. Updated Table 6-2 and Table 6-3. Added bullets on CapSense in page 1; added CapSense column in Section 12. Removed some references to footnote [1]. Changed INC_Rn cycles from 3 to 2 (Table 4-1). Added footnote in PLL AC Specification table. Added PLL intermediate frequency row with footnote in PLL AC Specs table. Added UDBs subsection under 11.6 Digital Peripherals. Updated Figure 2-6 (PCB Layout). Updated Pin Descriptions section and modified Figures 6-6, 6-8, 6-9. Updated LVD in Tables 6-2 and 6-3; modified Low-power modes bullet in page 1. Added note to Figures 2-5 and 6-2; Updated Figure 6-2 to add capacitors for V_{DDA} and V_{DDD} pins. Updated boost converter section (6.2.2). Updated Tstartup values in Table 11-3. Removed IPOR rows from Table 11-68. Updated 6.3.1.1, Power Voltage Level Monitors. Updated section 5.2 and Table 11-2 to correct suggestion of execution from flash. Updated V_{REF} specs in Table 11-21. Updated IDAC uncompensated gain error in Table 11-25. Updated Delay from Interrupt signal input to ISR code execution from ISR code in Table11-72. Removed other line in table. Added sentence to last paragraph of section 6.1.1.3. Updated T_{RESP}, high and low-power modes, in Table 11-24. Updated f_TCK values in Table 11-73 and f_SWDCK values in Table 11-74. Updated SNR condition in Table 11-20. Corrected unit of measurement in Table 11-21. Updated sleep wakeup time in Table 6-3 and Tsleep in Table 11-3. Added 1.71 V <= V_{DDD} < 3.3 V, SWD over USBIO pins value to Table 11-74. Removed mention of hibernate reset (HRES) from page 1 features, Table 6-3, Section 6.2.1.4, Section 6.3, and Section 6.3.1.1. Changed PPOR/PRES to TBDs in Section 6.3.1.1, Section 6.4.1.6 (changed PPOR to reset), Table 11-3 (changed PPOR to PRES), Table 11-68 (changed title, values TBD), and Table 11-69 (changed PPOR_TR to PRES_TR). Added sentence saying that LVD circuits can generate a reset to Section 6.3.1.1. Changed I_{DD} values on page 1, page 5, and Table 11-2. Changed resume time value in Section 6.2.1.3. Changed ESD HBM value in Table 11-1. Changed SNR in 16-bit resolution mode value and sample rate row in Table 11-20. Removed V_{DDA} = 1.65 V rows and changed BWag value in Table 11-22. Changed V_{IOFF} values and changed CMRR value in Table 11-23. Changed INL max value in Table 11-27. Added max value to the Quiescent current specs in Tables 11-29 and 11-31. Changed occurrences of “Block” to “Row” and deleted the “ECC not included” footnote in Table 11-57. Changed max response time value in Tables 11-69 and 11-71. Changed the Startup time in Table 11-79. Added condition to intermediate frequency row in Table 11-85. Added row to Table 11-69. Added brown out note to Section 11.8.1.

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*Q	3179219	02/22/2011	MKEA	Updated conditions for flash data retention time Updated 100-pin TQFP package spec. Updated EEPROM AC specifications.

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