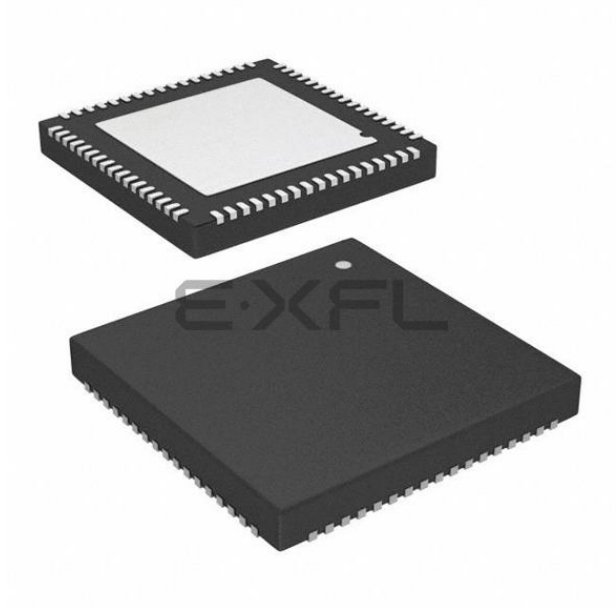

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x20b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3866lti-029

Figure 2-4. 100-pin TQFP Part Pinout

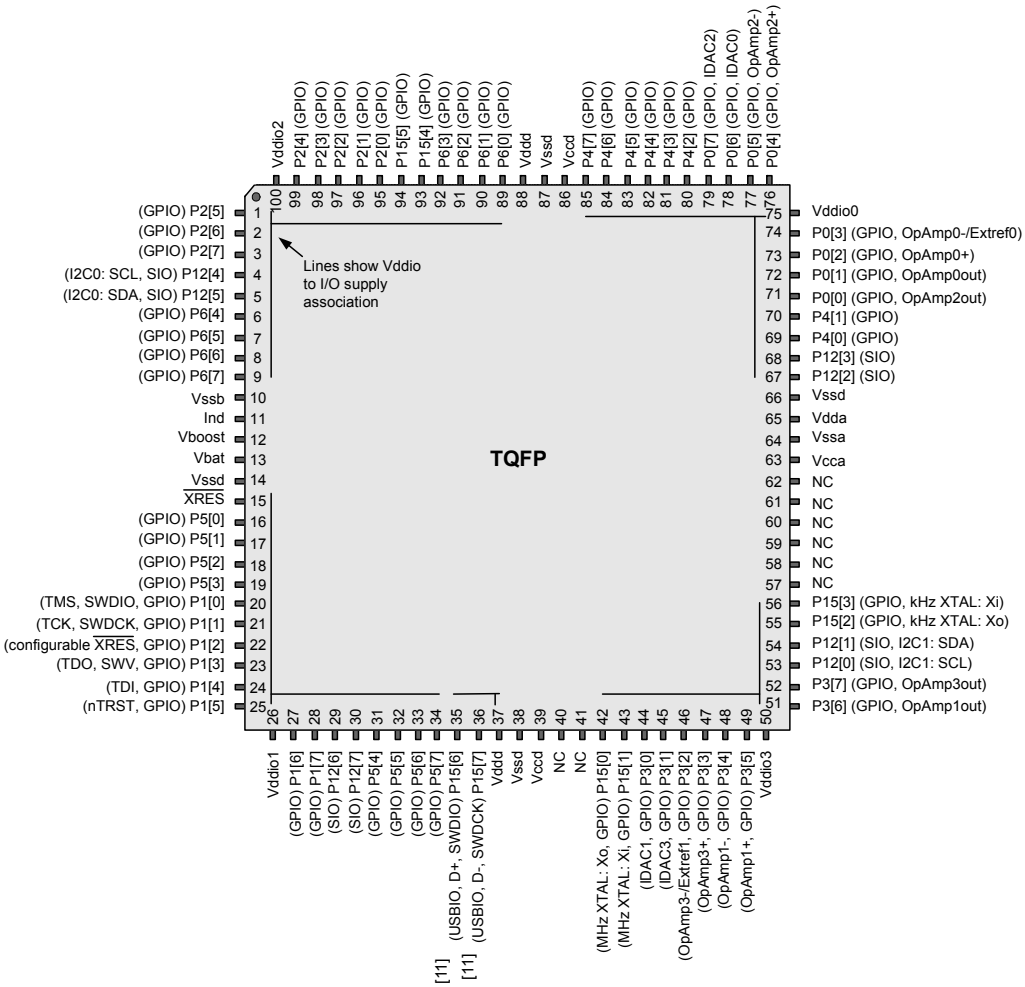
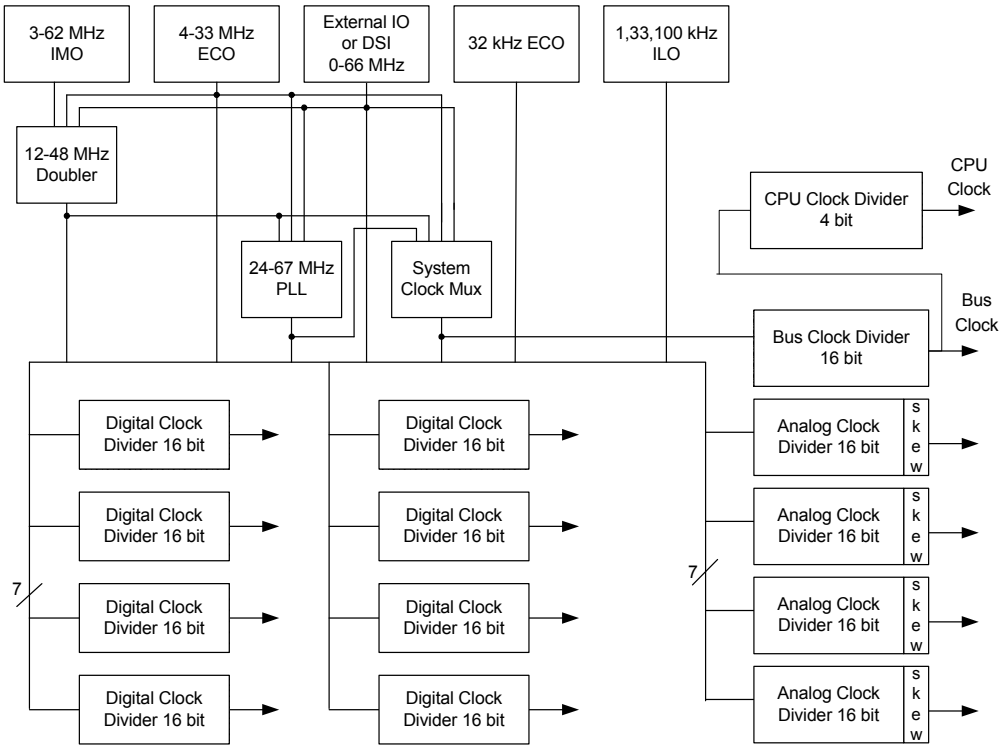


Figure 2-5 and Figure 2-6 show an example schematic and an example PCB layout, for the 100-pin TQFP part, for optimal analog performance on a two-layer board.

- The two pins labeled Vddd must be connected together.
- The two pins labeled Vccd must be connected together, with capacitance added, as shown in Figure 2-5 and Power System on page 24. The trace between the two Vccd pins should be as short as possible.
- The two pins labeled Vssd must be connected together.

Note
11. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.

Figure 6-1. Clocking Subsystem



6.1.1 Internal Oscillators

6.1.1.1 Internal Main Oscillator

In most designs the IMO is the only clock source required, due to its ±1-percent accuracy. The IMO operates with no external components and outputs a stable clock. A factory trim for each frequency range is stored in the device. With the factory trim, tolerance varies from ±1 percent at 3 MHz, up to ±7 percent at 62 MHz. The IMO, in conjunction with the PLL, allows generation of CPU and system clocks up to the device's maximum frequency (see PLL). The IMO provides clock outputs at 3, 6, 12, 24, 48, and 62 MHz.

6.1.1.2 Clock Doubler

The clock doubler outputs a clock at twice the frequency of the input clock. The doubler works for input frequency ranges of 6 to 24 MHz (providing 12 to 48 MHz at the output). It can be configured to use a clock from the IMO, MHzECO, or the DSI (external pin). The doubler is typically used to clock the USB.

6.1.1.3 PLL

The PLL allows low-frequency, high-accuracy clocks to be multiplied to higher frequencies. This is a trade off between higher clock frequency and accuracy and, higher power consumption and increased startup time.

The PLL block provides a mechanism for generating clock frequencies based upon a variety of input sources. The PLL outputs clock frequencies in the range of 24 to 67 MHz. Its input and feedback dividers supply 4032 discrete ratios to create almost any desired system clock frequency. The accuracy of the PLL output depends on the accuracy of the PLL input source. The most common PLL use is to multiply the IMO clock at 3 MHz, where it is most accurate, to generate the CPU and system clocks up to the device's maximum frequency.

The PLL achieves phase lock within 250 µs (verified by bit setting). It can be configured to use a clock from the IMO, MHzECO or DSI (external pin). The PLL clock source can be used until lock is complete and signaled with a lock bit. The lock signal can be routed through the DSI to generate an interrupt. Disable the PLL before entering low-power modes.

6.1.1.4 Internal Low-Speed Oscillator

The ILO provides clock frequencies for low-power consumption, including the watchdog timer, and sleep timer. The ILO generates up to three different clocks: 1 kHz, 33 kHz, and 100 kHz. The 1-kHz clock (CLK1K) is typically used for a background 'heartbeat' timer. This clock inherently lends itself to low-power supervisory operations such as the watchdog timer and long sleep intervals using the central timewheel (CTW).

The central timewheel is a 1-kHz, free running, 13-bit counter clocked by the ILO. The central timewheel is always enabled, except in hibernate mode and when the CPU is stopped during debug on chip mode. It can be used to generate periodic interrupts for timing purposes or to wake the system from a low-power mode. Firmware can reset the central timewheel. Systems that require accurate timing should use the RTC capability instead of the central timewheel.

The 100-kHz clock (CLK100K) works as a low-power system clock to run the CPU. It can also generate time intervals such as fast sleep intervals using the fast timewheel. The fast timewheel is a 100-kHz, 5-bit counter clocked by the ILO that can also be used to wake the system. The fast timewheel settings are programmable, and the counter automatically resets when the terminal count is reached. This enables flexible, periodic wakeups of the CPU at a higher rate than is allowed using the central timewheel. The fast timewheel can generate an optional interrupt each time the terminal count is reached.

- ALVI, DLVI, AHVI – Analog/digital low voltage interrupt, analog high voltage interrupt

  Interrupt circuits are available to detect when Vdda and Vddd go outside a voltage range. For AHVI, Vdda is compared to a fixed trip level. For ALVI and DLVI, Vdda and Vddd are compared to trip levels that are programmable, as listed in Table 6-5. ALVI and DLVI can also be configured to generate a device reset instead of an interrupt.

Table 6-5. Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt

Interrupt	Supply	Normal Voltage Range	Available Trip Settings	Accuracy
DLVI	V_{DDD}	1.71 V–5.5 V	1.70 V–5.45 V in 250 mV increments	±2%
ALVI	V_{DDA}	1.71 V–5.5 V	1.70 V–5.45 V in 250 mV increments	±2%
AHVI	V_{DDA}	1.71 V–5.5 V	5.75 V	±2%

The monitors are disabled until after IPOR. During sleep mode these circuits are periodically activated (buzzed). If an interrupt occurs during buzzing then the system first enters its wakeup sequence. The interrupt is then recognized and may be serviced.

6.3.1.2 Other Reset Sources

- XRES – External reset

  PSoC 3 has either a single GPIO pin that is configured as an external reset or a dedicated XRES pin. Either the dedicated XRES pin or the GPIO pin, if configured, holds the part in reset while held active (low). The response to an XRES is the same as to an IPOR reset.

  The external reset is active low. It includes an internal pull-up resistor. XRES is active during sleep and hibernate modes.

- SRES – Software reset

  A reset can be commanded under program control by setting a bit in the software reset register. This is done either directly by the program or indirectly by DMA access. The response to a SRES is the same as after an IPOR reset.

  Another register bit exists to disable this function.

- DRES – Digital logic reset

  A logic signal can be routed from the UDBs or other digital peripheral source through the DSI to the Configurable XRES pin, P1[2], to generate a hardware-controlled reset. The pin must be placed in XRES mode. The response to a DRES is the same as after an IPOR reset.

- WRES – Watchdog timer reset

  The watchdog reset detects when the software program is no longer being executed correctly. To indicate to the watchdog timer that it is running correctly, the program must periodically reset the timer. If the timer is not reset before a user-specified amount of time, then a reset is generated.

  Note IPOR disables the watchdog function. The program must enable the watchdog function at an appropriate point in the code by setting a register bit. When this bit is set, it cannot be cleared again except by an IPOR power on reset event.

6.4 I/O System and Routing

PSoC I/Os are extremely flexible. Every GPIO has analog and digital I/O capability. All I/Os have a large number of drive modes, which are set at POR. PSoC also provides up to four individual I/O voltage domains through the Vddio pins.

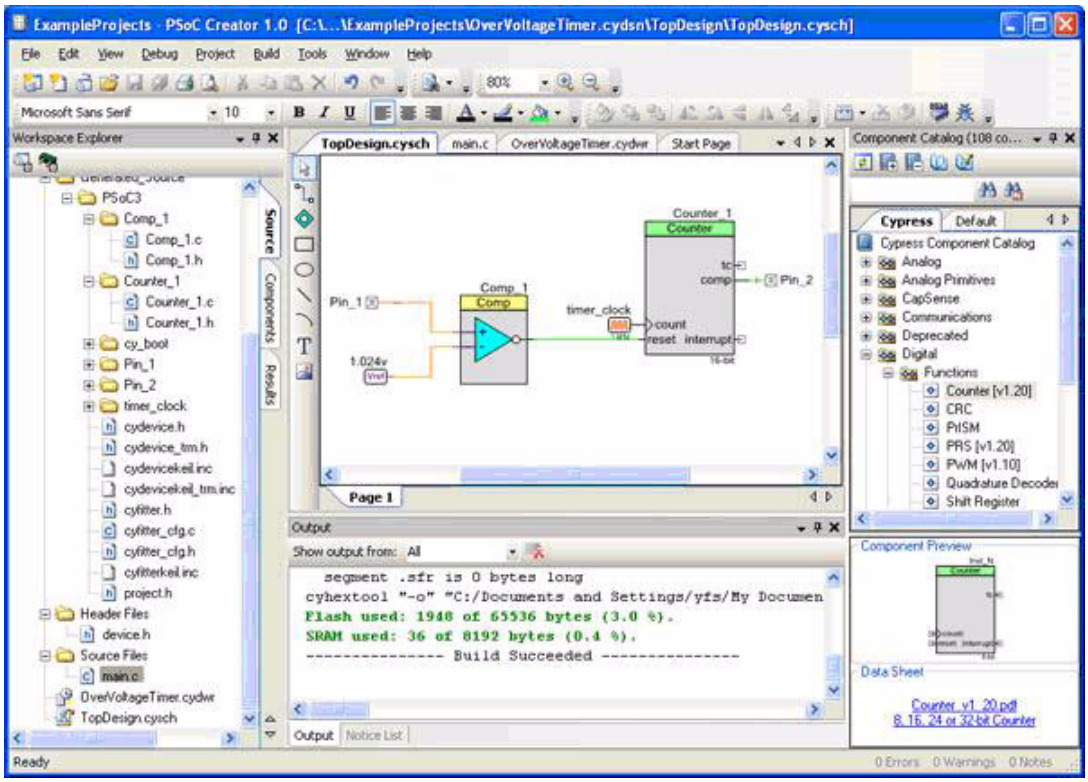
There are two types of I/O pins on every device; those with USB provide a third type. Both GPIO and SIO provide similar digital functionality. The primary differences are their analog capability and drive strength. Devices that include USB also provide two USBIO pins that support specific USB functionality as well as limited GPIO capability.

All I/O pins are available for use as digital inputs and outputs for both the CPU and digital peripherals. In addition, all I/O pins can generate an interrupt. The flexible and advanced capabilities of the PSoC I/O, combined with any signal to any pin routability, greatly simplify circuit design and board layout. All GPIO pins can be used for analog input, CapSense[14], and LCD segment drive, while SIO pins are used for voltages in excess of V_{DDA} and for programmable output voltages.

- Features supported by both GPIO and SIO:
  - User programmable port reset state
  - Separate I/O supplies and voltages for up to four groups of I/O
  - Digital peripherals use DSI to connect the pins
  - Input or output or both for CPU and DMA
  - Eight drive modes
  - Every pin can be an interrupt source configured as rising edge, falling edge or both edges. If required, level sensitive interrupts are supported through the DSI
  - Dedicated port interrupt vector for each port
  - Slew rate controlled digital output drive mode
  - Access port control and configuration registers on either port basis or pin basis
  - Separate port read (PS) and write (DR) data registers to avoid read modify write errors
  - Special functionality on a pin by pin basis
- Additional features only provided on the GPIO pins:
  - LCD segment drive on LCD equipped devices
  - CapSense[14]
  - Analog input and output capability
  - Continuous 100 µA clamp current capability
  - Standard drive strength down to 1.7 V
- Additional features only provided on SIO pins:
  - Higher drive strength than GPIO
  - Hot swap capability (5 V tolerance at any operating V_{DD})
  - Programmable and regulated high input and output drive levels down to 1.2 V
  - No analog input, CapSense, or LCD capability
  - Over voltage tolerance up to 5.5 V
  - SIO can act as a general purpose analog comparator
- USBIO features:
  - Full speed USB 2.0 compliant I/O
  - Highest drive strength for general purpose use
  - Input, output, or both for CPU and DMA
  - Input, output, or both for digital peripherals
  - Digital output (CMOS) drive mode
  - Each pin can be an interrupt source configured as rising edge, falling edge, or both edges

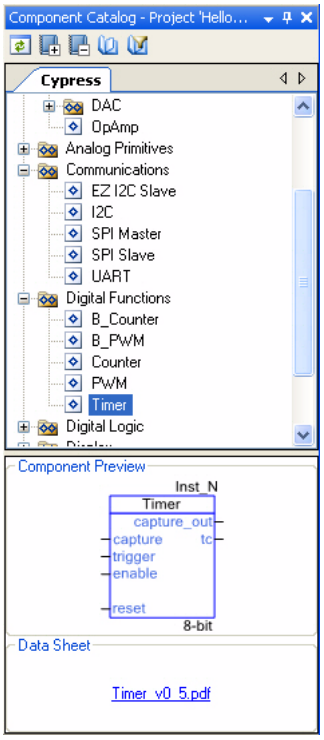
Note
14. GPIOs with opamp outputs are not recommended for use with CapSense.

Figure 7-2. PSoC Creator Framework



7.1.4.2 Component Catalog

Figure 7-3. Component Catalog



The component catalog is a repository of reusable design elements that select device functionality and customize your PSoC device. It is populated with an impressive selection of content; from simple primitives such as logic gates and device registers, through the digital timers, counters and PWMs, plus analog components such as ADC, DACs, and filters, and communication protocols, such as I^2C, USB, and CAN. See Example Peripherals on page 35 for more details about available peripherals. All content is fully characterized and carefully documented in datasheets with code examples, AC/DC specifications, and user code ready APIs.

7.1.4.3 Design Reuse

The symbol editor gives you the ability to develop reusable components that can significantly reduce future design time. Just draw a symbol and associate that symbol with your proven design. PSoC Creator allows for the placement of the new symbol anywhere in the component catalog along with the content provided by Cypress. You can then reuse your content as many times as you want, and in any number of projects, without ever having to revisit the details of the implementation.

Independent of the ALU operation, these functions are available:

- Shift left
- Shift right
- Nibble swap
- Bitwise OR mask

7.2.2.3 Conditionals

Each datapath has two compares, with bit masking options. Compare operands include the two accumulators and the two data registers in a variety of configurations. Other conditions include zero detect, all ones detect, and overflow. These conditions are the primary datapath outputs, a selection of which can be driven out to the UDB routing matrix. Conditional computation can use the built in chaining to neighboring UDBs to operate on wider data widths without the need to use routing resources.

7.2.2.4 Variable MSB

The most significant bit of an arithmetic and shift function can be programmatically specified. This supports variable width CRC and PRS functions, and in conjunction with ALU output masking, can implement arbitrary width timers, counters and shift blocks.

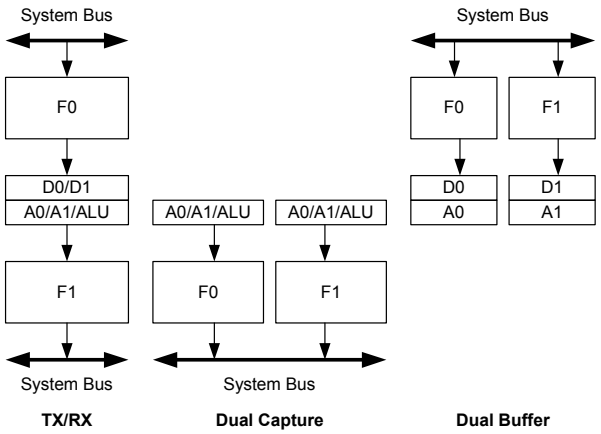
7.2.2.5 Built in CRC/PRS

The datapath has built-in support for single cycle CRC computation and PRS generation of arbitrary width and arbitrary polynomial. CRC/PRS functions longer than 8 bits may be implemented in conjunction with PLD logic, or built in chaining may be use to extend the function into neighboring UDBs.

7.2.2.6 Input/Output FIFOs

Each datapath contains two four-byte deep FIFOs, which can be independently configured as an input buffer (system bus writes to the FIFO, datapath internal reads the FIFO), or an output buffer (datapath internal writes to the FIFO, the system bus reads from the FIFO). The FIFOs generate status that are selectable as datapath outputs and can therefore be driven to the routing, to interact with sequencers, interrupts, or DMA.

Figure 7-9. Example FIFO Configurations



7.2.2.7 Chaining

The datapath can be configured to chain conditions and signals such as carries and shift data with neighboring datapaths to create higher precision arithmetic, shift, CRC/PRS functions.

7.2.2.8 Time Multiplexing

In applications that are over sampled, or do not need high clock rates, the single ALU block in the datapath can be efficiently shared with two sets of registers and condition generators. Carry and shift out data from the ALU are registered and can be selected as inputs in subsequent cycles. This provides support for 16-bit functions in one (8-bit) datapath.

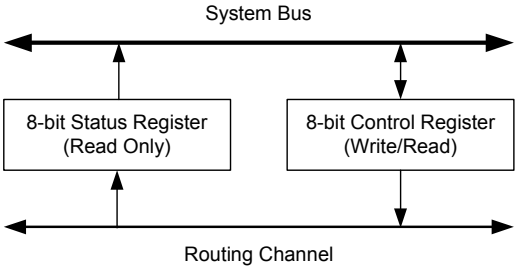
7.2.2.9 Datapath I/O

There are six inputs and six outputs that connect the datapath to the routing matrix. Inputs from the routing provide the configuration for the datapath operation to perform in each cycle, and the serial data inputs. Inputs can be routed from other UDB blocks, other device peripherals, device I/O pins, and so on. The outputs to the routing can be selected from the generated conditions, and the serial data outputs. Outputs can be routed to other UDB blocks, device peripherals, interrupt and DMA controller, I/O pins, and so on.

7.2.3 Status and Control Module

The primary purpose of this circuitry is to coordinate CPU firmware interaction with internal UDB operation.

Figure 7-10. Status and Control Registers

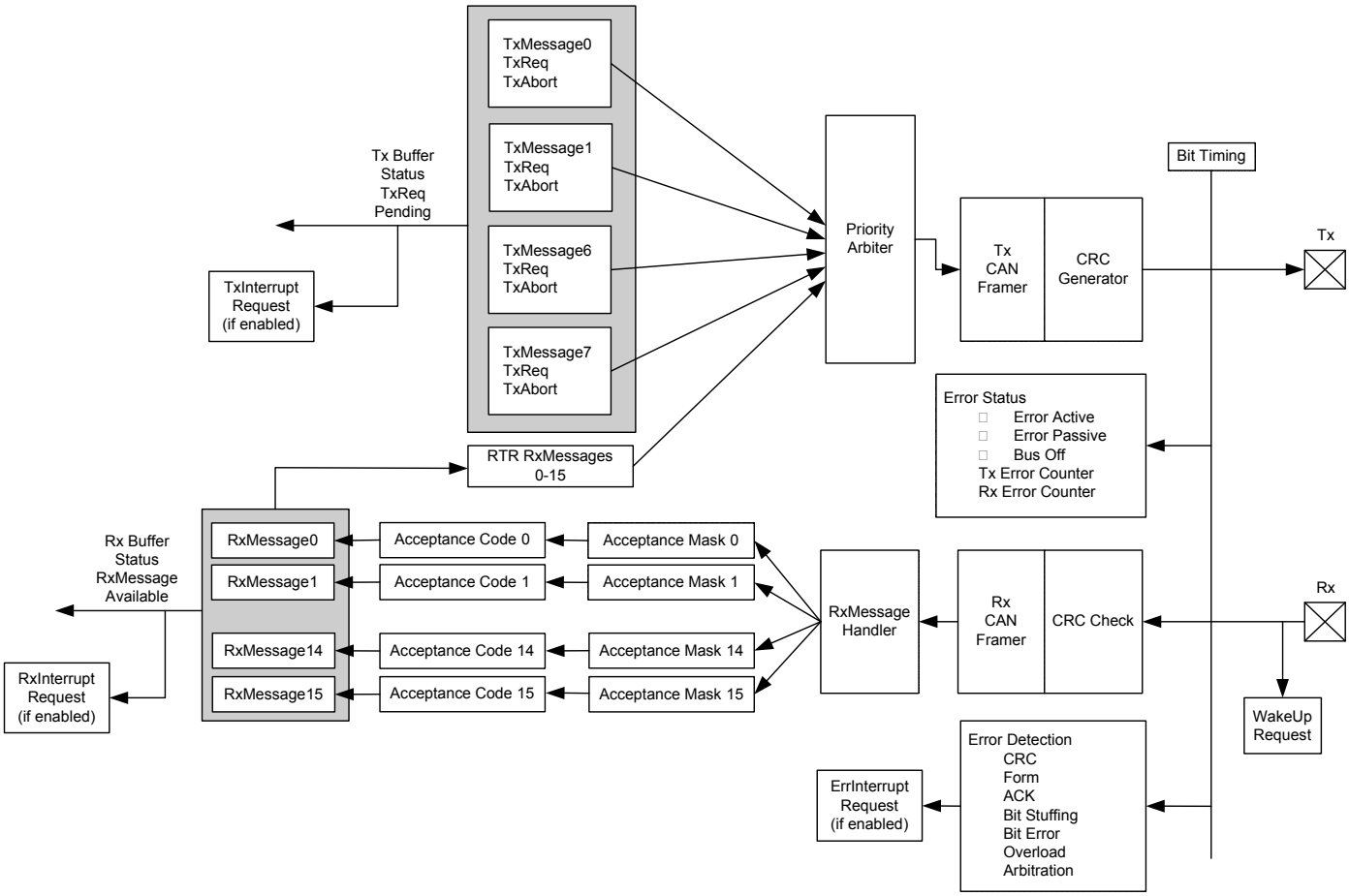


The bits of the control register, which may be written to by the system bus, are used to drive into the routing matrix, and thus provide firmware with the opportunity to control the state of UDB processing. The status register is read-only and it allows internal UDB state to be read out onto the system bus directly from internal routing. This allows firmware to monitor the state of UDB processing. Each bit of these registers has programmable connections to the routing matrix and routing connections are made depending on the requirements of the application.

7.2.3.1 Usage Examples

As an example of control input, a bit in the control register can be allocated as a function enable bit. There are multiple ways to enable a function. In one method the control bit output would be routed to the clock control block in one or more UDBs and serve as a clock enable for the selected UDB blocks. A status example is a case where a PLD or datapath block generated a condition, such as a “compare true” condition that is captured and latched by the status register and then read (and cleared) by CPU firmware.

Figure 7-19. CAN Controller Block Diagram



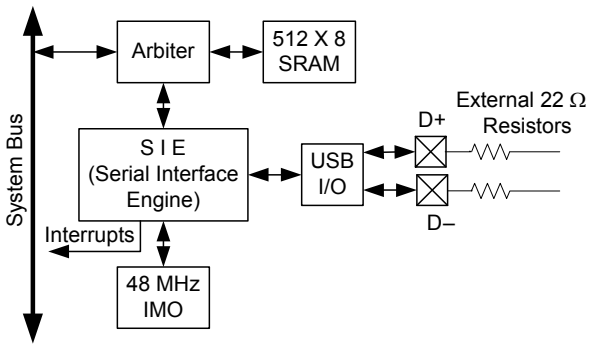
7.6 USB

PSoC includes a dedicated Full-Speed (12 Mbps) USB 2.0 transceiver supporting all four USB transfer types: control, interrupt, bulk, and isochronous. PSoC Creator provides full configuration support. USB interfaces to hosts through two dedicated USBIO pins, which are detailed in the "I/O System and Routing" section on page 28.

USB includes the following features:

- Eight unidirectional data endpoints
- One bidirectional control endpoint 0 (EP0)
- Shared 512-byte buffer for the eight data endpoints
- Dedicated 8-byte buffer for EP0
- Three memory modes
  - Manual memory management with no DMA access
  - Manual memory management with manual DMA access
  - Automatic memory management with automatic DMA access
- Internal 3.3-V regulator for transceiver
- Internal 48-MHz main oscillator mode that auto locks to USB bus clock, requiring no external crystal for USB (USB equipped parts only)
- Interrupts on bus and each endpoint event, with device wakeup
- USB reset, suspend, and resume operations
- Bus-powered and self-powered modes

Figure 7-20. USB



11.3 Power Regulators

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.3.1 Digital Core Regulator

Table 11-4. Digital Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDD}	Input voltage		1.8	–	5.5	V
V_{CCD}	Output voltage		–	1.80	–	V
	Regulator output capacitor	±10%, X5R ceramic or better. The two V_{CCD} pins must be shorted together, with as short a trace as possible, see Power System on page 24	–	1	–	µF

11.3.2 Analog Core Regulator

Table 11-5. Analog Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDA}	Input voltage		1.8	–	5.5	V
V_{CCA}	Output voltage		–	1.80	–	V
	Regulator output capacitor	±10%, X5R ceramic or better	–	1	–	µF

11.3.3 Inductive Boost Regulator.

Table 11-6. Inductive Boost Regulator DC Specifications

Unless otherwise specified, operating conditions are: V_{BAT} = 2.4 V, V_{OUT} = 2.7 V, I_{OUT} = 40 mA, F_{SW} = 400 kHz, L_{BOOST} = 22 µH, C_{BOOST} = 22 µF || 0.1 µF

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{BAT}	Input voltage Includes startup	T=-35 °C to +65 °C	0.5	–	5.5	V
		Over entire temperature range	0.68	–	5.5	V
I_{OUT}	Load current[25, 26]	V_{BAT} = 1.6 – 3.6 V, V_{OUT} = 3.6 – 5.0 V, external diode	–	–	50	mA
		V_{BAT} = 1.6 – 3.6 V, V_{OUT} = 1.6 – 3.6 V, internal diode	–	–	75	mA
		V_{BAT} = 0.8 – 1.6 V, V_{OUT} = 1.6 – 3.6 V, internal diode	–	–	30	mA
		V_{BAT} = 0.8 – 1.6 V, V_{OUT} = 3.6 – 5.0 V, external diode	–	–	20	mA
		V_{BAT} = 0.5 – 0.8 V, V_{OUT} = 1.6 – 3.6 V, internal diode	–	–	15	mA
I_{LPK}	Inductor peak current		–	–	700	mA
I_Q	Quiescent current	Boost active mode	–	200	–	µA
		Boost standby mode, 32 khz external crystal oscillator, I_{OUT} < 1 µA	–	12	–	µA

Notes
25. For output voltages above 3.6 V, an external diode is required.
26. Maximum output current applies for output voltages ≤ 4x input voltage.

Table 11-6. Inductive Boost Regulator DC Specifications *(continued)*

Unless otherwise specified, operating conditions are: V_{BAT} = 2.4 V, V_{OUT} = 2.7 V, I_{OUT} = 40 mA, F_{SW} = 400 kHz, L_{BOOST} = 22 µH, C_{BOOST} = 22 µF || 0.1 µF

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OUT}	Boost voltage range[27, 28]					
	1.8 V		1.71	1.80	1.89	V
	1.9 V		1.81	1.90	2.00	V
	2.0 V		1.90	2.00	2.10	V
	2.4 V		2.28	2.40	2.52	V
	2.7 V		2.57	2.70	2.84	V
	3.0 V		2.85	3.00	3.15	V
	3.3 V		3.14	3.30	3.47	V
	3.6 V		3.42	3.60	3.78	V
	5.0 V	External diode required	4.75	5.00	5.25	V
Reg_{LOAD}	Load regulation		–	–	3.8	%
Reg_{LINE}	Line regulation		–	–	4.1	%
η_{OUT}	Efficiency	L_{BOOST} = 10 µH	70	85	–	%
		L_{BOOST} = 22 µH	82	90	–	%

Table 11-7. Inductive Boost Regulator AC Specifications

Unless otherwise specified, operating conditions are: V_{BAT} = 2.4 V, V_{OUT} = 2.7 V, I_{OUT} = 40 mA, F_{SW} = 400 kHz, L_{BOOST} = 22 µH, C_{BOOST} = 22 µF || 0.1 µF.

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{RIPPLE}	Ripple voltage (peak-to-peak)	V_{OUT} = 1.8 V, F_{SW} = 400 kHz, I_{OUT} = 10 mA	–	–	100	mV
F_{SW}	Switching frequency		–	0.1, 0.4, or 2	–	MHz

Table 11-8. Recommended External Components for Boost Circuit

Parameter	Description	Conditions	Min	Typ	Max	Units
L_{BOOST}	Boost inductor		4.7	10	47	µH
C_{BOOST}	Filter capacitor[27]		10	22	47	µF
I_F	External Schottky diode average forward current	External Schottky diode is required for V_{OUT} > 3.6 V	1	–	–	A
V_R			20	–	–	V

Notes
27. Based on device characterization (Not production tested).
28. At boost frequency of 2 MHz, Vboost is limited to 2 x Vbat. At 400 kHz, Vboost is limited to 4 x Vbat.

Table 11-12. SIO AC Specifications *(continued)*

Parameter	Description	Conditions	Min	Typ	Max	Units
Fsioout	SIO output operating frequency					
	3.3 V < V_{DDIO} < 5.5 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	33	MHz
	1.71 V < V_{DDIO} < 3.3 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	16	MHz
	3.3 V < V_{DDIO} < 5.5 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	5	MHz
	1.71 V < V_{DDIO} < 3.3 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	4	MHz
	3.3 V < V_{DDIO} < 5.5 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	–	–	20	MHz
	1.71 V < V_{DDIO} < 3.3 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	–	–	10	MHz
	1.71 V < V_{DDIO} < 5.5 V, Regulated output mode, slow strong drive mode	Output continuously switching into 25 pF	–	–	2.5	MHz
Fsioin	SIO input operating frequency					
	1.71 V ≤ V_{DDIO} ≤ 5.5 V	90/10% V_{DDIO}	–	–	66	MHz

11.4.3 USBIO

For operation in GPIO mode, the standard range for V_{DDD} applies, see Device Level Specifications on page 60.

Table 11-13. USBIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ pull-up resistance	With idle bus	0.900	–	1.575	kΩ
Rusba	USB D+ pull-up resistance	While receiving traffic	1.425	–	3.090	kΩ
Vohusb	Static output high	15 kΩ ±5% to Vss, internal pull-up enabled	2.8	–	3.6	V
Volusb	Static output low	15 kΩ ±5% to Vss, internal pull-up enabled	–	–	0.3	V
Vohgpio	Output voltage high, GPIO mode	I_{OH} = 4 mA, V_{DDD} ≥ 3 V	2.4	–	–	V
Volgpio	Output voltage low, GPIO mode	I_{OL} = 4 mA, V_{DDD} ≥ 3 V	–	–	0.3	V
Vdi	Differential input sensitivity	|(D+) – (D–)|	–	–	0.2	V
Vcm	Differential input common mode range	–	0.8	–	2.5	V
Vse	Single ended receiver threshold	–	0.8	–	2	V
Rps2	PS/2 pull-up resistance	In PS/2 mode, with PS/2 pull-up enabled	3	–	7	kΩ
Rext	External USB series resistor	In series with each USB pin	21.78 (–1%)	22	22.22 (+1%)	Ω
Zo	USB driver output impedance	Including Rext	28	–	44	Ω
C_{IN}	USB transceiver input capacitance	–	–	–	20	pF
I_{IL}	Input leakage current (absolute value)	25 °C, V_{DDD} = 3.0 V	–	–	2	nA

Table 11-19. Opamp AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
GBW	Gain-bandwidth product	Power mode = minimum, 200 pF load	1	–	–	MHz
		Power mode = low, 200 pF load	2	–	–	MHz
		Power mode = medium, 200 pF load	1	–	–	MHz
		Power mode = high, 200 pF load	3	–	–	MHz
SR	Slew rate, 20% - 80%	Power mode = low, 200 pF load	1.1	–	–	V/µs
		Power mode = medium, 200 pF load	0.9	–	–	V/µs
		Power mode = high, 200 pF load	3	–	–	V/µs
e_n	Input noise density	Power mode = high, Vdda = 5 V, at 100 kHz	–	45	–	nV/sqrtHz

Figure 11-10. Open Loop Gain and Phase vs Frequency and Temperature, Power Mode = High, Cl = 15 Pf, Vdda = 5V

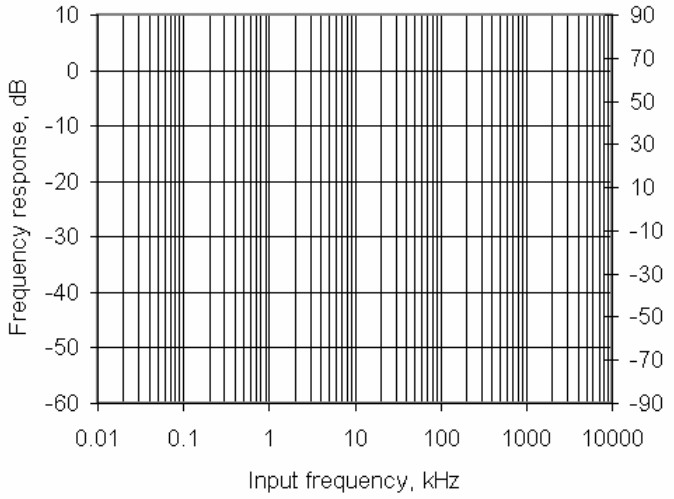


Figure 11-11. Opamp Closed Loop Frequency Response, Gain = 1, Vdda = 5V

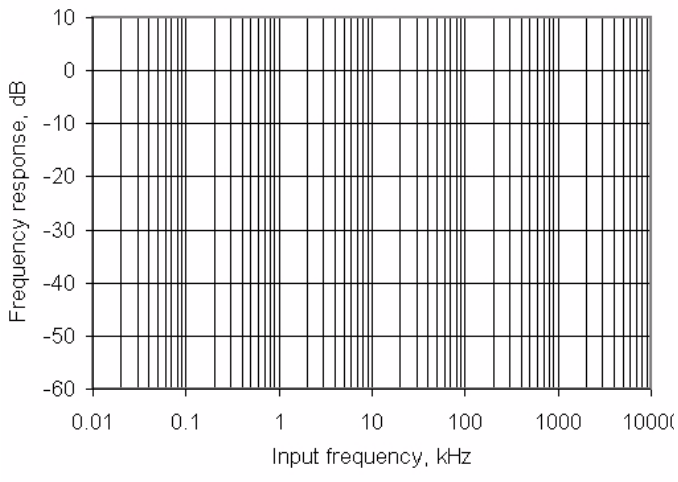


Table 11-24. Delta-sigma ADC RMS Noise vs. Input Range and Sample Rate, 16-bit, Internal Reference

RMS Noise, Counts	Input Voltage Range								
	Single-Ended				Differential				
Sample rate, sps	0 to V_{REF}	0 to V_{REF} × 2	V_{SSA} to V_{DDA}	0 to V_{REF} × 6	±V_{REF}	±V_{REF}/2	±V_{REF}/4	±V_{REF}/8	±V_{REF}/16
750									
1500									
3000									
6000									
12000									
24000									
48000									

Figure 11-23. Delta-sigma ADC DNL vs Output Code, 16-bit, 48 ksps, 25 °C V_{DDA} = 3.3 V

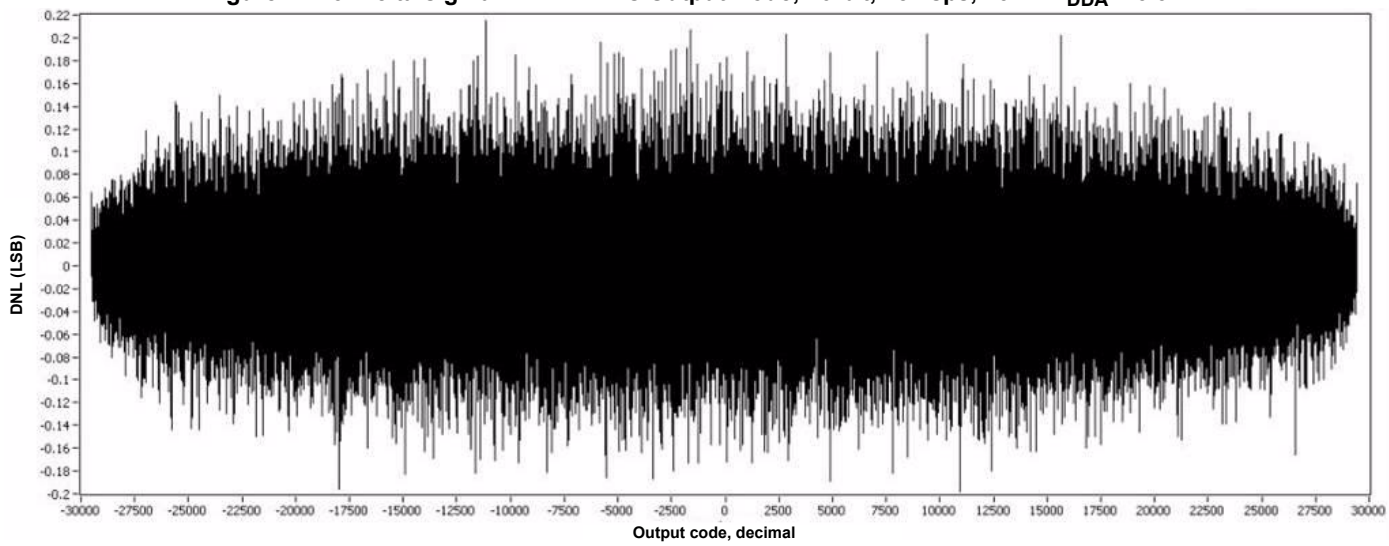


Figure 11-24. Delta-sigma ADC INL vs Output Code, 16-bit, 48 ksps, 25 °C V_{DDA} = 3.3 V

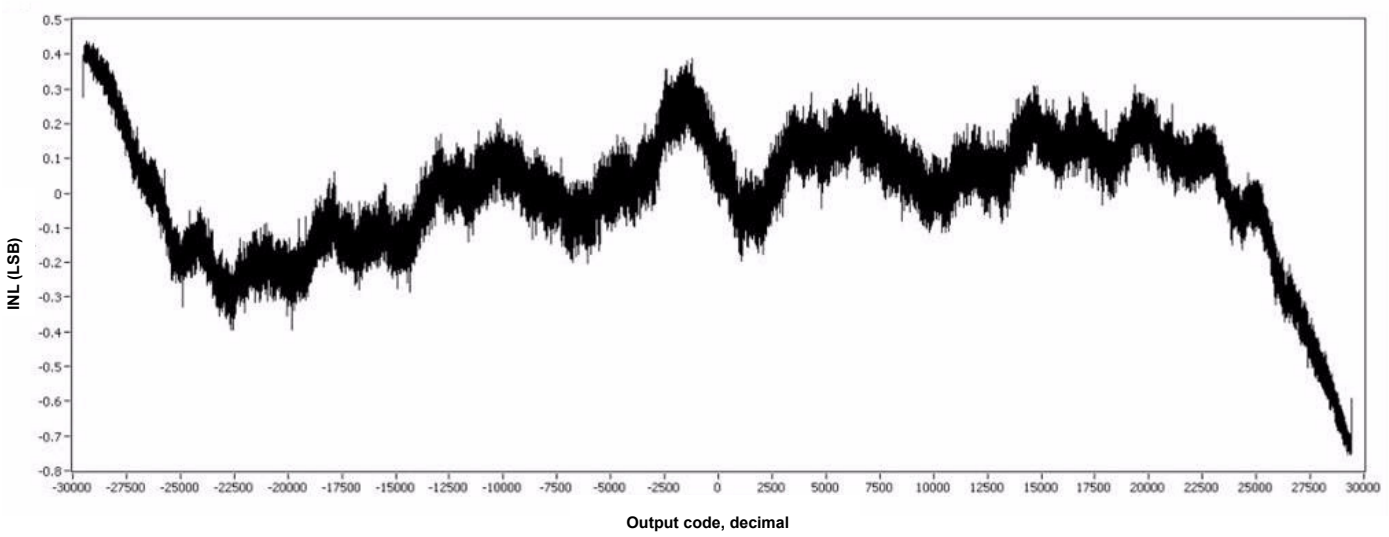


Table 11-29. IDAC DC Specifications *(continued)*

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	Operating current, code = 0	Slow mode, source mode, range = 31.875 µA	–	–	44	µA
		Slow mode, source mode, range = 255 µA,	–	–	33	µA
		Slow mode, source mode, range = 2.04 mA	–	–	33	µA
		Slow mode, sink mode, range = 31.875 µA	–	–	36	µA
		Slow mode, sink mode, range = 255 µA	–	–	33	µA
		Slow mode, sink mode, range = 2.04 mA	–	–	33	µA
		Fast mode, source mode, range = 31.875 µA	–	–	310	µA
		Fast mode, source mode, range = 255 µA	–	–	305	µA
		Fast mode, source mode, range = 2.04 mA	–	–	305	µA
		Fast mode, sink mode, range = 31.875 µA	–	–	310	µA
		Fast mode, sink mode, range = 255 µA	–	–	300	µA
		Fast mode, sink mode, range = 2.04 mA	–	–	300	µA

Figure 11-25. IDAC INL vs Input Code, Range = 255 µA, Source Mode

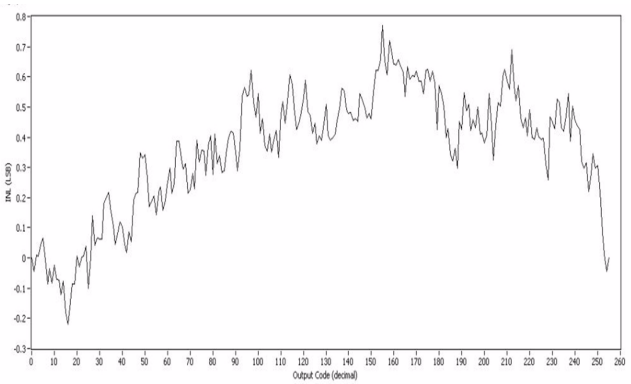
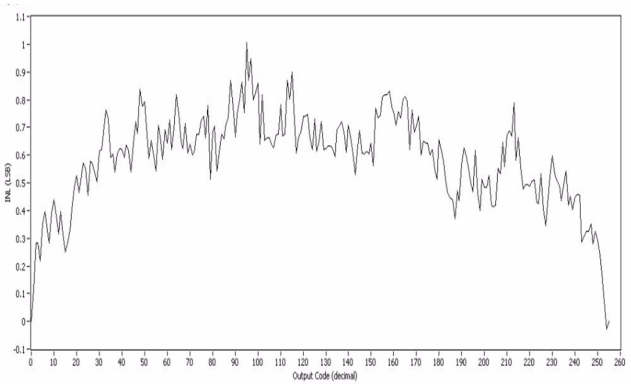


Figure 11-26. IDAC INL vs Input Code, Range = 255 µA, Sink Mode



11.5.7 Voltage Digital to Analog Converter (VDAC)

See the VDAC component datasheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, all charts and graphs show typical values.

Table 11-31. VDAC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		–	8	–	bits
INL1	Integral nonlinearity	1 V scale	–	±2.1	±2.5	LSB
DNL1	Differential nonlinearity	1 V scale	–	±0.3	±1	LSB
Rout	Output resistance	1 V scale	–	4	–	kΩ
		4 V scale	–	16	–	kΩ
V_{OUT}	Output voltage range, code = 255	1 V scale	–	1	–	V
		4 V scale, Vdda = 5 V	–	4	–	V
	Monotonicity		–	–	Yes	–
V_{OS}	Zero scale error		–	0	±0.9	LSB
Eg	Gain error	1 V scale, 25 °C	–	–	±2.5	%
		4 V scale, 25 °C	–	–	±2.5	%
TC_Eg	Temperature coefficient, gain error	1 V scale, 25 °C	–	–	0.03	%FSR / °C
		4 V scale, 25 °C	–	–	0.03	%FSR / °C
I_{DD}	Operating current	Slow mode	–	–	100	µA
		Fast mode	–	–	500	µA

Figure 11-35. VDAC INL vs Input Code, 1 V Mode

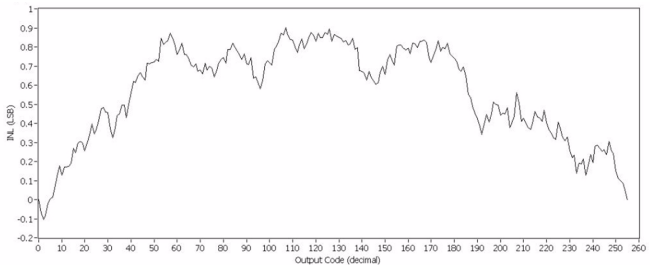


Figure 11-36. VDAC DNL vs Input Code, 1 V Mode

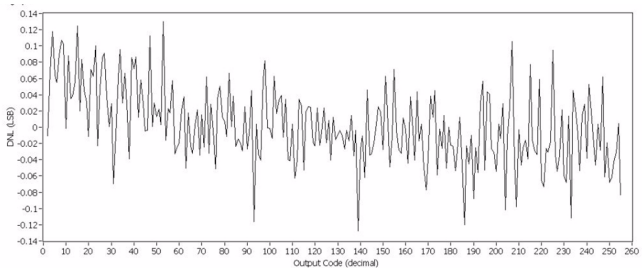


Figure 11-37. VDAC INL vs Temperature, 1 V Mode

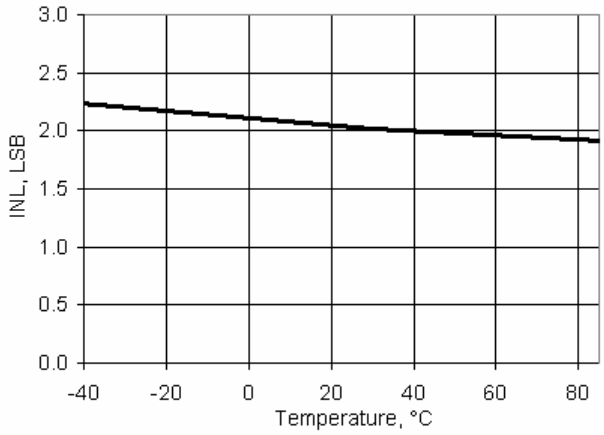
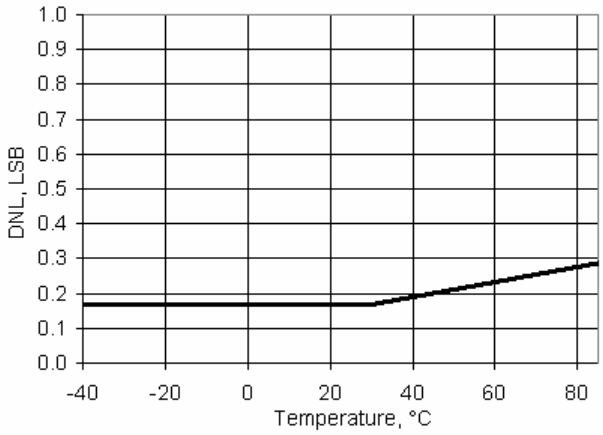


Figure 11-38. VDAC DNL vs Temperature, 1 V Mode



11.5.8 Mixer

The mixer is created using a SC/CT analog block; see the Mixer component datasheet in PSoC Creator for full electrical specifications and APIs.

Table 11-33. Mixer DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OS}	Input offset voltage		–	–	10	mV
	Quiescent current		–	0.9	2	mA
G	Gain		–	0	–	dB

Table 11-34. Mixer AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
f_{LO}	Local oscillator frequency	Down mixer mode	–	–	4	MHz
f_{in}	Input signal frequency	Down mixer mode	–	–	14	MHz
f_{LO}	Local oscillator frequency	Up mixer mode	–	–	1	MHz
f_{in}	Input signal frequency	Up mixer mode	–	–	1	MHz
SR	Slew rate		3	–	–	V/µs

11.5.9 Transimpedance Amplifier

The TIA is created using a SC/CT analog block; see the TIA component datasheet in PSoC Creator for full electrical specifications and APIs.

Table 11-35. Transimpedance Amplifier (TIA) DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{IOFF}	Input offset voltage		–	–	10	mV
Rconv	Conversion resistance[40]	R = 20K; 40 pF load	–25	–	+35	%
		R = 30K; 40 pF load	–25	–	+35	%
		R = 40K; 40 pF load	–25	–	+35	%
		R = 80K; 40 pF load	–25	–	+35	%
		R = 120K; 40 pF load	–25	–	+35	%
		R = 250K; 40 pF load	–25	–	+35	%
		R= 500K; 40 pF load	–25	–	+35	%
		R = 1M; 40 pF load	–25	–	+35	%
	Quiescent current		–	1.1	2	mA

Table 11-36. Transimpedance Amplifier (TIA) AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
BW	Input bandwidth (–3 dB)	R = 20K; –40 pF load	1500	–	–	kHz
		R = 120K; –40 pF load	240	–	–	kHz
		R = 1M; –40 pF load	25	–	–	kHz

Note
40. Conversion resistance values are not calibrated. Calibrated values and details about calibration are provided in PSoC Creator component datasheets. External precision resistors can also be used.

11.6.3 Pulse Width Modulation

The following specifications apply to the Timer/Counter/PWM peripheral, in PWM mode. PWM components can also be implemented in UDBs; for more information, see the PWM component datasheet in PSoC Creator.

Table 11-46. PWM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit PWM, at listed input clock frequency	–	–	–	µA
	3 MHz		–	15	–	µA
	12 MHz		–	60	–	µA
	48 MHz		–	260	–	µA
	67 MHz		–	350	–	µA

Table 11-47. Pulse Width Modulation (PWM) AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	67	MHz
	Pulse width		15	–	–	ns
	Pulse width (external)		30	–	–	ns
	Kill pulse width		15	–	–	ns
	Kill pulse width (external)		30	–	–	ns
	Enable pulse width		15	–	–	ns
	Enable pulse width (external)		30	–	–	ns
	Reset pulse width		15	–	–	ns
	Reset pulse width (external)		30	–	–	ns

11.6.4 I^2C

Table 11-48. Fixed I^2C DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	Enabled, configured for 100 kbps	–	–	250	µA
	–	Enabled, configured for 400 kbps	–	–	260	µA
	–	Wake from sleep mode	–	–	30	µA

Table 11-49. Fixed I^2C AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Bit rate		–	–	1	Mbps

11.6.5 Controller Area Network[41]

Table 11-50. CAN AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Bit rate	Minimum 8 MHz clock	–	–	1	Mbit

Note
41. Refer to ISO 11898 specification for details.

11.9.6 Phase-Locked Loop

Table 11-83. PLL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	PLL operating current	In = 3 MHz, Out = 67 MHz	–	400	–	µA
		In = 3 MHz, Out = 24 MHz	–	200	–	µA

Table 11-84. PLL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Fpllin	PLL input frequency[51]		1	–	48	MHz
	PLL intermediate frequency[52]	Output of prescaler	1	–	3	MHz
Fpllout	PLL output frequency[51]		24	–	67	MHz
	Lock time at startup		–	–	250	µs
Jperiod-rms	Jitter (rms)[53]		–	–	250	ps

Notes
51. This specification is guaranteed by testing the PLL across the specified range using the IMO as the source for the PLL.
52. PLL input divider, Q, must be set so that the input frequency is divided down to the intermediate frequency range. Value for Q ranges from 1 to 16.
53. Based on device characterization (Not production tested).

12. Ordering Information

In addition to the features listed in Table 12-1, every CY8C38 device includes: a precision on-chip voltage reference, precision oscillators, flash, ECC, DMA, a fixed function I²C, 4 KB trace RAM, JTAG/SWD programming and debug, external memory interface, and more. In addition to these features, the flexible UDBs and analog subsection support a wide range of peripherals. To assist you in selecting the ideal part, PSoC Creator makes a part recommendation after you choose the components required by your application. All CY8C38 derivatives incorporate device and flash security in user-selectable security levels; see the TRM for details.

Table 12-1. CY8C38 Family with Single Cycle 8051

Part Number	MCU Core				Analog								Digital				I/O[56]				Package	JTAG ID[57]
	CPU Speed (MHz)	Flash (KB)	SRAM (KB)	EEPROM (KB)	LCD Segment Drive	ADC	DAC	Comparator	SC/CT Analog Blocks[54]	Opamps	DFB	CapSense	UDBs[55]	16-bit Timer/PWM	FS USB	CAN 2.0b	Total I/O	GPIO	SIO	USBIO		
32 KB Flash																						
CY8C3865AXI-056	67	32	4	1	–	20-bit Del-Sig	4	4	4	4	✔	✔	20	4	–	–	70	62	8	0	100-pin TQFP	0×0E038069
CY8C3865LTI-045	67	32	4	1	–	20-bit Del-Sig	4	4	4	4	✔	✔	20	4	–	–	46	38	8	0	68-pin QFN	0×0E02D069
CY8C3865LTI-058	67	32	4	1	–	20-bit Del-Sig	4	4	4	2	✔	✔	20	4	–	–	29	25	4	0	48-pin QFN	0×0E03A069
CY8C3865PVI-051	67	32	4	1	–	20-bit Del-Sig	4	4	4	2	✔	✔	20	4	–	–	29	25	4	0	48-pin SSOP	0×0E033069
CY8C3865AXI-015	67	32	4	1	–	20-bit Del-Sig	4	4	4	4	✔	✔	20	4	✔	–	72	62	8	2	100-pin TQFP	0×0E00F069
CY8C3865LTI-032	67	32	4	1	–	20-bit Del-Sig	4	4	4	4	✔	✔	20	4	✔	–	48	38	8	2	68-pin QFN	0×0E020069
CY8C3865LTI-061	67	32	4	1	–	20-bit Del-Sig	4	4	4	2	✔	✔	20	4	✔	–	31	25	4	2	48-pin QFN	0×0E03D069
CY8C3865PVI-053	67	32	4	1	–	20-bit Del-Sig	4	4	4	2	✔	✔	20	4	✔	–	31	25	4	2	48-pin SSOP	0×0E035069
CY8C3865AXI-018	67	32	4	1	✔	20-bit Del-Sig	4	4	4	4	✔	✔	20	4	–	–	70	62	8	0	100-pin TQFP	0×0E012069
CY8C3865LTI-024	67	32	4	1	✔	20-bit Del-Sig	4	4	4	4	✔	✔	20	4	–	–	46	38	8	0	68-pin QFN	0×0E018069
CY8C3865LTI-059	67	32	4	1	✔	20-bit Del-Sig	4	4	4	2	✔	✔	20	4	–	–	29	25	4	0	48-pin QFN	0×0E03B069
CY8C3865PVI-060	67	32	4	1	✔	20-bit Del-Sig	4	4	4	2	✔	✔	20	4	–	–	29	25	4	0	48-pin SSOP	0×0E03C069
CY8C3865AXI-019	67	32	4	1	✔	20-bit Del-Sig	4	4	4	4	✔	✔	20	4	✔	–	72	62	8	2	100-pin TQFP	0×0E013069
CY8C3865LTI-014	67	32	4	1	✔	20-bit Del-Sig	4	4	4	4	✔	✔	20	4	✔	–	48	38	8	2	68-pin QFN	0×0E00E069
CY8C3865LTI-062	67	32	4	1	✔	20-bit Del-Sig	4	4	4	2	✔	✔	20	4	✔	–	31	25	4	2	48-pin QFN	0×0E03E069
CY8C3865PVI-063	67	32	4	1	✔	20-bit Del-Sig	4	4	4	2	✔	✔	20	4	✔	–	31	25	4	2	48-pin SSOP	0×0E03F069
64 KB Flash																						
CY8C3866AXI-054	67	64	8	2	–	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	–	–	70	62	8	0	100-pin TQFP	0×0E036069
CY8C3866LTI-020	67	64	8	2	–	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	–	–	46	38	8	0	68-pin QFN	0×0E014069
CY8C3866LTI-064	67	64	8	2	–	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	–	–	29	25	4	0	48-pin QFN	0×0E040069
CY8C3866PVI-005	67	64	8	2	–	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	–	–	29	25	4	0	48-pin SSOP	0×0E005069
CY8C3866AXI-033	67	64	8	2	–	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	✔	–	72	62	8	2	100-pin TQFP	0×0E021069
CY8C3866LTI-023	67	64	8	2	–	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	✔	–	48	38	8	2	68-pin QFN	0×0E017069
CY8C3866LTI-067	67	64	8	2	–	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	✔	–	31	25	4	2	48-pin QFN	0×0E043069
CY8C3866PVI-021	67	64	8	2	–	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	✔	–	31	25	4	2	48-pin SSOP	0×0E015069
CY8C3866AXI-038	67	64	8	2	✔	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	–	–	70	62	8	0	100-pin TQFP	0×0E026069
CY8C3866LTI-029	67	64	8	2	✔	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	–	–	46	38	8	0	68-pin QFN	0×0E01D069
CY8C3866LTI-065	67	64	8	2	✔	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	–	–	29	25	4	0	48-pin QFN	0×0E041069
CY8C3866PVI-066	67	64	8	2	✔	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	–	–	29	25	4	0	48-pin SSOP	0×0E042069

Notes

54. Analog blocks support a variety of functionality including TIA, PGA, and mixers. See the Example Peripherals on page 35 for more information on how analog blocks can be used.
55. UDBs support a variety of functionality including SPI, LIN, UART, timer, counter, PWM, PRS, and others. Individual functions may use a fraction of a UDB or multiple UDBs. Multiple functions can share a single UDB. See the Example Peripherals on page 35 for more information on how UDBs can be used.
56. The I/O Count includes all types of digital I/O: GPIO, SIO, and the two USB I/O. See the I/O System and Routing on page 28 for details on the functionality of each of these types of I/O.
57. The JTAG ID has three major fields. The most significant nibble (left digit) is the version, followed by a 2 byte part number and a 3 nibble manufacturer ID.

Table 12-1. CY8C38 Family with Single Cycle 8051 *(continued)*

Part Number	MCU Core				Analog								Digital				I/O[60]				Package	JTAG ID[61]
	CPU Speed (MHz)	Flash (KB)	SRAM (KB)	EEPROM (KB)	LCD Segment Drive	ADC	DAC	Comparator	SC/CT Analog Blocks[58]	Opamps	DFB	CapSense	UDBs[59]	16-Bit Timer/PWM	FS USB	CAN 2.0b	Total I/O	GPIO	SIO	USBIO		
CY8C3866AXI-039	67	64	8	2	✔	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	✔	–	72	62	8	2	100-pin TQFP	0×0E027069
CY8C3866LTI-030	67	64	8	2	✔	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	✔	–	48	38	8	2	68-pin QFN	0×0E01E069
CY8C3866LTI-068	67	64	8	2	✔	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	✔	✔	31	25	4	2	48-pin QFN	0×0E044069
CY8C3866PVI-069	67	64	8	2	✔	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	✔	–	31	25	4	2	48-pin SSOP	0×0E045069
CY8C3866AXI-040	67	64	8	2	✔	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	✔	✔	72	62	8	2	100-pin TQFP	0×0E028069
CY8C3866PVI-047	67	64	8	2	–	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	–	✔	29	25	4	0	48-pin SSOP	0×0E02F069
CY8C3866PVI-070	67	64	8	2	✔	20-bit Del-Sig	4	4	4	2	✔	✔	24	4	–	✔	29	25	4	0	48-pin SSOP	0×0E046069
CY8C3866AXI-055	67	64	8	2	–	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	–	✔	70	62	8	0	100-pin TQFP	0×0E037069
CY8C3866AXI-035	67	64	8	2	✔	20-bit Del-Sig	4	4	4	4	✔	✔	24	4	–	✔	70	62	8	0	100-pin TQFP	0×0E023069

Notes
58. Analog blocks support a variety of functionality including TIA, PGA, and mixers. See the Example Peripherals on page 35 for more information on how analog blocks can be used.
59. UDBs support a variety of functionality including SPI, LIN, UART, timer, counter, PWM, PRS, and others. Individual functions may use a fraction of a UDB or multiple UDBs. Multiple functions can share a single UDB. See the Example Peripherals on page 35 for more information on how UDBs can be used.
60. The I/O Count includes all types of digital I/O: GPIO, SIO, and the two USB I/O. See the I/O System and Routing on page 28 for details on the functionality of each of these types of I/O.
61. The JTAG ID has three major fields. The most significant nibble (left digit) is the version, followed by a 2 byte part number and a 3 nibble manufacturer ID.

Table 16-1. Units of Measure *(continued)*

Symbol	Unit of Measure
µA	microamperes
µF	microfarads
µH	microhenrys
µs	microseconds
µV	microvolts
µW	microwatts
mA	milliamperes
ms	milliseconds
mV	millivolts
nA	nanoamperes
ns	nanoseconds
nV	nanovolts
Ω	ohms
pF	picofarads
ppm	parts per million
ps	picoseconds
s	seconds
sps	samples per second
sqrtHz	square root of hertz
V	volts

Description Title: PSoC® 3: CY8C38 Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-11729				
*K	2903576	04/01/2010	MKEA	Updated Vb pin in PCB Schematic. Updated Tstartup parameter in AC Specifications table. Added Load regulation and Line regulation parameters to Inductive Boost Regulator DC Specifications table. Updated I_{CC} parameter in LCD Direct Drive DC Specs table. In page 1, updated internal oscillator range under Precision programmable clocking to start from 3 MHz. Updated I_{OUT} parameter in LCD Direct Drive DC Specs table. Updated Table 6-2 and Table 6-3. Added bullets on CapSense in page 1; added CapSense column in Section 12. Removed some references to footnote [1]. Changed INC_Rn cycles from 3 to 2 (Table 4-1). Added footnote in PLL AC Specification table. Added PLL intermediate frequency row with footnote in PLL AC Specs table. Added UDBs subsection under 11.6 Digital Peripherals. Updated Figure 2-6 (PCB Layout). Updated Pin Descriptions section and modified Figures 6-6, 6-8, 6-9. Updated LVD in Tables 6-2 and 6-3; modified Low-power modes bullet in page 1. Added note to Figures 2-5 and 6-2; Updated Figure 6-2 to add capacitors for V_{DDA} and V_{DDD} pins. Updated boost converter section (6.2.2). Updated Tstartup values in Table 11-3. Removed IPOR rows from Table 11-68. Updated 6.3.1.1, Power Voltage Level Monitors. Updated section 5.2 and Table 11-2 to correct suggestion of execution from flash. Updated V_{REF} specs in Table 11-21. Updated IDAC uncompensated gain error in Table 11-25. Updated Delay from Interrupt signal input to ISR code execution from ISR code in Table11-72. Removed other line in table. Added sentence to last paragraph of section 6.1.1.3. Updated T_{RESP}, high and low-power modes, in Table 11-24. Updated f_TCK values in Table 11-73 and f_SWDCK values in Table 11-74. Updated SNR condition in Table 11-20. Corrected unit of measurement in Table 11-21. Updated sleep wakeup time in Table 6-3 and Tsleep in Table 11-3. Added 1.71 V <= V_{DDD} < 3.3 V, SWD over USBIO pins value to Table 11-74. Removed mention of hibernate reset (HRES) from page 1 features, Table 6-3, Section 6.2.1.4, Section 6.3, and Section 6.3.1.1. Changed PPOR/PRES to TBDs in Section 6.3.1.1, Section 6.4.1.6 (changed PPOR to reset), Table 11-3 (changed PPOR to PRES), Table 11-68 (changed title, values TBD), and Table 11-69 (changed PPOR_TR to PRES_TR). Added sentence saying that LVD circuits can generate a reset to Section 6.3.1.1. Changed I_{DD} values on page 1, page 5, and Table 11-2. Changed resume time value in Section 6.2.1.3. Changed ESD HBM value in Table 11-1. Changed SNR in 16-bit resolution mode value and sample rate row in Table 11-20. Removed V_{DDA} = 1.65 V rows and changed BWag value in Table 11-22. Changed V_{IOFF} values and changed CMRR value in Table 11-23. Changed INL max value in Table 11-27. Added max value to the Quiescent current specs in Tables 11-29 and 11-31. Changed occurrences of “Block” to “Row” and deleted the “ECC not included” footnote in Table 11-57. Changed max response time value in Tables 11-69 and 11-71. Changed the Startup time in Table 11-79. Added condition to intermediate frequency row in Table 11-85. Added row to Table 11-69. Added brown out note to Section 11.8.1.