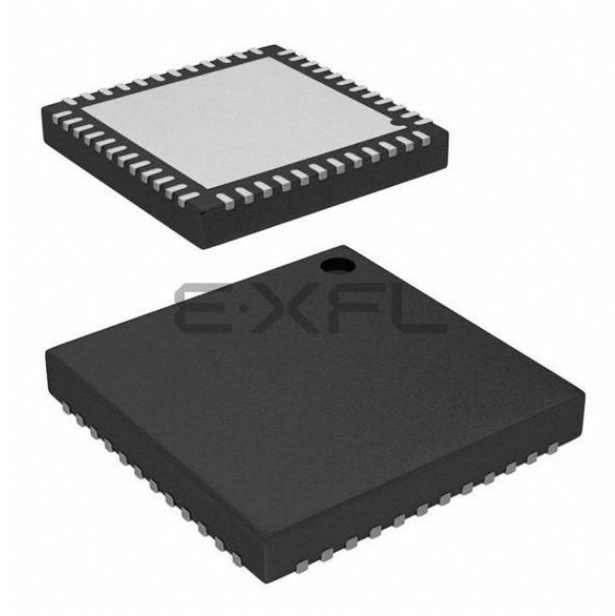

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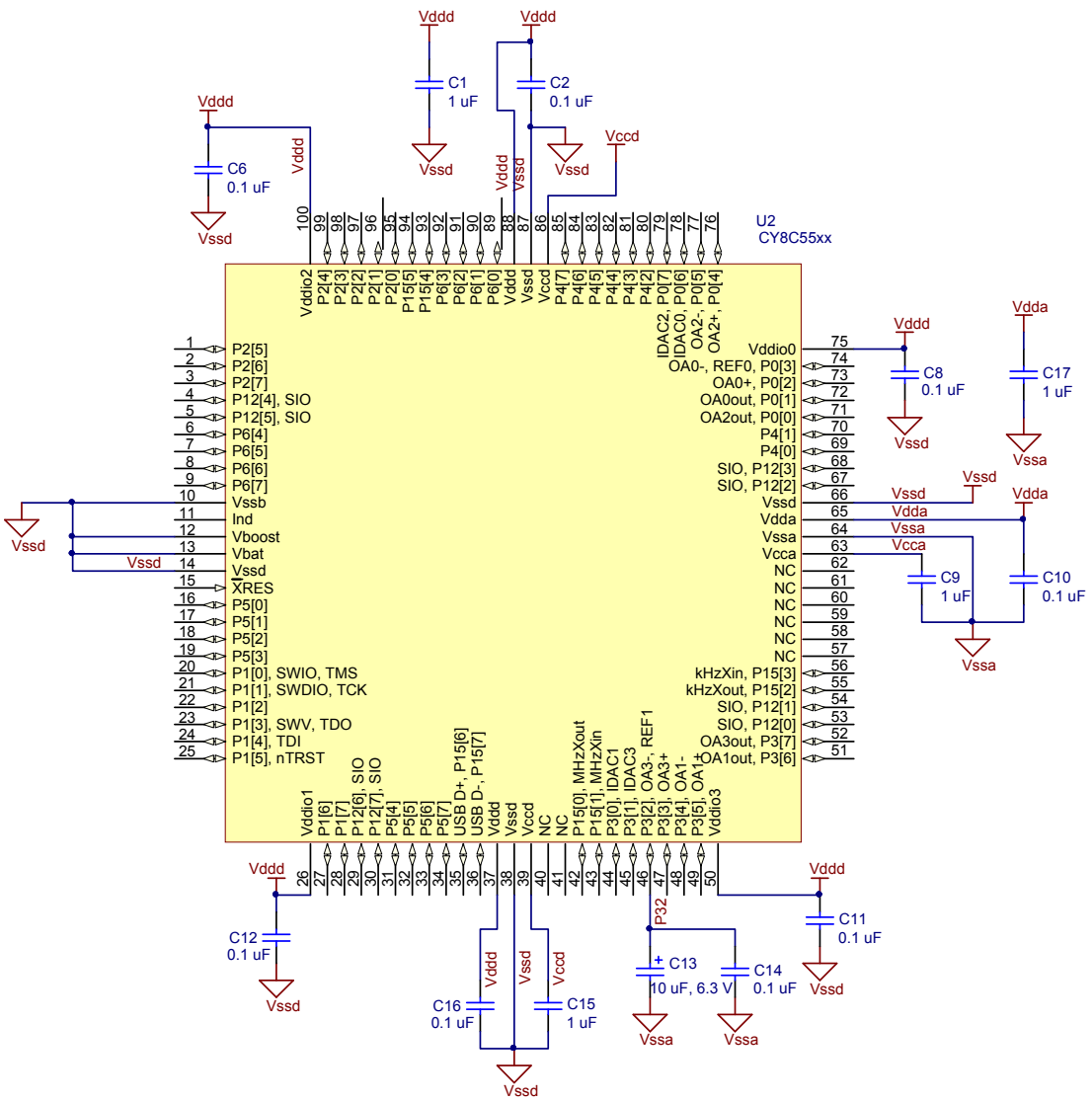
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x20b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3866lti-065

Figure 2-5. Example Schematic for 100-pin TQFP Part with Power Connections



Note The two Vccd pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in Figure 2-6 on page 10.

TMS

JTAG test mode select programming and debug port connection.

USBIO, D+

Provides D+ connection directly to a USB 2.0 bus. May be used as a digital I/O pin; it is powered from V_{DDD} instead of from a Vddio. Pins are Do Not Use (DNU) on devices without USB.

USBIO, D–

Provides D– connection directly to a USB 2.0 bus. May be used as a digital I/O pin; it is powered from V_{DDD} instead of from a Vddio. Pins are Do Not Use (DNU) on devices without USB.

Vboost

Power sense connection to boost pump.

Vbat

Battery supply to boost pump.

Vcca

Output of analog core regulator and input to analog core. Requires a 1-µF capacitor to V_{SSA}. Regulator output not for external use.

Vccd

Output of digital core regulator and input to digital core. The two V_{CCD} pins must be shorted together, with the trace between them as short as possible, and a 1-µF capacitor to V_{SSD}; see Power System on page 24. Regulator output not for external use.

Vdda

Supply for all analog peripherals and analog core regulator. **Vdda must be the highest voltage present on the device. All other supply pins must be less than or equal to Vdda.**

Vddd

Supply for all digital peripherals and digital core regulator. Vddd must be less than or equal to Vdda.

Vssa

Ground for all analog peripherals.

Vssb

Ground connection for boost pump.

Vssd

Ground for all digital logic and I/O pins.

Vddio0, Vddio1, Vddio2, Vddio3

Supply for I/O pins. Each Vddio must be tied to a valid operating voltage (1.71 V to 5.5 V), and must be less than or equal to Vdda. If the I/O pins associated with Vddio0, Vddio2, or Vddio3 are not used then that Vddio should be tied to ground (Vssd or Vssa).

$\overline{\text{XRES}}$ (and configurable $\overline{\text{XRES}}$)

External reset pin. Active low with internal pull-up. In 48-pin SSOP parts and 48-pin QFN parts, P1[2] may be configured as $\overline{\text{XRES}}$. In all other parts the pin is configured as a GPIO.

4. CPU

4.1 8051 CPU

The CY8C38 devices use a single cycle 8051 CPU, which is fully compatible with the original MCS-51 instruction set. The CY8C38 family uses a pipelined RISC architecture, which executes most instructions in 1 to 2 cycles to provide peak performance of up to 33 MIPS with an average of 2 cycles per instruction. The single cycle 8051 CPU runs ten times faster than a standard 8051 processor.

The 8051 CPU subsystem includes these features:

- Single cycle 8051 CPU
- Up to 64 KB of flash memory, up to 2 KB of EEPROM, and up to 8 KB of SRAM
- Programmable nested vector interrupt controller
- DMA controller
- Peripheral HUB (PHUB)
- External memory interface (EMIF)

4.2 Addressing Modes

The following addressing modes are supported by the 8051:

- Direct Addressing: The operand is specified by a direct 8-bit address field. Only the internal RAM and the SFRs can be accessed using this mode.
- Indirect Addressing: The instruction specifies the register which contains the address of the operand. The registers R0 or R1 are used to specify the 8-bit address, while the data pointer (DPTR) register is used to specify the 16-bit address.
- Register Addressing: Certain instructions access one of the registers (R0 to R7) in the specified register bank. These instructions are more efficient because there is no need for an address field.
- Register Specific Instructions: Some instructions are specific to certain registers. For example, some instructions always act on the accumulator. In this case, there is no need to specify the operand.
- Immediate Constants: Some instructions carry the value of the constants directly instead of an address.
- Indexed Addressing: This type of addressing can be used only for a read of the program memory. This mode uses the Data Pointer as the base and the accumulator value as an offset to read a program memory.
- Bit Addressing: In this mode, the operand is one of 256 bits.

4.3 Instruction Set

The 8051 instruction set is highly optimized for 8-bit handling and Boolean operations. The types of instructions supported include:

- Arithmetic instructions
- Logical instructions
- Data transfer instructions
- Boolean instructions
- Program branching instructions

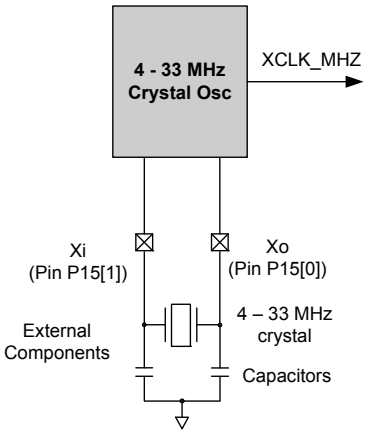
The 33-kHz clock (CLK33K) comes from a divide-by-3 operation on CLK100K. This output can be used as a reduced accuracy version of the 32.768-kHz ECO clock with no need for a crystal.

6.1.2 External Oscillators

6.1.2.1 MHz External Crystal Oscillator

The MHzECO provides high frequency, high precision clocking using an external crystal (see Figure 6-2). It supports a wide variety of crystal types, in the range of 4 to 33 MHz. When used in conjunction with the PLL, it can generate CPU and system clocks up to the device's maximum frequency (see PLL). The GPIO pins connecting to the external crystal and capacitors are fixed. MHzECO accuracy depends on the crystal chosen.

Figure 6-2. MHzECO Block Diagram

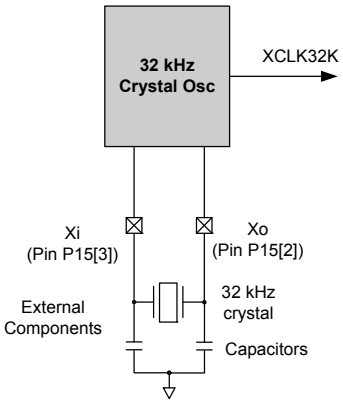


6.1.2.2 32.768-kHz ECO

The 32.768-kHz external crystal oscillator (32kHzECO) provides precision timing with minimal power consumption using an external 32.768-kHz watch crystal (see Figure 6-3). The 32kHzECO also connects directly to the sleep timer and provides the source for the RTC. The RTC uses a 1-second interrupt to implement the RTC functionality in firmware.

The oscillator works in two distinct power modes. This allows users to trade off power consumption with noise immunity from neighboring circuits. The GPIO pins connected to the external crystal and capacitors are fixed.

Figure 6-3. 32kHzECO Block Diagram



6.1.2.3 Digital System Interconnect

The DSI provides routing for clocks taken from external clock oscillators connected to I/O. The oscillators can also be generated within the device in the digital system and UDBs.

While the primary DSI clock input provides access to all clocking resources, up to eight other DSI clocks (internally or externally generated) may be routed directly to the eight digital clock dividers. This is only possible if there are multiple precision clock sources.

6.1.3 Clock Distribution

All seven clock sources are inputs to the central clock distribution system. The distribution system is designed to create multiple high precision clocks. These clocks are customized for the design's requirements and eliminate the common problems found with limited resolution prescalers attached to peripherals. The clock distribution system generates several types of clock trees.

- The system clock is used to select and supply the fastest clock in the system for general system clock requirements and clock synchronization of the PSoC device.
- Bus clock 16-bit divider uses the system clock to generate the system's bus clock used for data transfers. Bus clock is the source clock for the CPU clock divider.
- Eight fully programmable 16-bit clock dividers generate digital system clocks for general use in the digital system, as configured by the design's requirements. Digital system clocks can generate custom clocks derived from any of the seven clock sources for any purpose. Examples include baud rate generators, accurate PWM periods, and timer clocks, and many others. If more than eight digital clock dividers are required, the UDBs and fixed function timer/counter/PWMs can also generate clocks.
- Four 16-bit clock dividers generate clocks for the analog system components that require clocking, such as ADC and mixers. The analog clock dividers include skew control to ensure that critical analog events do not occur simultaneously with digital switching events. This is done to reduce analog system noise.

Each clock divider consists of an 8-input multiplexer, a 16-bit clock divider (divide by 2 and higher) that generates ~50 percent duty cycle clocks, system clock resynchronization logic, and deglitch logic. The outputs from each digital clock tree can be routed into the digital system interconnect and then brought back into the clock system as an input, allowing clock chaining of up to 32 bits.

6.1.4 USB Clock Domain

The USB clock domain is unique in that it operates largely asynchronously from the main clock network. The USB logic contains a synchronous bus interface to the chip, while running on an asynchronous clock to process USB data. The USB logic requires a 48 MHz frequency. This frequency can be generated from different sources, including DSI clock at 48 MHz or doubled value of 24 MHz from internal oscillator, DSI signal, or crystal oscillator.

Figure 6-8. GPIO Block Diagram

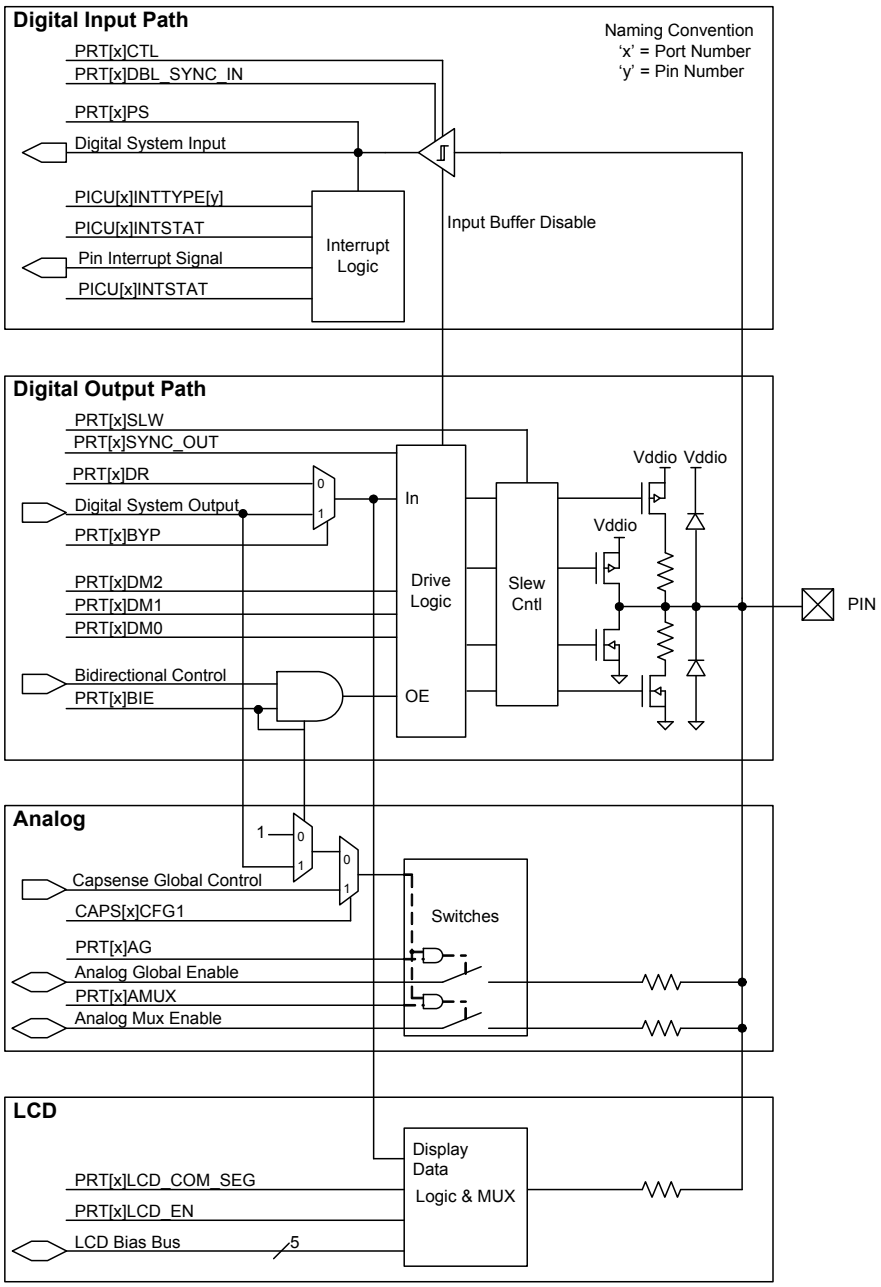
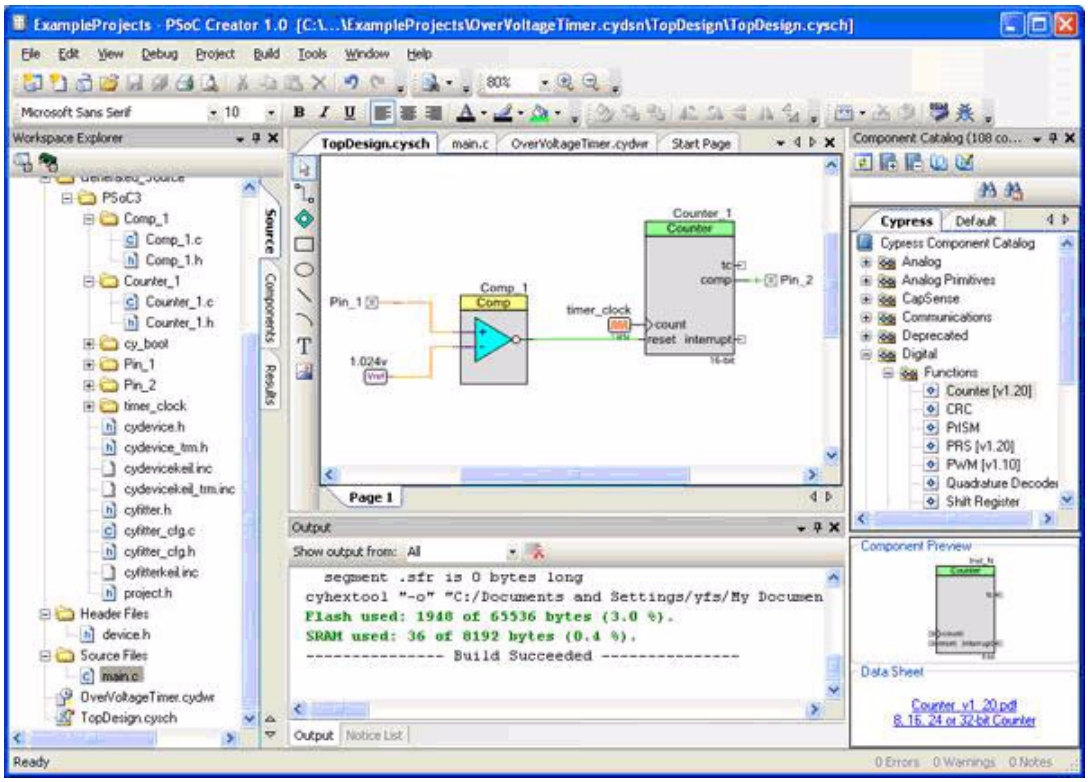
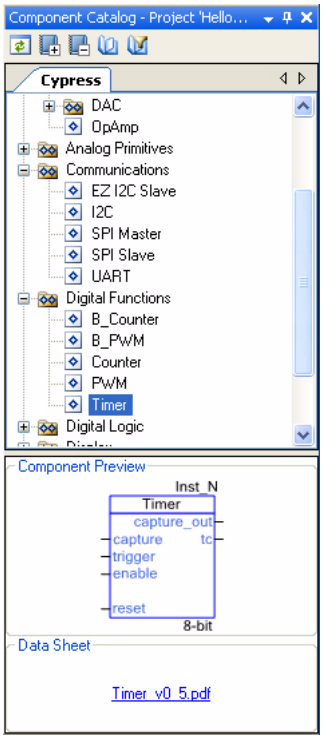


Figure 7-2. PSoC Creator Framework



7.1.4.2 Component Catalog

Figure 7-3. Component Catalog



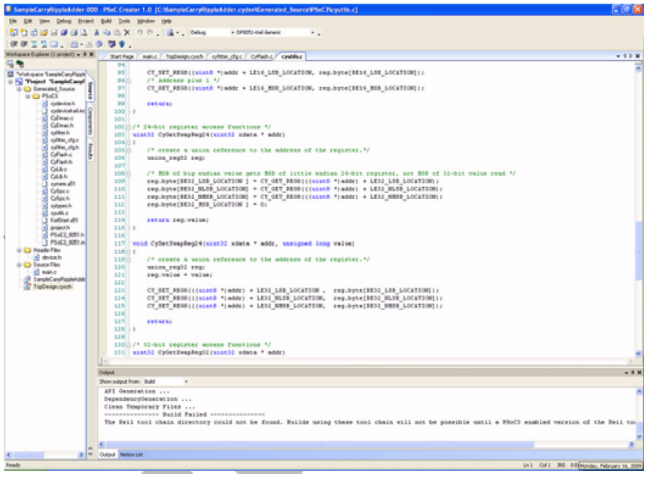
The component catalog is a repository of reusable design elements that select device functionality and customize your PSoC device. It is populated with an impressive selection of content; from simple primitives such as logic gates and device registers, through the digital timers, counters and PWMs, plus analog components such as ADC, DACs, and filters, and communication protocols, such as I^2C, USB, and CAN. See Example Peripherals on page 35 for more details about available peripherals. All content is fully characterized and carefully documented in datasheets with code examples, AC/DC specifications, and user code ready APIs.

7.1.4.3 Design Reuse

The symbol editor gives you the ability to develop reusable components that can significantly reduce future design time. Just draw a symbol and associate that symbol with your proven design. PSoC Creator allows for the placement of the new symbol anywhere in the component catalog along with the content provided by Cypress. You can then reuse your content as many times as you want, and in any number of projects, without ever having to revisit the details of the implementation.

7.1.4.4 Software Development

Figure 7-4. Code Editor

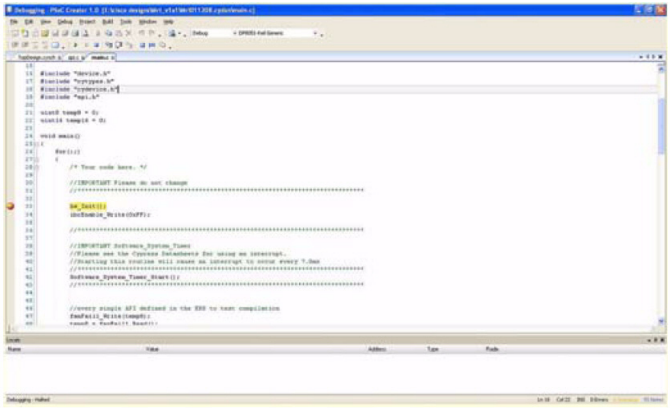


Anchoring the tool is a modern, highly customizable user interface. It includes project management and integrated editors for C and assembler source code, as well the design entry tools.

Project build control leverages compiler technology from top commercial vendors such as ARM® Limited, Keil™, and CodeSourcery (GNU). Free versions of Keil C51 and GNU C Compiler (GCC) for ARM, with no restrictions on code size or end product distribution, are included with the tool distribution. Upgrading to more optimizing compilers is a snap with support for the professional Keil C51 product and ARM RealView™ compiler.

7.1.4.5 Nonintrusive Debugging

Figure 7-5. PSoC Creator Debugger



With JTAG (4-wire) and SWD (2-wire) debug connectivity available on all devices, the PSoC Creator debugger offers full control over the target device with minimum intrusion. Breakpoints and code execution commands are all readily available from toolbar buttons and an impressive lineup of windows—register, locals, watch, call stack, memory and peripherals—make for an unparalleled level of visibility into the system.

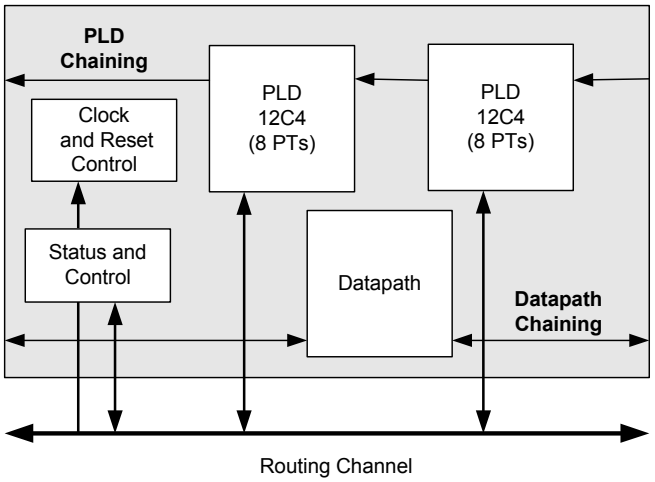
PSoC Creator contains all the tools necessary to complete a design, and then to maintain and extend that design for years to come. All steps of the design flow are carefully integrated and optimized for ease-of-use and to maximize productivity.

7.2 Universal Digital Block

The UDB represents an evolutionary step to the next generation of PSoC embedded digital peripheral functionality. The architecture in first generation PSoC digital blocks provides coarse programmability in which a few fixed functions with a small number of options are available. The new UDB architecture is the optimal balance between configuration granularity and efficient implementation. A cornerstone of this approach is to provide the ability to customize the devices digital operation to match application requirements.

To achieve this, UDBs consist of a combination of uncommitted logic (PLD), structured logic (Datapath), and a flexible routing scheme to provide interconnect between these elements, I/O connections, and other peripherals. UDB functionality ranges from simple self contained functions that are implemented in one UDB, or even a portion of a UDB (unused resources are available for other functions), to more complex functions that require multiple UDBs. Examples of basic functions are timers, counters, CRC generators, PWMs, dead band generators, and communications functions, such as UARTs, SPI, and I^2C. Also, the PLD blocks and connectivity provide full featured general purpose programmable logic within the limits of the available resources.

Figure 7-6. UDB Block Diagram



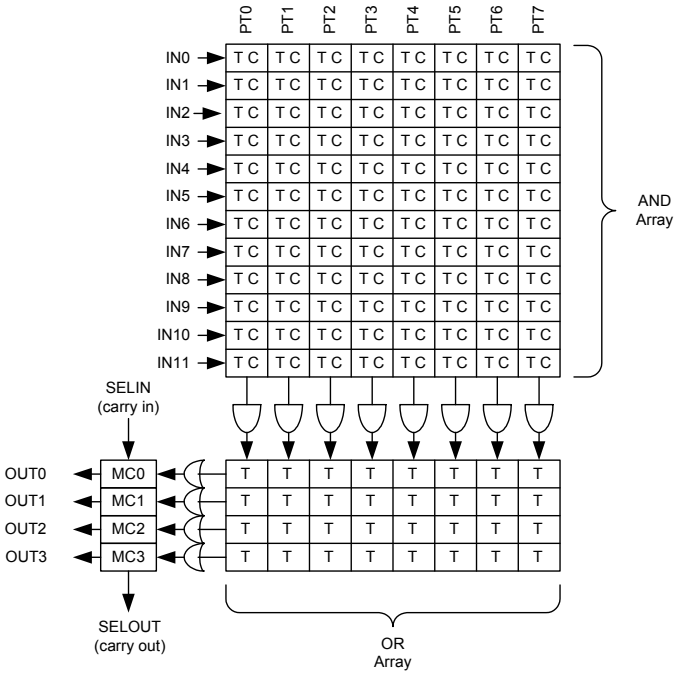
The main component blocks of the UDB are:

- PLD blocks – There are two small PLDs per UDB. These blocks take inputs from the routing array and form registered or combinational sum-of-products logic. PLDs are used to implement state machines, state bits, and combinational logic equations. PLD configuration is automatically generated from graphical primitives.
- Datapath module – This 8-bit wide datapath contains structured logic to implement a dynamically configurable ALU, a variety of compare configurations and condition generation. This block also contains input/output FIFOs, which are the primary parallel data interface between the CPU/DMA system and the UDB.
- Status and control module – The primary role of this block is to provide a way for CPU firmware to interact and synchronize with UDB operation.
- Clock and reset module – This block provides the UDB clocks and reset selection and control.

7.2.1 PLD Module

The primary purpose of the PLD blocks is to implement logic expressions, state machines, sequencers, lookup tables, and decoders. In the simplest use model, consider the PLD blocks as a standalone resource onto which general purpose RTL is synthesized and mapped. The more common and efficient use model is to create digital functions from a combination of PLD and datapath blocks, where the PLD implements only the random logic and state portion of the function while the datapath (ALU) implements the more structured elements.

Figure 7-7. PLD 12C4 Structure

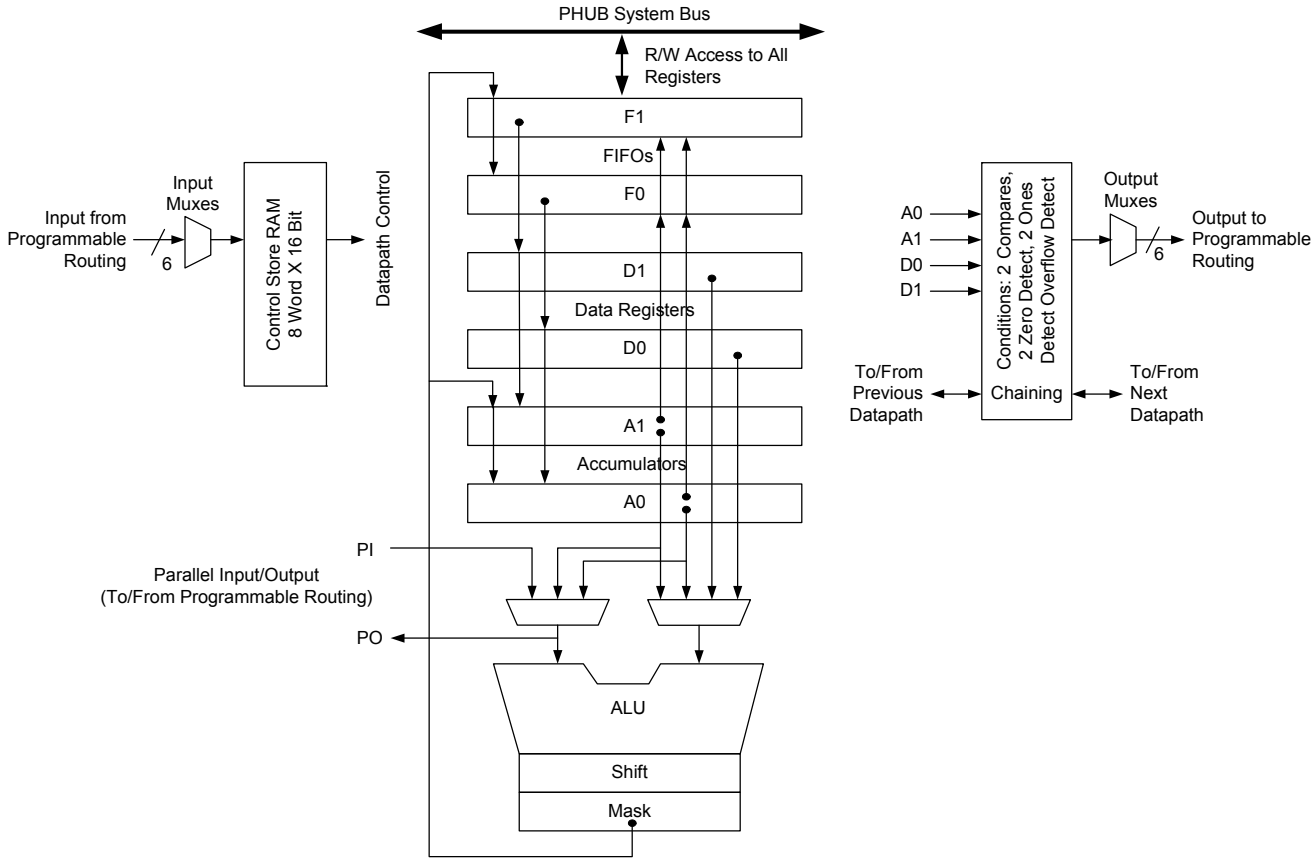


One 12C4 PLD block is shown in Figure 7-7. This PLD has 12 inputs, which feed across eight product terms. Each product term (AND function) can be from 1 to 12 inputs wide, and in a given product term, the true (T) or complement (C) of each input can be selected. The product terms are summed (OR function) to create the PLD outputs. A sum can be from 1 to 8 product terms wide. The 'C' in 12C4 indicates that the width of the OR gate (in this case 8) is constant across all outputs (rather than variable as in a 22V10 device). This PLA like structure gives maximum flexibility and insures that all inputs and outputs are permutable for ease of allocation by the software tools. There are two 12C4 PLDs in each UDB.

7.2.2 Datapath Module

The datapath contains an 8-bit single cycle ALU, with associated compare and condition generation logic. This datapath block is optimized to implement embedded functions, such as timers, counters, integrators, PWMs, PRS, CRC, shifters and dead band generators and many others.

Figure 7-8. Datapath Top Level



7.2.2.1 Working Registers

The datapath contains six primary working registers, which are accessed by CPU firmware or DMA during normal operation.

Table 7-1. Working Datapath Registers

Name	Function	Description
A0 and A1	Accumulators	These are sources and sinks for the ALU and also sources for the compares.
D0 and D1	Data Registers	These are sources for the ALU and sources for the compares.
F0 and F1	FIFOs	These are the primary interface to the system bus. They can be a data source for the data registers and accumulators or they can capture data from the accumulators or ALU. Each FIFO is four bytes deep.

7.2.2.2 Dynamic Datapath Configuration RAM

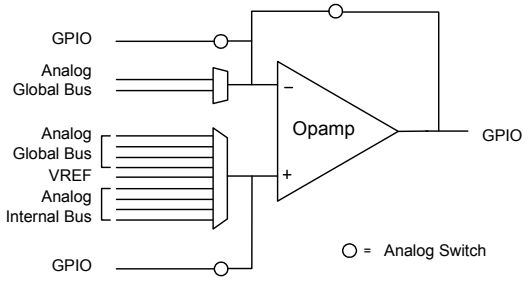
Dynamic configuration is the ability to change the datapath function and internal configuration on a cycle-by-cycle basis, under sequencer control. This is implemented using the 8-word × 16-bit configuration RAM, which stores eight unique 16-bit wide configurations. The address input to this RAM controls the sequence, and can be routed from any block connected to the UDB routing matrix, most typically PLD logic, I/O pins, or from the outputs of this or other datapath blocks.

ALU

The ALU performs eight general purpose functions. They are:

- Increment
- Decrement
- Add
- Subtract
- Logical AND
- Logical OR
- Logical XOR
- Pass, used to pass a value through the ALU to the shift register, mask, or another UDB register.

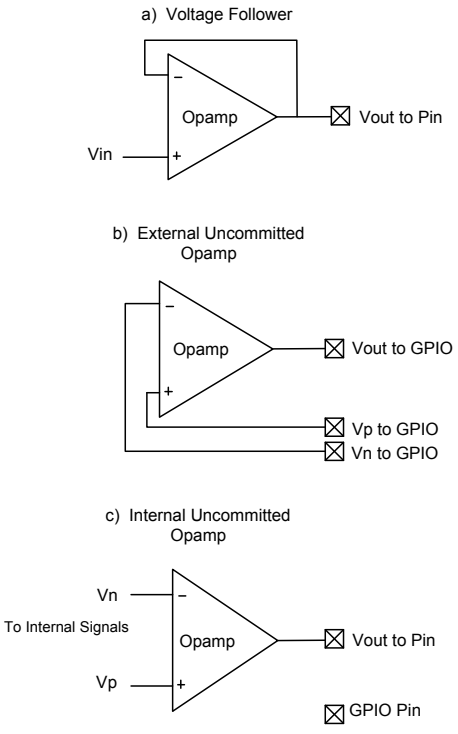
Figure 8-7. Opamp



The opamp is uncommitted and can be configured as a gain stage or voltage follower, or output buffer on external or internal signals.

See Figure 8-8. In any configuration, the input and output signals can all be connected to the internal global signals and monitored with an ADC, or comparator. The configurations are implemented with switches between the signals and GPIO pins.

Figure 8-8. Opamp Configurations



The opamp has three speed modes, slow, medium, and fast. The slow mode consumes the least amount of quiescent power and the fast mode consumes the most power. The inputs are able to swing rail-to-rail. The output swing is capable of rail-to-rail operation at low current output, within 50 mV of the rails. When driving high current loads (about 25 mA) the output voltage may only get within 500 mV of the rails.

8.5 Programmable SC/CT Blocks

The CY8C38 family of devices contains up to four switched capacitor/continuous time (SC/CT) blocks in a device. Each switched capacitor/continuous time block is built around a single rail-to-rail high bandwidth opamp.

Switched capacitor is a circuit design technique that uses capacitors plus switches instead of resistors to create analog functions. These circuits work by moving charge between capacitors by opening and closing different switches. Nonoverlapping in phase clock signals control the switches, so that not all switches are ON simultaneously.

The PSoC Creator tool offers a user friendly interface, which allows you to easily program the SC/CT blocks. Switch control and clock phase control configuration is done by PSoC Creator so users only need to determine the application use parameters such as gain, amplifier polarity, V_{REF} connection, and so on.

The same opamps and block interfaces are also connectable to an array of resistors which allows the construction of a variety of continuous time functions.

The opamp and resistor array is programmable to perform various analog functions including

- Naked operational amplifier – Continuous mode
- Unity-gain buffer – Continuous mode
- PGA – Continuous mode
- Transimpedance amplifier (TIA) – Continuous mode
- Up/down mixer – Continuous mode
- Sample and hold mixer (NRZ S/H) – Switched cap mode
- First order analog to digital modulator – Switched cap mode

8.5.1 Naked Opamp

The Naked Opamp presents both inputs and the output for connection to internal or external signals. The opamp has a unity gain bandwidth greater than 6.0 MHz and output drive current up to 650 µA. This is sufficient for buffering internal signals (such as DAC outputs) and driving external loads greater than 7.5 kohms.

8.5.2 Unity Gain

The Unity Gain buffer is a Naked Opamp with the output directly connected to the inverting input for a gain of 1.00. It has a –3 dB bandwidth greater than 6.0 MHz.

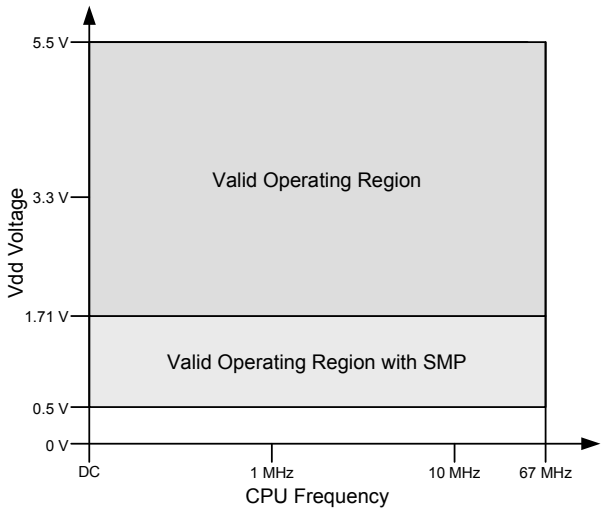
8.5.3 PGA

The PGA amplifies an external or internal signal. The PGA can be configured to operate in inverting mode or noninverting mode. The PGA function may be configured for both positive and negative gains as high as 50 and 49 respectively. The gain is adjusted by changing the values of R1 and R2 as illustrated in Figure 8-9. The schematic in Figure 8-9 shows the configuration and possible resistor settings for the PGA. The gain is switched from inverting and non inverting by changing the shared select value of the both the input muxes. The bandwidth for each gain case is listed in Table 8-3.

Table 11-3. AC Specifications[24]

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{CPU}	CPU frequency	1.71 V ≤ V_{DDD} ≤ 5.5 V	DC	–	67	MHz
F_{BUSCLK}	Bus frequency	1.71 V ≤ V_{DDD} ≤ 5.5 V	DC	–	67	MHz
Svdd	V_{DD} ramp rate		–	–	1	V/ns
T_{IO_INIT}	Time from V_{DDD}/V_{DDA}/V_{CCD}/V_{CCA} ≥ IPOR to I/O ports set to their reset states		–	–	10	µs
$T_{STARTUP}$	Time from V_{DDD}/V_{DDA}/V_{CCD}/V_{CCA} ≥ PRES to CPU executing code at reset vector	V_{CCA}/V_{DDA} = regulated from V_{DDA}/V_{DDD}, no PLL used, fast IMO boot mode (48 MHz typ.)	–	–	33	µs
		V_{CCA}/V_{CCD} = regulated from V_{DDA}/V_{DDD}, no PLL used, slow IMO boot mode (12 MHz typ.)	–	–	66	µs
T_{SLEEP}	Wakeup from sleep mode – Application of non-LVD interrupt to beginning of execution of next CPU instruction		–	–	15	µs
$T_{HIBERNATE}$	Wakeup from hibernate mode – Application of external interrupt to beginning of execution of next CPU instruction		–	–	100	µs

Figure 11-1. F_{CPU} vs. V_{DD}



Note
24. Based on device characterization (Not production tested).

Table 11-14. USBIO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Tdrate	Full-speed data rate average bit rate		12 – 0.25%	12	12 + 0.25%	MHz
Tjr1	Receiver data jitter tolerance to next transition		–8	–	8	ns
Tjr2	Receiver data jitter tolerance to pair transition		–5	–	5	ns
Tdj1	Driver differential jitter to next transition		–3.5	–	3.5	ns
Tdj2	Driver differential jitter to pair transition		–4	–	4	ns
Tfdeop	Source jitter for differential transition to SE0 transition		–2	–	5	ns
Tfeopt	Source SE0 interval of EOP		160	–	175	ns
Tfeopr	Receiver SE0 interval of EOP		82	–	–	ns
Tfst	Width of SE0 interval during differential transition		–	–	14	ns
Fgpio_out	GPIO mode output operating frequency	$3\ V \le V_{DDD} \le 5.5\ V$	–	–	20	MHz
		$V_{DDD} = 1.71\ V$	–	–	6	MHz
Tr_gpio	Rise time, GPIO mode, 10%/90% V_{DDD}	$V_{DDD} > 3\ V$, 25 pF load	–	–	12	ns
		$V_{DDD} = 1.71\ V$, 25 pF load	–	–	40	ns
Tf_gpio	Fall time, GPIO mode, 90%/10% V_{DDD}	$V_{DDD} > 3\ V$, 25 pF load	–	–	12	ns
		$V_{DDD} = 1.71\ V$, 25 pF load	–	–	40	ns

Table 11-15. USB Driver AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Tr	Transition rise time		–	–	20	ns
Tf	Transition fall time		–	–	20	ns
TR	Rise/fall time matching	V_{USB_5}, $V_{USB\_3.3}$, see USB DC Specifications on page 93	90%	–	111%	
Vcrs	Output signal crossover voltage		1.3	–	2	V

11.4.4 XRES

Table 11-16. XRES DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input voltage high threshold		$0.7 \times V_{DDIO}$	–	–	V
V_{IL}	Input voltage low threshold		–	–	$0.3 \times V_{DDIO}$	V
Rpullup	Pull-up resistor		3.5	5.6	8.5	kΩ
C_{IN}	Input capacitance[32]		–	3	–	pF
V_H	Input voltage hysteresis (Schmitt-Trigger)[32]		–	100	–	mV
Idiode	Current through protection diode to V_{DDIO} and V_{SSIO}		–	–	100	µA

Table 11-17. XRES AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{RESET}	Reset pulse width		1	–	–	µs

Note
32. Based on device characterization (Not production tested).

11.5.2 Delta-sigma ADC

Unless otherwise specified, operating conditions are:

- Operation in continuous sample mode
- fclk = 3.072 MHz for resolution = 16 to 20 bits; fclk = 6.144 MHz for resolution = 8 to 15 bits
- Reference = 1.024 V internal reference bypassed on P3.2 or P0.3
- Unless otherwise specified, all charts and graphs show typical values

Table 11-20. 20-bit Delta-sigma ADC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		8	–	20	bits
	Number of channels, single ended		–	–	No. of GPIO	–
	Number of channels, differential	Differential pair is formed using a pair of GPIOs.	–	–	No. of GPIO/2	–
	Monotonic	Yes	–	–	–	–
Ge	Gain error	Buffered, buffer gain = 1, modulator gain = 1, 16-bit mode, 25 °C	–	–	±0.2	%
Gd	Gain drift	Buffered, buffer gain = 1, modulator gain = 1, 16-bit mode	–	–	50	ppm/°C
Vos	Input offset voltage	Buffered	–	–	±0.1	mV
TCVos	ADC TC input offset voltage	Temperature coefficient, input offset voltage	–	–	55	µV/°C
	Input voltage range, single ended[33]		V_{SSA}	–	V_{DDA}	V
	Input voltage range, differential unbuffered[33]		V_{SSA}	–	V_{DDA}	V
	Input voltage range, differential, buffered[33]		V_{SSA}	–	$V_{DDA} – 1$	V
PSRRb	Power supply rejection ratio, buffered[33]	Buffer gain = 1, 16-bit, Range = ±1.024 V	90	–	–	dB
CMRRb	Common mode rejection ratio, buffered[33]	Buffer gain = 1, 16 bit, Range = ±1.024 V	85	–	–	dB
INL20	Integral non linearity[33]	Range = ±1.024 V, unbuffered	–	–	±32	LSB
DNL20	Differential non linearity[33]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
INL16	Integral non linearity[33]	Range = ±1.024 V, unbuffered	–	–	±2	LSB
DNL16	Differential non linearity[33]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
INL12	Integral non linearity[33]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
DNL12	Differential non linearity[33]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
INL8	Integral non linearity[33]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
DNL8	Differential non linearity[33]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
Rin_Buff	ADC input resistance	Input buffer used	10	–	–	MΩ
Rin_ADC16	ADC input resistance	Input buffer bypassed, 16-bit, Range = ±1.024 V	–	74[34]	–	kΩ
Rin_ADC12	ADC input resistance	Input buffer bypassed, 12 bit, Range = ±1.024 V	–	148[34]	–	kΩ
Cin_G1	ADC input capacitance[33]	Gain = 1	–	5	–	pF

Notes

33. Based on device characterization (not production tested).
34. By using switched capacitors at the ADC input an effective input resistance is created. Holding the gain and number of bits constant, the resistance is proportional to the inverse of the clock frequency. This value is calculated, not measured. For more information see the Technical Reference Manual.

Table 11-20. 20-bit Delta-sigma ADC DC Specifications *(continued)*

Parameter	Description	Conditions	Min	Typ	Max	Units
Vextref	ADC external reference input voltage, see also internal reference in Voltage Reference on page 80	Pins P0[3], P3[2]	0.9	–	1.3	V
Current Consumption						
I_{DD_20}	Current consumption, 20 bit[35]	187 sps, unbuffered	–	–	1.25	mA
I_{DD_16}	Current consumption, 16 bit[35]	48 ksps, unbuffered	–	–	1.2	mA
I_{DD_12}	Current consumption, 12 bit[35]	192 ksps, unbuffered	–	–	1.4	mA
I_{BUFF}	Buffer current consumption[35]		–	–	2.5	mA

Table 11-21. Delta-sigma ADC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Startup time		–	–	4	Samples
THD	Total harmonic distortion[35]	Buffer gain = 1, 16 bit, Range = ±1.024 V	–	–	0.0032	%
20-Bit Resolution Mode						
SR20	Sample rate[35]	Range = ±1.024 V, unbuffered	7.8	–	187	sps
BW20	Input bandwidth at max sample rate[35]	Range = ±1.024 V, unbuffered	–	40	–	Hz
16-Bit Resolution Mode						
SR16	Sample rate[35]	Range = ±1.024 V, unbuffered	2	–	48	ksps
BW16	Input bandwidth at max sample rate[35]	Range = ±1.024 V, unbuffered	–	11	–	kHz
SINAD16int	Signal to noise ratio, 16-bit, internal reference[35]	Range = ±1.024V, unbuffered	81	–	–	dB
SINAD16ext	Signal to noise ratio, 16-bit, external reference[35]	Range = ±1.024 V, unbuffered	84	–	–	dB
12-Bit Resolution Mode						
SR12	Sample rate, continuous, high power[35]	Range = ±1.024 V, unbuffered	4	–	192	ksps
BW12	Input bandwidth at max sample rate[35]	Range = ±1.024 V, unbuffered	–	44	–	kHz
SINAD12int	Signal to noise ratio, 12-bit, internal reference[35]	Range = ±1.024 V, unbuffered	66	–	–	dB
8-Bit Resolution Mode						
SR8	Sample rate, continuous, high power[35]	Range = ±1.024 V, unbuffered	8	–	384	ksps
BW8	Input bandwidth at max sample rate[35]	Range = ±1.024 V, unbuffered	–	88	–	kHz
SINAD8int	Signal to noise ratio, 8-bit, internal reference[35]	Range = ±1.024 V, unbuffered	43	–	–	dB

Notes
35. Based on device characterization (Not production tested).

Figure 11-19. Delta-sigma ADC Noise Histogram, 1000 Samples, 20-Bit, 187 sps, Ext Ref, $V_{IN} = V_{REF}/2$, Range = ±1.024 V

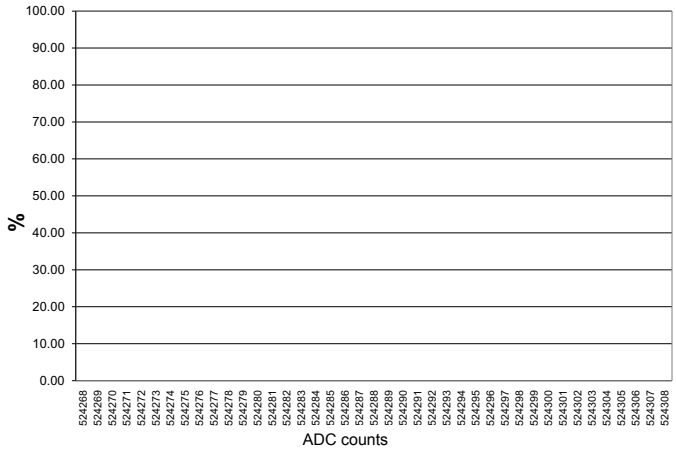


Figure 11-20. Delta-sigma ADC Noise Histogram, 1000 samples, 16-bit, 48 ksps, Ext Ref, $V_{IN} = V_{REF}/2$, Range = ±1.024 V

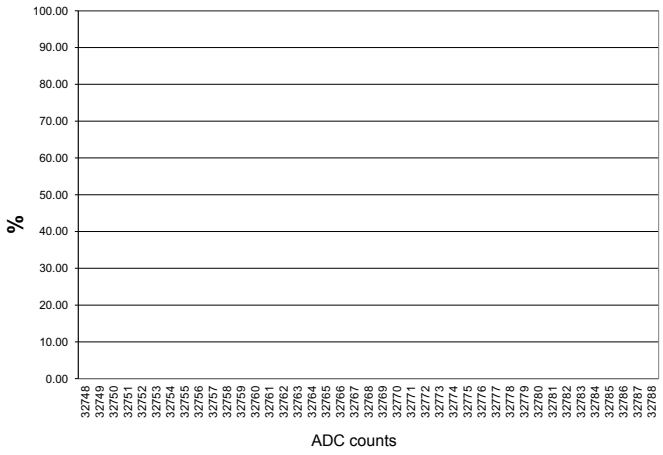


Figure 11-21. Delta-sigma ADC Noise Histogram, 1000 samples, 16-bit, 48 ksps, Int Ref, $V_{IN} = V_{REF}/2$, Range = ±1.024 V

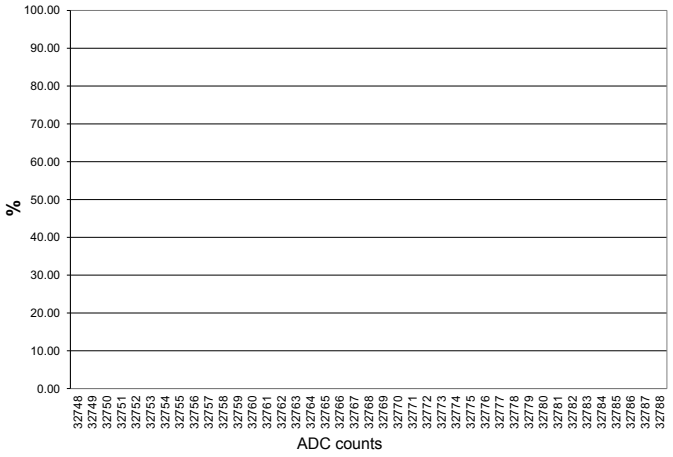


Figure 11-22. Delta-sigma ADC Noise Histogram, 1000 samples, 12-bit, 192 ksps, Int Ref, $V_{IN} = V_{REF}/2$, Range = ±1.024 V

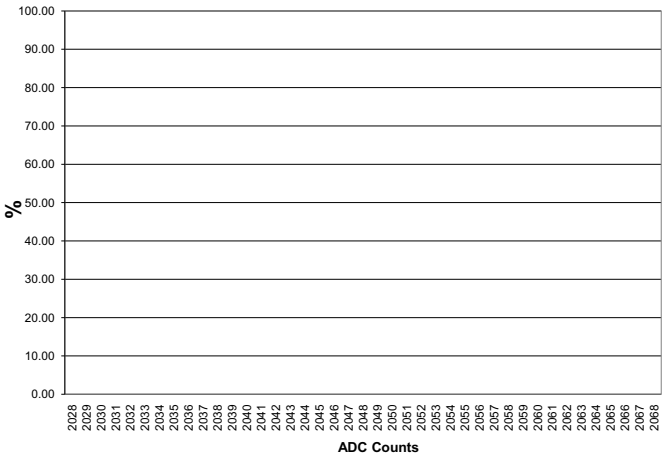


Table 11-23. Delta-sigma ADC RMS Noise vs. Input Range and Sample Rate, 20-bit, External Reference

RMS Noise, Counts	Input Voltage Range								
	Single-Ended				Differential				
Sample rate, sps	0 to V_{REF}	0 to V_{REF} × 2	V_{SSA} to V_{DDA}	0 to V_{REF} × 6	±V_{REF}	±$V_{REF}/2$	±$V_{REF}/4$	±$V_{REF}/8$	±$V_{REF}/16$
2.8									
5.6									
11.3									
22.5									
45									
90									
187.5									

Table 11-28. Comparator AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{RESP}	Response time, high current mode[39]	50 mV overdrive, measured pin-to-pin	–	75	110	ns
	Response time, low current mode[39]	50 mV overdrive, measured pin-to-pin	–	155	200	ns
	Response time, ultra low-power mode[39]	50 mV overdrive, measured pin-to-pin	–	55	–	µs

11.5.6 Current Digital-to-analog Converter(IDAC)

See the IDAC component datasheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, all charts and graphs show typical values.

Table 11-29. IDAC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		–	–	8	bits
I_{OUT}	Output current at code = 255	Range = 2.048 mA, code = 255, $V_{DDA} \geq 2.7$ V, Rload = 600 Ω	–	2.048	–	mA
		Range = 2.048 mA, High mode, code = 255, $V_{DDA} \leq 2.7$ V, Rload = 300 Ω	–	2.048	–	mA
		Range = 255 µA, code = 255, Rload = 600 Ω	–	255	–	µA
		Range = 31.875 µA, code = 255, Rload = 600 Ω	–	31.875	–	µA
	Monotonicity		–	–	Yes	
Ezs	Zero scale error		–	0	±1	LSB
Eg	Gain error	Range = 2.048 mA, 25 °C	–	–	±2.5	%
		Range = 255 µA, 25 ° C	–	–	±2.5	%
		Range = 31.875 µA, 25 ° C	–	–	±3.5	%
TC_Eg	Temperature coefficient of gain error	Range = 2.048 mA	–	–	0.04	% / °C
		Range = 255 µA	–	–	0.04	% / °C
		Range = 31.875 µA	–	–	0.05	% / °C
INL	Integral nonlinearity	Sink mode, range = 255 µA, Codes 8 – 255, Rload = 2.4 kΩ, Cload = 15 pF	–	±0.9	±1	LSB
		Source mode, range = 255 µA, Codes 8 – 255, Rload = 2.4 kΩ, Cload = 15 pF	–	±1.2	±1.5	LSB
DNL	Differential nonlinearity	Sink mode, range = 255 µA, Rload = 2.4 kΩ, Cload = 15 pF	–	±0.3	±1	LSB
		Source mode, range = 255 µA, Rload = 2.4 kΩ, Cload = 15 pF	–	±0.3	±1	LSB
Vcompliance	Dropout voltage, source or sink mode	Voltage headroom at max current, Rload to Vdda or Rload to Vssa, Vdiff from Vdda	1	–	–	V

Note
39. Based on device characterization (Not production tested).

Figure 11-33. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Source Mode

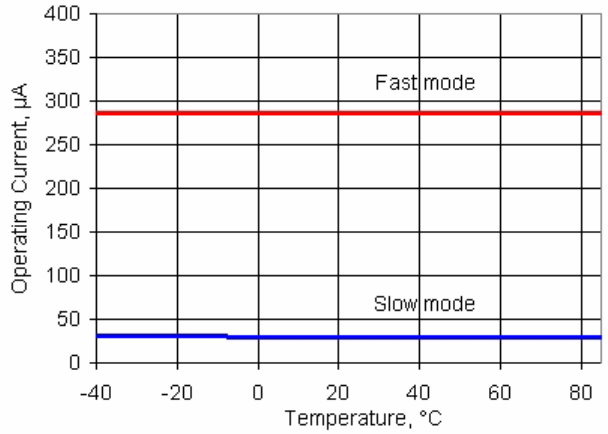


Figure 11-34. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Sink Mode

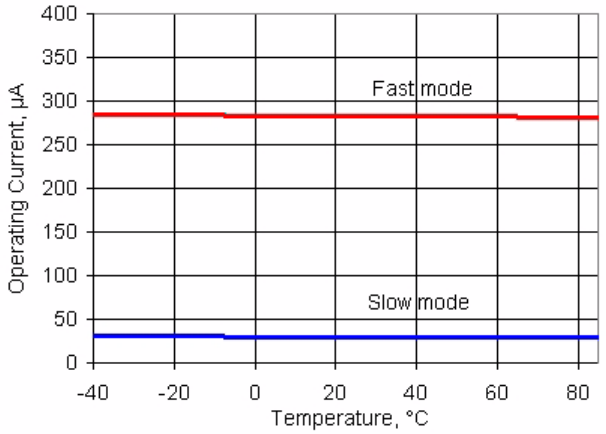


Table 11-30. IDAC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DAC}	Update rate		–	–	8	Msps
T_{SETTLE}	Settling time to 0.5 LSB	Range = 31.875 µA or 255 µA, full scale transition, fast mode, 600 Ω 15-pF load	–	–	125	ns

11.6 Digital Peripherals

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.6.1 Timer

The following specifications apply to the Timer/Counter/PWM peripheral in timer mode. Timers can also be implemented in UDBs; for more information, see the Timer component datasheet in PSoC Creator.

Table 11-42. Timer DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit timer, at listed input clock frequency	–	–	–	µA
	3 MHz		–	15	–	µA
	12 MHz		–	60	–	µA
	48 MHz		–	260	–	µA
	67 MHz		–	350	–	µA

Table 11-43. Timer AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	67	MHz
	Capture pulse width (Internal)		15	–	–	ns
	Capture pulse width (external)		30	–	–	ns
	Timer resolution		15	–	–	ns
	Enable pulse width		15	–	–	ns
	Enable pulse width (external)		30	–	–	ns
	Reset pulse width		15	–	–	ns
	Reset pulse width (external)		30	–	–	ns

11.6.2 Counter

The following specifications apply to the Timer/Counter/PWM peripheral, in counter mode. Counters can also be implemented in UDBs; for more information, see the Counter component datasheet in PSoC Creator.

Table 11-44. Counter DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit counter, at listed input clock frequency	–	–	–	µA
	3 MHz		–	15	–	µA
	12 MHz		–	60	–	µA
	48 MHz		–	260	–	µA
	67 MHz		–	350	–	µA

Table 11-45. Counter AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	67	MHz
	Capture pulse		15	–	–	ns
	Resolution		15	–	–	ns
	Pulse width		15	–	–	ns
	Pulse width (external)		30			ns
	Enable pulse width		15	–	–	ns
	Enable pulse width (external)		30	–	–	ns
	Reset pulse width		15	–	–	ns
	Reset pulse width (external)		30	–	–	ns

Table 11-63. Asynchronous Read Cycle Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T	EMIF clock period[43]	Vdda ≥ 3.3 V	30.3	–	–	nS
Tcel	EM_CEn low time		2T – 5	–	2T+ 5	nS
Taddrv	EM_CEn low to EM_Addr valid		–	–	5	nS
Taddrh	Address hold time after EM_Wen high		T	–	–	nS
Toel	EM_OEn low time		2T – 5	–	2T + 5	nS
Tdoesu	Data to EM_OEn high setup time		T + 15	–	–	nS
Tdoeh	Data hold time after EM_OEn high		3	–	–	nS

Figure 11-49. Asynchronous Write Cycle Timing

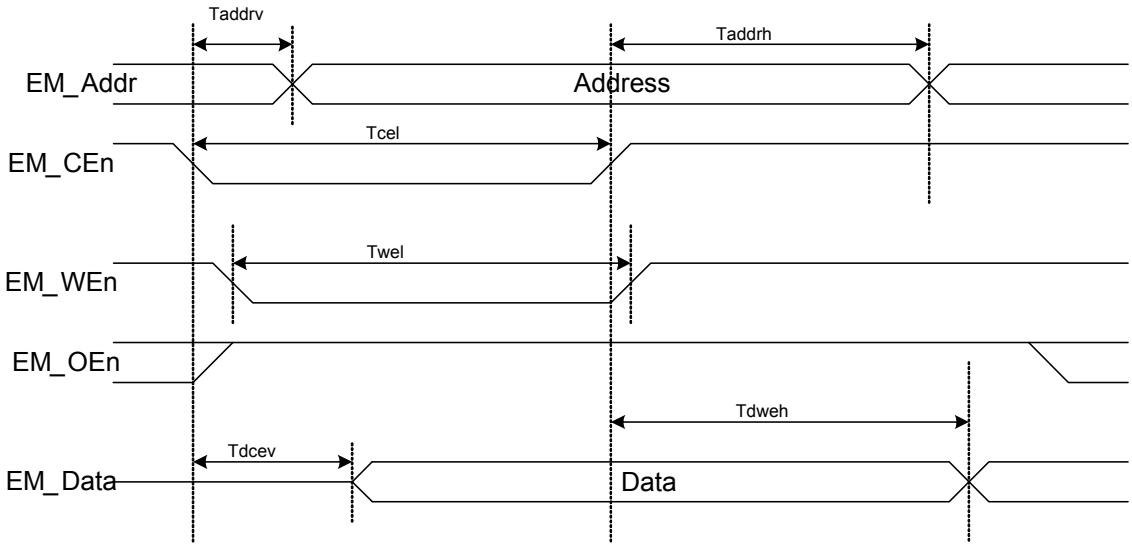


Table 11-64. Asynchronous Write Cycle Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T	EMIF clock period[43]	Vdda ≥ 3.3 V	30.3	–	–	nS
Tcel	EM_CEn low time		T – 5	–	T + 5	nS
Taddrv	EM_CEn low to EM_Addr valid		–	–	5	nS
Taddrh	Address hold time after EM_WEn high		T	–	–	nS
Twel	EM_WEn low time		T – 5	–	T + 5	nS
Tdcev	EM_CEn low to data valid		–	–	7	nS
Tdweh	Data hold time after EM_WEn high		T	–	–	nS

Note
43. Limited by GPIO output frequency, see Table 11-10 on page 65.

13. Packaging

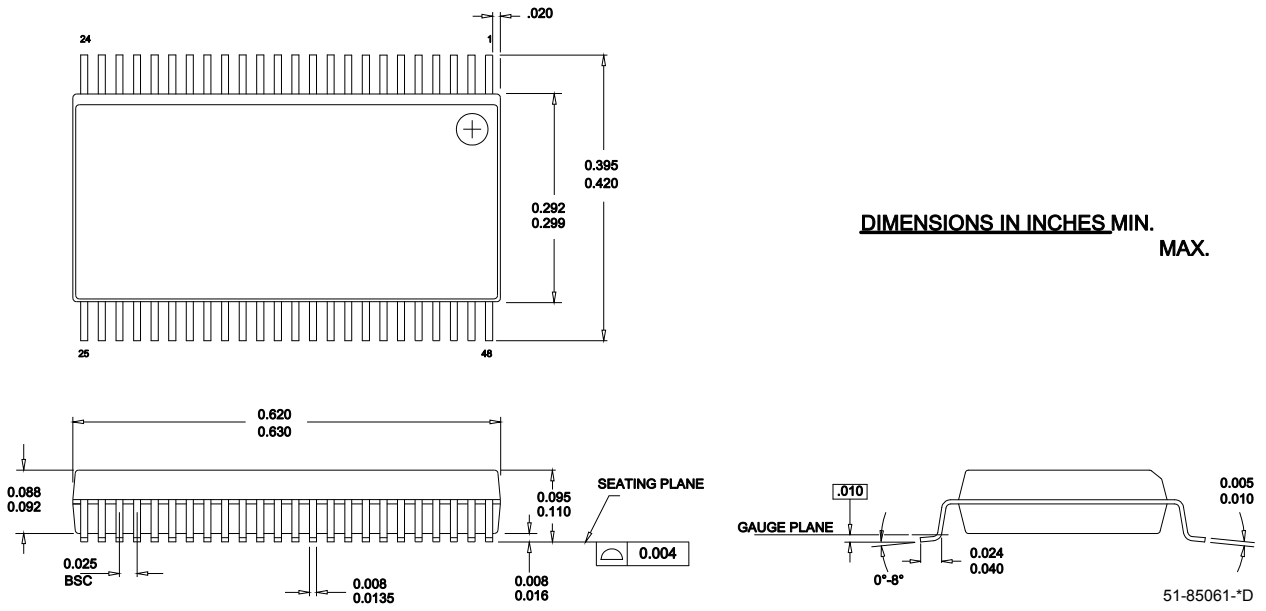
Table 13-1. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature		–40	25.00	85	°C
T_J	Operating junction temperature		–40	–	100	°C
Tja	Package θJA (48-pin SSOP)		–	45.16	–	°C/Watt
Tja	Package θJA (48-pin QFN)		–	15.94	–	°C/Watt
Tja	Package θJA (68-pin QFN)		–	11.72	–	°C/Watt
Tja	Package θJA (100-pin TQFP)		–	30.52	–	°C/Watt
Tjc	Package θJC (48-pin SSOP)		–	27.84	–	°C/Watt
Tjc	Package θJC (48-pin QFN)		–	7.05	–	°C/Watt
Tjc	Package θJC (68-pin QFN)		–	6.32	–	°C/Watt
Tjc	Package θJC (100-pin TQFP)		–	9.04	–	°C/Watt
	Pb-free assemblies (20s to 40s) – Sn-Ag-Cu solder paste reflow temperature		235	–	245	°C
	Pb-free assemblies (20s to 40s) – Sn-Pb solder paste reflow temperature		205	–	220	°C

Table 13-2. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
48-pin SSOP	MSL 1
48-pin QFN	MSL 3
68-pin QFN	MSL 3
100-pin TQFP	MSL 3

Figure 13-1. 48-pin (300 mil) SSOP Package Outline



Description Title: PSoC® 3: CY8C38 Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-11729				
*L	2938381	05/27/10	MKEA	Replaced V_{DDIO} with V_{DDD} in USBIO diagram and specification tables, added text in USBIO section of Electrical Specifications. Added Table 13-2 (Package MSL) Modified Tstorag condition and changed max spec to 100 Added bullet (Pass) under ALU (section 7.2.2.2) Added figures for kHzECO and MHzECO in the External Oscillator section Updated Figure 6-1(Clocking Subsystem diagram) Removed CPUCLK_DIV in table 5-2, Deleted Clock Divider SFR subsection Updated PSoC Creator Framework image Updated SIO DC Specifications (V_{IH} and V_{IL} parameters) Updated bullets in Clocking System and Clocking Distribution sections Updated Figure 8-2 Updated PCB Layout and Schematic, updated as per MTRB review comments Updated Table 6-3 (power changed to current) In 32kHZ EC DC Specifications table, changed I_{CC} Max to 0.25 In IMO DC Specifications table, updated Supply Current values Updated GPIO DC Specs table
*M	2958674	06/22/10	SHEA	Minor ECN to post datasheet to external website
*N	2989685	08/04/10	MKEA	INL max is changed from 16 to 32 in Table 11-20, 20-bit Delta-sigma ADC AC Specifications. Added to Table 6-6 a footnote and references to same. Added sentences to the resistive pullup and pull-down description bullets. Added sentence to Section 6.4.11, Adjustable Output Level. Updated section 5.5 External Memory Interface Updated Table 11-73 JTAG Interface AC Specifications Updated Table 11-74 SWD Interface AC Specifications Updated style changes as per the new template.
*O	3078568	11/04/10	MKEA	Added 48-SSOP pin and package details. Removed PLL output duty cycle spec. Updated "Current Digital-to-analog Converter(IDAC)" on page 81 Updated "Voltage Digital to Analog Converter (VDAC)" on page 85 Updated Table 11-2, "DC Specifications," on page 60 Updated Table 11-25, "Voltage Reference Specifications," on page 80
*P	3107314	12/10/2010	MKEA	Updated delta-sigma tables and graphs. Updated Flash AC specs Formatted table 11.2. Updated interrupt controller table Updated transimpedance amplifier section Updated SIO DC specs table Updated Voltage Monitors DC Specifications table Updated LCD Direct Drive DC specs table Replaced the Discrete Time Mixer and Continuous Time Mixer tables with Mixer DC and AC specs tables Updated ESD_{HBM} value. Updated IDAC and VDAC sections Removed ESO parts from ordering information Changed USBIO pins from NC to DNU and removed redundant USBIO pin description notes Updated POR with brown out DC and AC specs Updated PGA AC specs Updated 32 kHz External Crystal DC Specifications Updated opamp AC specs Updated XRES IO specs Updated Inductive boost regulator section Delta sigma ADC spec updates Updated comparator section Removed buzz mode from Power Mode Transition diagram Updated opamp DC and AC spec tables Updated PGA DC table