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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	67MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x20b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	48-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3866pvi-047

It also contains a separate, very low-power internal low-speed oscillator (ILO) for the sleep and watchdog timers. A 32.768-kHz external watch crystal is also supported for use in real-time clock (RTC) applications. The clocks, together with programmable clock dividers, provide the flexibility to integrate most timing requirements.

The CY8C38 family supports a wide supply operating range from 1.71 V to 5.5 V. This allows operation from regulated supplies such as 1.8 V ± 5%, 2.5 V ±10%, 3.3 V ± 10%, or 5.0 V ± 10%, or directly from a wide range of battery types. In addition, it provides an integrated high efficiency synchronous boost converter that can power the device from supply voltages as low as 0.5 V. This enables the device to be powered directly from a single battery or solar cell. In addition, you can use the boost converter to generate other voltages required by the device, such as a 3.3-V supply for LCD glass drive. The boost's output is available on the Vboost pin, allowing other devices in the application to be powered from the PSoC.

PSoC supports a wide range of low-power modes. These include a 200-nA hibernate mode with RAM retention and a 1-µA sleep mode with RTC. In the second mode, the optional 32.768-kHz watch crystal runs continuously and maintains an accurate RTC.

Power to all major functional blocks, including the programmable digital and analog peripherals, can be controlled independently by firmware. This allows low-power background processing when some peripherals are not in use. This, in turn, provides a total device current of only 1.2 mA when the CPU is running at 6 MHz, or 0.8 mA running at 3 MHz.

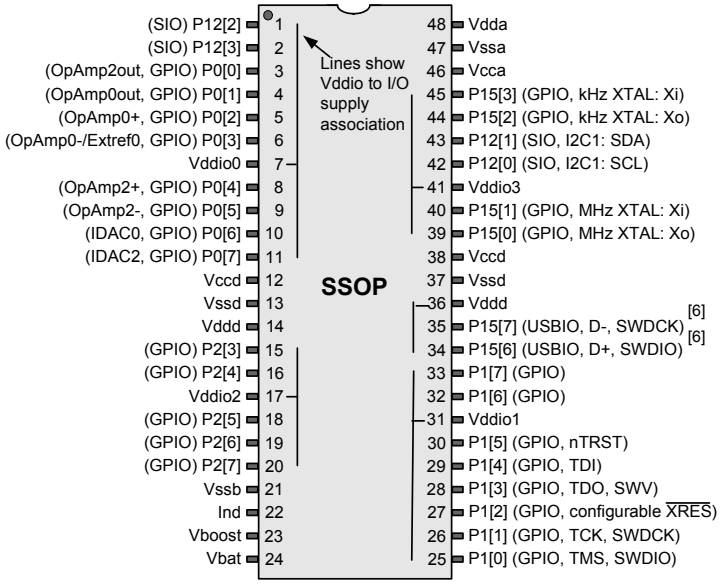
The details of the PSoC power modes are covered in the "Power System" section on page 24 of this datasheet.

PSoC uses JTAG (4-wire) or SWD (2-wire) interfaces for programming, debug, and test. The 1-wire SWV may also be used for 'printf' style debugging. By combining SWD and SWV, you can implement a full debugging interface with just three pins. Using these standard interfaces you can debug or program the PSoC with a variety of hardware solutions from Cypress or third party vendors. PSoC supports on-chip break points and 4-KB instruction and data race memory for debug. Details of the programming, test, and debugging interfaces are discussed in the "Programming, Debug Interfaces, Resources" section on page 56 of this datasheet.

2. Pinouts

The Vddio pin that supplies a particular set of pins is indicated by the black lines drawn on the pinout diagrams in Figure 2-1 through Figure 2-4. Using the Vddio pins, a single PSoC can support multiple interface voltage levels, eliminating the need for off-chip level shifters. Each Vddio may sink up to 100 mA total to its associated I/O pins and opamps. On the 68-pin and 100-pin devices each set of Vddio associated pins may sink up to 100 mA. The 48-pin device may sink up to 100 mA total for all Vddio0 plus Vddio2 associated I/O pins and 100 mA total for all Vddio1 plus Vddio3 associated I/O pins.

Figure 2-1. 48-pin SSOP Part Pinout



Note
6. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.

TMS

JTAG test mode select programming and debug port connection.

USBIO, D+

Provides D+ connection directly to a USB 2.0 bus. May be used as a digital I/O pin; it is powered from V_{DDD} instead of from a Vddio. Pins are Do Not Use (DNU) on devices without USB.

USBIO, D–

Provides D– connection directly to a USB 2.0 bus. May be used as a digital I/O pin; it is powered from V_{DDD} instead of from a Vddio. Pins are Do Not Use (DNU) on devices without USB.

Vboost

Power sense connection to boost pump.

Vbat

Battery supply to boost pump.

Vcca

Output of analog core regulator and input to analog core. Requires a 1-µF capacitor to V_{SSA}. Regulator output not for external use.

Vccd

Output of digital core regulator and input to digital core. The two V_{CCD} pins must be shorted together, with the trace between them as short as possible, and a 1-µF capacitor to V_{SSD}; see Power System on page 24. Regulator output not for external use.

Vdda

Supply for all analog peripherals and analog core regulator. **Vdda must be the highest voltage present on the device. All other supply pins must be less than or equal to Vdda.**

Vddd

Supply for all digital peripherals and digital core regulator. Vddd must be less than or equal to Vdda.

Vssa

Ground for all analog peripherals.

Vssb

Ground connection for boost pump.

Vssd

Ground for all digital logic and I/O pins.

Vddio0, Vddio1, Vddio2, Vddio3

Supply for I/O pins. Each Vddio must be tied to a valid operating voltage (1.71 V to 5.5 V), and must be less than or equal to Vdda. If the I/O pins associated with Vddio0, Vddio2, or Vddio3 are not used then that Vddio should be tied to ground (Vssd or Vssa).

$\overline{\text{XRES}}$ (and configurable $\overline{\text{XRES}}$)

External reset pin. Active low with internal pull-up. In 48-pin SSOP parts and 48-pin QFN parts, P1[2] may be configured as $\overline{\text{XRES}}$. In all other parts the pin is configured as a GPIO.

4. CPU

4.1 8051 CPU

The CY8C38 devices use a single cycle 8051 CPU, which is fully compatible with the original MCS-51 instruction set. The CY8C38 family uses a pipelined RISC architecture, which executes most instructions in 1 to 2 cycles to provide peak performance of up to 33 MIPS with an average of 2 cycles per instruction. The single cycle 8051 CPU runs ten times faster than a standard 8051 processor.

The 8051 CPU subsystem includes these features:

- Single cycle 8051 CPU
- Up to 64 KB of flash memory, up to 2 KB of EEPROM, and up to 8 KB of SRAM
- Programmable nested vector interrupt controller
- DMA controller
- Peripheral HUB (PHUB)
- External memory interface (EMIF)

4.2 Addressing Modes

The following addressing modes are supported by the 8051:

- Direct Addressing: The operand is specified by a direct 8-bit address field. Only the internal RAM and the SFRs can be accessed using this mode.
- Indirect Addressing: The instruction specifies the register which contains the address of the operand. The registers R0 or R1 are used to specify the 8-bit address, while the data pointer (DPTR) register is used to specify the 16-bit address.
- Register Addressing: Certain instructions access one of the registers (R0 to R7) in the specified register bank. These instructions are more efficient because there is no need for an address field.
- Register Specific Instructions: Some instructions are specific to certain registers. For example, some instructions always act on the accumulator. In this case, there is no need to specify the operand.
- Immediate Constants: Some instructions carry the value of the constants directly instead of an address.
- Indexed Addressing: This type of addressing can be used only for a read of the program memory. This mode uses the Data Pointer as the base and the accumulator value as an offset to read a program memory.
- Bit Addressing: In this mode, the operand is one of 256 bits.

4.3 Instruction Set

The 8051 instruction set is highly optimized for 8-bit handling and Boolean operations. The types of instructions supported include:

- Arithmetic instructions
- Logical instructions
- Data transfer instructions
- Boolean instructions
- Program branching instructions

4.3.1 Instruction Set Summary

4.3.1.1 Arithmetic Instructions

Arithmetic instructions support the direct, indirect, register, immediate constant, and register-specific instructions. Arithmetic modes are used for addition, subtraction, multiplication, division, increment, and decrement operations. Table 4-1 lists the different arithmetic instructions.

Table 4-1. Arithmetic Instructions

Mnemonic	Description	Bytes	Cycles
ADD A,Rn	Add register to accumulator	1	1
ADD A,Direct	Add direct byte to accumulator	2	2
ADD A,@Ri	Add indirect RAM to accumulator	1	2
ADD A,#data	Add immediate data to accumulator	2	2
ADDC A,Rn	Add register to accumulator with carry	1	1
ADDC A,Direct	Add direct byte to accumulator with carry	2	2
ADDC A,@Ri	Add indirect RAM to accumulator with carry	1	2
ADDC A,#data	Add immediate data to accumulator with carry	2	2
SUBB A,Rn	Subtract register from accumulator with borrow	1	1
SUBB A,Direct	Subtract direct byte from accumulator with borrow	2	2
SUBB A,@Ri	Subtract indirect RAM from accumulator with borrow	1	2
SUBB A,#data	Subtract immediate data from accumulator with borrow	2	2
INC A	Increment accumulator	1	1
INC Rn	Increment register	1	2
INC Direct	Increment direct byte	2	3
INC @Ri	Increment indirect RAM	1	3
DEC A	Decrement accumulator	1	1
DEC Rn	Decrement register	1	2
DEC Direct	Decrement direct byte	2	3
DEC @Ri	Decrement indirect RAM	1	3
INC DPTR	Increment data pointer	1	1
MUL	Multiply accumulator and B	1	2
DIV	Divide accumulator by B	1	6
DAA	Decimal adjust accumulator	1	3

4.3.1.2 Logical Instructions

The logical instructions perform Boolean operations such as AND, OR, XOR on bytes, rotate of accumulator contents, and swap of nibbles in an accumulator. The Boolean operations on the bytes are performed on the bit-by-bit basis. Table 4-2 shows the list of logical instructions and their description.

Table 4-2. Logical Instructions

Mnemonic	Description	Bytes	Cycles
ANL A,Rn	AND register to accumulator	1	1
ANL A,Direct	AND direct byte to accumulator	2	2
ANL A,@Ri	AND indirect RAM to accumulator	1	2
ANL A,#data	AND immediate data to accumulator	2	2
ANL Direct, A	AND accumulator to direct byte	2	3

6.2.1 Power Modes

PSoC 3 devices have four different power modes, as shown in Table 6-2 and Table 6-3. The power modes allow a design to easily provide required functionality and processing power while simultaneously minimizing power consumption and maximizing battery life in low-power and portable devices.

PSoC 3 power modes, in order of decreasing power consumption are:

- Active
- Alternate Active
- Sleep
- Hibernate

Active is the main processing mode. Its functionality is configurable. Each power controllable subsystem is enabled or disabled by using separate power configuration template registers. In alternate active mode, fewer subsystems are enabled, reducing power. In sleep mode most resources are disabled regardless of the template settings. Sleep mode is optimized to provide timed sleep intervals and Real Time Clock functionality. The lowest power mode is hibernate, which retains register and SRAM state, but no clocks, and allows wakeup only from I/O pins. Figure 6-5 on page 26 illustrates the allowable transitions between power modes

Table 6-2. Power Modes

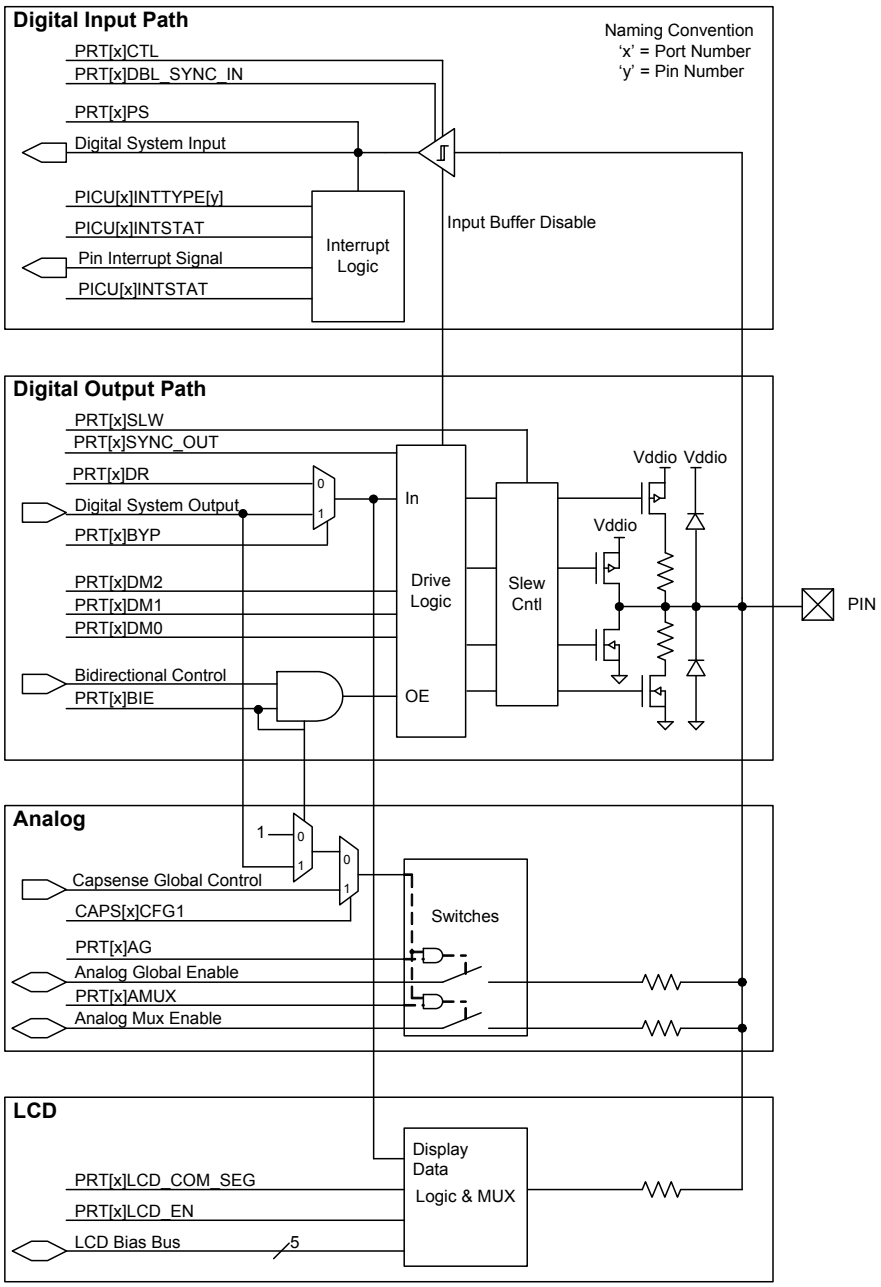
Power Modes	Description	Entry Condition	Wakeup Source	Active Clocks	Regulator
Active	Primary mode of operation, all peripherals available (programmable)	Wakeup, reset, manual register entry	Any interrupt	Any (programmable)	All regulators available. Digital and analog regulators can be disabled if external regulation used.
Alternate Active	Similar to Active mode, and is typically configured to have fewer peripherals active to reduce power. One possible configuration is to use the UDBs for processing, with the CPU turned off	Manual register entry	Any interrupt	Any (programmable)	All regulators available. Digital and analog regulators can be disabled if external regulation used.
Sleep	All subsystems automatically disabled	Manual register entry	Comparator, PICU, I^2C, RTC, CTW, LVD	ILO/kHzECO	Both digital and analog regulators buzzed. Digital and analog regulators can be disabled if external regulation used.
Hibernate	All subsystems automatically disabled Lowest power consuming mode with all peripherals and internal regulators disabled, except hibernate regulator is enabled Configuration and memory contents retained	Manual register entry	PICU		Only hibernate regulator active.

Table 6-3. Power Modes Wakeup Time and Power Consumption

Sleep Modes	Wakeup Time	Current (typ)	Code Execution	Digital Resources	Analog Resources	Clock Sources Available	Wakeup Sources	Reset Sources
Active	–	1.2 mA[13]	Yes	All	All	All	–	All
Alternate Active	–	–	User defined	All	All	All	–	All
Sleep	<15 µs	1 µA	No	I^2C	Comparator	ILO/kHzECO	Comparator, PICU, I^2C, RTC, CTW, LVD	XRES, LVD, WDR
Hibernate	<100 µs	200 nA	No	None	None	None	PICU	XRES

Note
13. Bus clock off. Execute from CPU instruction buffer at 6 MHz. See Table 11-2 on page 60.

Figure 6-8. GPIO Block Diagram



6.4.15 Over Voltage Tolerance

All I/O pins provide an over voltage tolerance feature at any operating V_{DD}.

- There are no current limitations for the SIO pins as they present a high impedance load to the external circuit where Vddio ≤ V_{IN} ≤ 5.5 V.
- The GPIO pins must be limited to 100 µA using a current limiting resistor. GPIO pins clamp the pin voltage to approximately one diode above the Vddio supply where Vddio ≤ V_{IN} ≤ V_{DDA}.
- In case of a GPIO pin configured for analog input/output, the analog voltage on the pin must not exceed the Vddio supply voltage to which the GPIO belongs.

A common application for this feature is connection to a bus such as I^2C where different devices are running from different supply voltages. In the I^2C case, the PSoC chip is configured into the Open Drain, Drives Low mode for the SIO pin. This allows an external pull-up to pull the I^2C bus voltage above the PSoC pin supply. For example, the PSoC chip could operate at 1.8 V, and an external device could run from 5 V. Note that the SIO pin's V_{IH} and V_{IL} levels are determined by the associated Vddio supply pin. The I/O pin must be configured into a high impedance drive mode, open drain low drive mode, or pull-down drive mode, for over voltage tolerance to work properly. Absolute maximum ratings for the device must be observed for all I/O pins.

6.4.16 Reset Configuration

While reset is active all I/Os are reset to and held in the High Impedance Analog state. After reset is released, the state can be reprogrammed on a port-by-port basis to pull-down or pull-up. To ensure correct reset operation, the port reset configuration data is stored in special nonvolatile registers. The stored reset data is automatically transferred to the port reset configuration registers at reset release.

6.4.17 Low-Power Functionality

In all low-power modes the I/O pins retain their state until the part is awakened and changed or reset. To awaken the part, use a pin interrupt, because the port interrupt logic continues to function in all low-power modes.

6.4.18 Special Pin Functionality

Some pins on the device include additional special functionality in addition to their GPIO or SIO functionality. The specific special function pins are listed in Pinouts on page 5. The special features are:

- Digital
  - 4- to 33-MHz crystal oscillator
  - 32.768-kHz crystal oscillator
  - Wake from sleep on I^2C address match. Any pin can be used for I^2C if wake from sleep is not required.
  - JTAG interface pins
  - SWD interface pins
  - SWV interface pins
  - External reset
- Analog
  - Opamp inputs and outputs
  - High current IDAC outputs
  - External reference inputs

6.4.19 JTAG Boundary Scan

The device supports standard JTAG boundary scan chains on all I/O pins for board level test.

7. Digital Subsystem

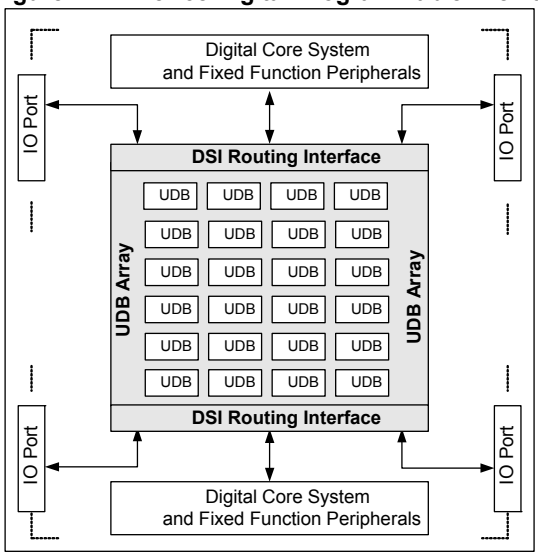
The digital programmable system creates application specific combinations of both standard and advanced digital peripherals and custom logic functions. These peripherals and logic are then interconnected to each other and to any pin on the device, providing a high level of design flexibility and IP security.

The features of the digital programmable system are outlined here to provide an overview of capabilities and architecture. You do not need to interact directly with the programmable digital system at the hardware and register level. PSoC Creator provides a high level schematic capture graphical interface to automatically place and route resources similar to PLDs.

The main components of the digital programmable system are:

- UDB – These form the core functionality of the digital programmable system. UDBs are a collection of uncommitted logic (PLD) and structural logic (Datapath) optimized to create all common embedded peripherals and customized functionality that are application or design specific.
- Universal digital block array – UDB blocks are arrayed within a matrix of programmable interconnect. The UDB array structure is homogeneous and allows for flexible mapping of digital functions onto the array. The array supports extensive and flexible routing interconnects between UDBs and the Digital System Interconnect.
- Digital system interconnect (DSI) – Digital signals from UDBs, fixed function peripherals, I/O pins, interrupts, DMA, and other system core signals are attached to the digital system interconnect to implement full featured device connectivity. The DSI allows any digital function to any pin or other feature routability when used with the universal digital block array.

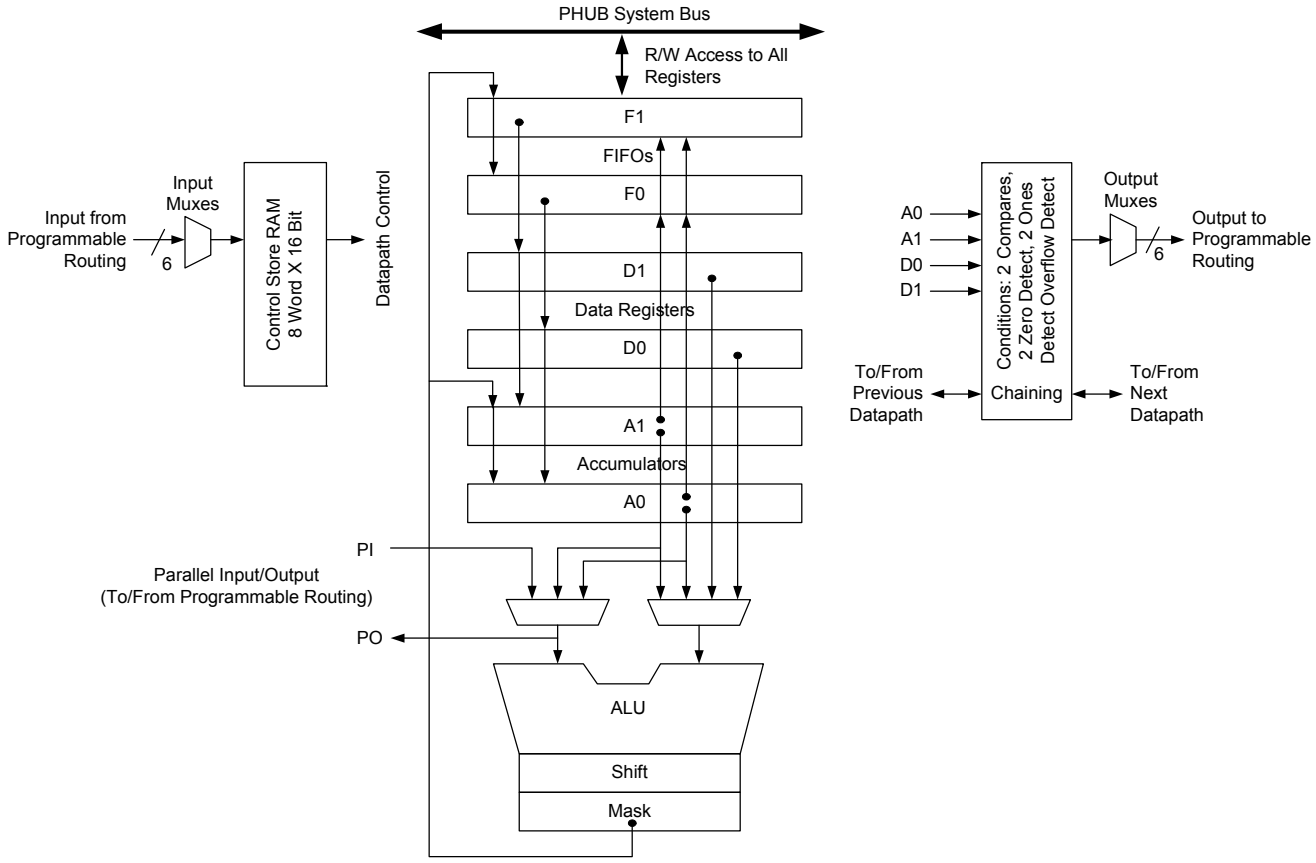
Figure 7-1. CY8C38 Digital Programmable Architecture



7.2.2 Datapath Module

The datapath contains an 8-bit single cycle ALU, with associated compare and condition generation logic. This datapath block is optimized to implement embedded functions, such as timers, counters, integrators, PWMs, PRS, CRC, shifters and dead band generators and many others.

Figure 7-8. Datapath Top Level



7.2.2.1 Working Registers

The datapath contains six primary working registers, which are accessed by CPU firmware or DMA during normal operation.

Table 7-1. Working Datapath Registers

Name	Function	Description
A0 and A1	Accumulators	These are sources and sinks for the ALU and also sources for the compares.
D0 and D1	Data Registers	These are sources for the ALU and sources for the compares.
F0 and F1	FIFOs	These are the primary interface to the system bus. They can be a data source for the data registers and accumulators or they can capture data from the accumulators or ALU. Each FIFO is four bytes deep.

7.2.2.2 Dynamic Datapath Configuration RAM

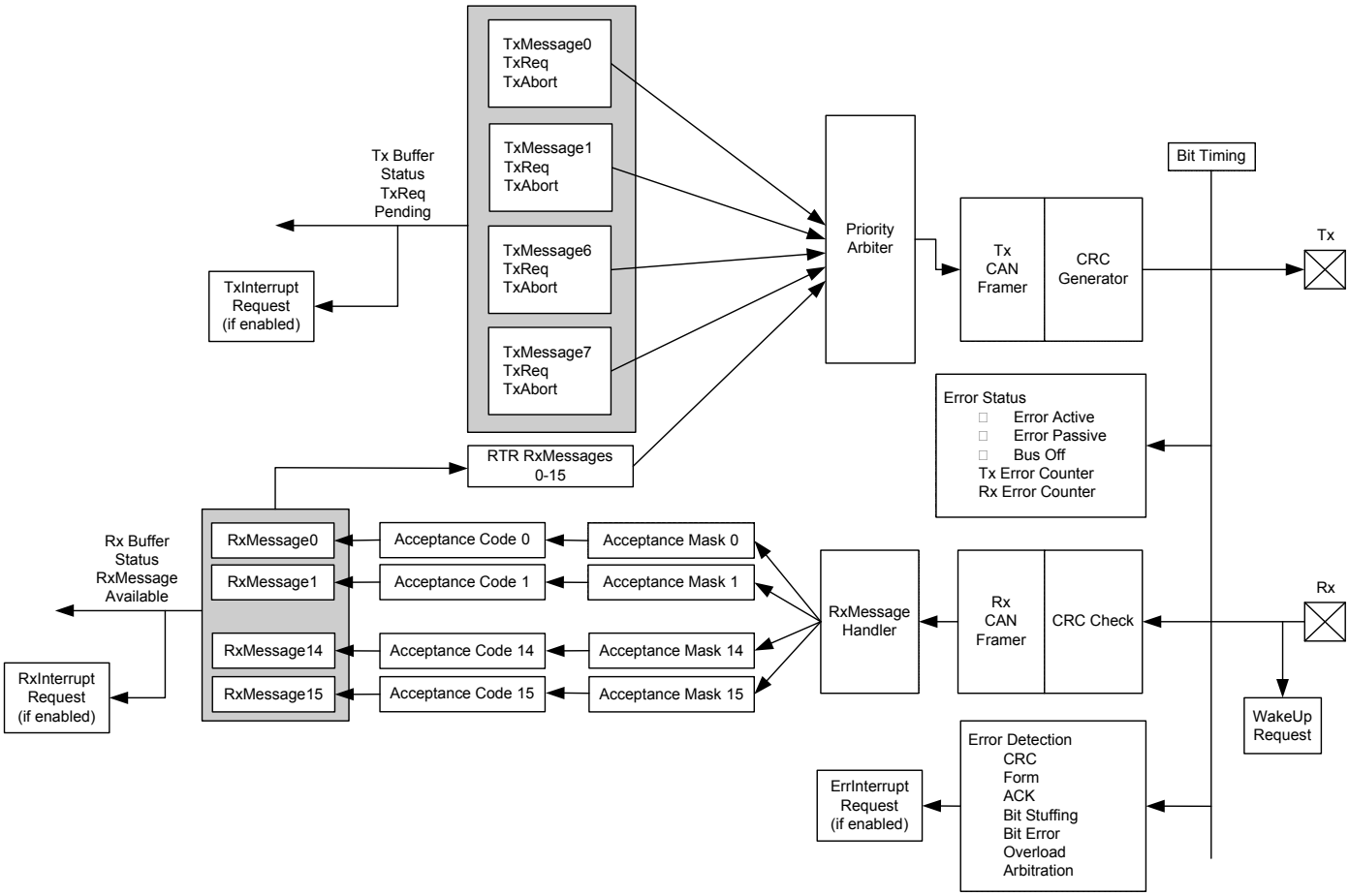
Dynamic configuration is the ability to change the datapath function and internal configuration on a cycle-by-cycle basis, under sequencer control. This is implemented using the 8-word × 16-bit configuration RAM, which stores eight unique 16-bit wide configurations. The address input to this RAM controls the sequence, and can be routed from any block connected to the UDB routing matrix, most typically PLD logic, I/O pins, or from the outputs of this or other datapath blocks.

ALU

The ALU performs eight general purpose functions. They are:

- Increment
- Decrement
- Add
- Subtract
- Logical AND
- Logical OR
- Logical XOR
- Pass, used to pass a value through the ALU to the shift register, mask, or another UDB register.

Figure 7-19. CAN Controller Block Diagram



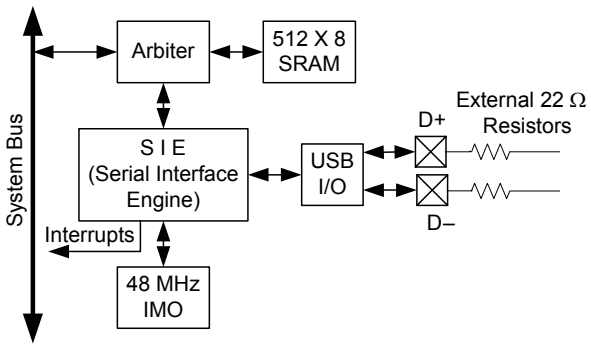
7.6 USB

PSoC includes a dedicated Full-Speed (12 Mbps) USB 2.0 transceiver supporting all four USB transfer types: control, interrupt, bulk, and isochronous. PSoC Creator provides full configuration support. USB interfaces to hosts through two dedicated USBIO pins, which are detailed in the "I/O System and Routing" section on page 28.

USB includes the following features:

- Eight unidirectional data endpoints
- One bidirectional control endpoint 0 (EP0)
- Shared 512-byte buffer for the eight data endpoints
- Dedicated 8-byte buffer for EP0
- Three memory modes
  - Manual memory management with no DMA access
  - Manual memory management with manual DMA access
  - Automatic memory management with automatic DMA access
- Internal 3.3-V regulator for transceiver
- Internal 48-MHz main oscillator mode that auto locks to USB bus clock, requiring no external crystal for USB (USB equipped parts only)
- Interrupts on bus and each endpoint event, with device wakeup
- USB reset, suspend, and resume operations
- Bus-powered and self-powered modes

Figure 7-20. USB



8.11.1 Down Mixer

The SC/CT block can be used as a mixer to down convert an input signal. This circuit is a high bandwidth passive sample network that can sample input signals up to 14 MHz. This sampled value is then held using the opamp with a maximum clock rate of 4 MHz. The output frequency is at the difference between the input frequency and the highest integer multiple of the Local Oscillator that is less than the input.

8.11.2 First Order Modulator – SC Mode

A first order modulator is constructed by placing the SC/CT block in an integrator mode and using a comparator to provide a 1-bit feedback to the input. Depending on this bit, a reference voltage is either subtracted or added to the input signal. The block output is the output of the comparator and not the integrator in the modulator case. The signal is downshifted and buffered and then processed by a decimator to make a delta-sigma converter or a counter to make an incremental converter. The accuracy of the sampled data from the first-order modulator is determined from several factors.

The main application for this modulator is for a low-frequency ADC with high accuracy. Applications include strain gauges, thermocouples, precision voltage, and current measurement.

9. Programming, Debug Interfaces, Resources

PSoC devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware. Three interfaces are available: JTAG, SWD, and SWV. JTAG and SWD support all programming and debug features of the device. JTAG also supports standard JTAG scan chains for board level test and chaining multiple JTAG devices to a single JTAG connection.

Complete Debug on Chip (DoC) functionality enables full device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE software provides fully integrated programming and debug support for PSoC devices. The low cost MiniProg3 programmer and debugger is designed to provide full programming and debug support of PSoC devices in conjunction with the PSoC Creator IDE. PSoC JTAG, SWD, and SWV interfaces are fully compatible with industry standard third party tools.

All DOC circuits are disabled by default and can only be enabled in firmware. If not enabled, the only way to reenable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables DOC. Disabling DOC features, robust flash protection, and hiding custom analog and digital functionality inside the PSoC device provide a level of security not possible with multichip application solutions. Additionally, all device interfaces can be permanently disabled (Device Security) for applications concerned about phishing attacks due to a maliciously reprogrammed device. Permanently disabling interfaces is not recommended in most applications because you cannot access the device later. Because all programming, debug, and test interfaces are disabled when device security is enabled, PSoCs with Device Security enabled may not be returned for failure analysis.

Table 9-1. Debug Configurations

Debug and Trace Configuration	GPIO Pins Used
All debug and trace disabled	0
JTAG	4 or 5
SWD	2
SWV	1
SWD + SWV	3

9.1 JTAG Interface

The IEEE 1149.1 compliant JTAG interface exists on four or five pins (the nTRST pin is optional). The JTAG clock frequency can be up to 8 MHz, or 1/3 of the CPU clock frequency for 8 and 16-bit transfers, or 1/5 of the CPU clock frequency for 32-bit transfers, whichever is least. By default, the JTAG pins are enabled on new devices but the JTAG interface can be disabled, allowing these pins to be used as General Purpose I/O (GPIO) instead. The JTAG interface is used for programming the flash memory, debugging, I/O scan chains, and JTAG device chaining.

9.2 Serial Wire Debug Interface

The SWD interface is the preferred alternative to the JTAG interface. It requires only two pins instead of the four or five needed by JTAG. SWD provides all of the programming and debugging features of JTAG at the same speed. SWD does not provide access to scan chains or device chaining. The SWD clock frequency can be up to 1/3 of the CPU clock frequency.

SWD uses two pins, either two of the JTAG pins (TMS and TCK) or the USBIO D+ and D– pins. The USBIO pins are useful for in system programming of USB solutions that would otherwise require a separate programming connector. One pin is used for the data clock and the other is used for data input and output. SWD can be enabled on only one of the pin pairs at a time. This only happens if, within 8 µs (key window) after reset, that pin pair (JTAG or USB) receives a predetermined sequence of 1s and 0s. SWD is used for debugging or for programming the flash memory.

The SWD interface can be enabled from the JTAG interface or disabled, allowing its pins to be used as GPIO. Unlike JTAG, the SWD interface can always be reacquired on any device during the key window. It can then be used to reenable the JTAG interface, if desired. When using SWD or JTAG pins as standard GPIO, make sure that the GPIO functionality and PCB circuits do not interfere with SWD or JTAG use.

10. Development Support

The CY8C38 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit psoc.cypress.com/getting-started to find out more.

10.1 Documentation

A suite of documentation, supports the CY8C38 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component datasheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers.

10.2 Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

10.3 Tools

With industry standard cores, programming, and debugging interfaces, the CY8C38 family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Table 11-6. Inductive Boost Regulator DC Specifications *(continued)*

Unless otherwise specified, operating conditions are: V_{BAT} = 2.4 V, V_{OUT} = 2.7 V, I_{OUT} = 40 mA, F_{SW} = 400 kHz, L_{BOOST} = 22 µH, C_{BOOST} = 22 µF || 0.1 µF

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OUT}	Boost voltage range[27, 28]					
	1.8 V		1.71	1.80	1.89	V
	1.9 V		1.81	1.90	2.00	V
	2.0 V		1.90	2.00	2.10	V
	2.4 V		2.28	2.40	2.52	V
	2.7 V		2.57	2.70	2.84	V
	3.0 V		2.85	3.00	3.15	V
	3.3 V		3.14	3.30	3.47	V
	3.6 V		3.42	3.60	3.78	V
	5.0 V	External diode required	4.75	5.00	5.25	V
Reg_{LOAD}	Load regulation		–	–	3.8	%
Reg_{LINE}	Line regulation		–	–	4.1	%
η_{OUT}	Efficiency	L_{BOOST} = 10 µH	70	85	–	%
		L_{BOOST} = 22 µH	82	90	–	%

Table 11-7. Inductive Boost Regulator AC Specifications

Unless otherwise specified, operating conditions are: V_{BAT} = 2.4 V, V_{OUT} = 2.7 V, I_{OUT} = 40 mA, F_{SW} = 400 kHz, L_{BOOST} = 22 µH, C_{BOOST} = 22 µF || 0.1 µF.

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{RIPPLE}	Ripple voltage (peak-to-peak)	V_{OUT} = 1.8 V, F_{SW} = 400 kHz, I_{OUT} = 10 mA	–	–	100	mV
F_{SW}	Switching frequency		–	0.1, 0.4, or 2	–	MHz

Table 11-8. Recommended External Components for Boost Circuit

Parameter	Description	Conditions	Min	Typ	Max	Units
L_{BOOST}	Boost inductor		4.7	10	47	µH
C_{BOOST}	Filter capacitor[27]		10	22	47	µF
I_F	External Schottky diode average forward current	External Schottky diode is required for V_{OUT} > 3.6 V	1	–	–	A
V_R			20	–	–	V

Notes
27. Based on device characterization (Not production tested).
28. At boost frequency of 2 MHz, Vboost is limited to 2 x Vbat. At 400 kHz, Vboost is limited to 4 x Vbat.

11.5.2 Delta-sigma ADC

Unless otherwise specified, operating conditions are:

- Operation in continuous sample mode
- fclk = 3.072 MHz for resolution = 16 to 20 bits; fclk = 6.144 MHz for resolution = 8 to 15 bits
- Reference = 1.024 V internal reference bypassed on P3.2 or P0.3
- Unless otherwise specified, all charts and graphs show typical values

Table 11-20. 20-bit Delta-sigma ADC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		8	–	20	bits
	Number of channels, single ended		–	–	No. of GPIO	–
	Number of channels, differential	Differential pair is formed using a pair of GPIOs.	–	–	No. of GPIO/2	–
	Monotonic	Yes	–	–	–	–
Ge	Gain error	Buffered, buffer gain = 1, modulator gain = 1, 16-bit mode, 25 °C	–	–	±0.2	%
Gd	Gain drift	Buffered, buffer gain = 1, modulator gain = 1, 16-bit mode	–	–	50	ppm/°C
Vos	Input offset voltage	Buffered	–	–	±0.1	mV
TCVos	ADC TC input offset voltage	Temperature coefficient, input offset voltage	–	–	55	µV/°C
	Input voltage range, single ended[33]		V_{SSA}	–	V_{DDA}	V
	Input voltage range, differential unbuffered[33]		V_{SSA}	–	V_{DDA}	V
	Input voltage range, differential, buffered[33]		V_{SSA}	–	$V_{DDA} – 1$	V
PSRRb	Power supply rejection ratio, buffered[33]	Buffer gain = 1, 16-bit, Range = ±1.024 V	90	–	–	dB
CMRRb	Common mode rejection ratio, buffered[33]	Buffer gain = 1, 16 bit, Range = ±1.024 V	85	–	–	dB
INL20	Integral non linearity[33]	Range = ±1.024 V, unbuffered	–	–	±32	LSB
DNL20	Differential non linearity[33]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
INL16	Integral non linearity[33]	Range = ±1.024 V, unbuffered	–	–	±2	LSB
DNL16	Differential non linearity[33]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
INL12	Integral non linearity[33]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
DNL12	Differential non linearity[33]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
INL8	Integral non linearity[33]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
DNL8	Differential non linearity[33]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
Rin_Buff	ADC input resistance	Input buffer used	10	–	–	MΩ
Rin_ADC16	ADC input resistance	Input buffer bypassed, 16-bit, Range = ±1.024 V	–	74[34]	–	kΩ
Rin_ADC12	ADC input resistance	Input buffer bypassed, 12 bit, Range = ±1.024 V	–	148[34]	–	kΩ
Cin_G1	ADC input capacitance[33]	Gain = 1	–	5	–	pF

Notes

33. Based on device characterization (not production tested).
34. By using switched capacitors at the ADC input an effective input resistance is created. Holding the gain and number of bits constant, the resistance is proportional to the inverse of the clock frequency. This value is calculated, not measured. For more information see the Technical Reference Manual.

11.5.3 Voltage Reference

Table 11-25. Voltage Reference Specifications

See also ADC external reference specifications in *Section 11.5.2*.

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{REF}	Precision reference voltage	Initial trimming	1.023 (–0.1%)	1.024	1.025 (+0.1%)	V
	Temperature drift[36]		–	–	20	ppm/°C
	Long term drift		–	100	–	ppm/Khr
	Thermal cycling drift (stability)[36]		–	100	–	ppm

11.5.4 Analog Globals

Table 11-26. Analog Globals Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Rppag	Resistance pin-to-pin through analog global[37]	V_{DDA} = 3.0 V	–	939	1461	Ω
Rppmuxbus	Resistance pin-to-pin through analog mux bus[37]	V_{DDA} = 3.0 V	–	721	1135	Ω

11.5.5 Comparator

Table 11-27. Comparator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OS}	Input offset voltage in fast mode	Factory trim, Vdda > 2.7 V, Vin ≥ 0.5 V	–		10	mV
	Input offset voltage in slow mode	Factory trim, Vin ≥ 0.5 V	–		9	mV
V_{OS}	Input offset voltage in fast mode[38]	Custom trim	–	–	4	mV
	Input offset voltage in slow mode[38]	Custom trim	–	–	4	mV
V_{OS}	Input offset voltage in ultra low-power mode		–	±12	–	mV
V_{HYST}	Hysteresis	Hysteresis enable mode	–	10	32	mV
V_{ICM}	Input common mode voltage	High current / fast mode	V_{SSA}	–	V_{DDA} – 0.1	V
		Low current / slow mode	V_{SSA}	–	V_{DDA}	V
		Ultra low power mode	V_{SSA}	–	V_{DDA} – 0.9	V
CMRR	Common mode rejection ratio		–	50	–	dB
I_{CMP}	High current mode/fast mode[36]		–	–	400	µA
	Low current mode/slow mode[36]		–	–	100	µA
	Ultra low-power mode[36]		–	6	–	µA

Notes
36. Based on device characterization (Not production tested).
37. The resistance of the analog global and analog mux bus is high if $V_{DDA} \leq 2.7$ V, and the chip is in either sleep or hibernate mode. Use of analog global and analog mux bus under these conditions is not recommended.
38. The recommended procedure for using a custom trim value for the on-chip comparators can be found in the TRM.

Table 11-29. IDAC DC Specifications *(continued)*

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	Operating current, code = 0	Slow mode, source mode, range = 31.875 µA	–	–	44	µA
		Slow mode, source mode, range = 255 µA,	–	–	33	µA
		Slow mode, source mode, range = 2.04 mA	–	–	33	µA
		Slow mode, sink mode, range = 31.875 µA	–	–	36	µA
		Slow mode, sink mode, range = 255 µA	–	–	33	µA
		Slow mode, sink mode, range = 2.04 mA	–	–	33	µA
		Fast mode, source mode, range = 31.875 µA	–	–	310	µA
		Fast mode, source mode, range = 255 µA	–	–	305	µA
		Fast mode, source mode, range = 2.04 mA	–	–	305	µA
		Fast mode, sink mode, range = 31.875 µA	–	–	310	µA
		Fast mode, sink mode, range = 255 µA	–	–	300	µA
		Fast mode, sink mode, range = 2.04 mA	–	–	300	µA

Figure 11-25. IDAC INL vs Input Code, Range = 255 µA, Source Mode

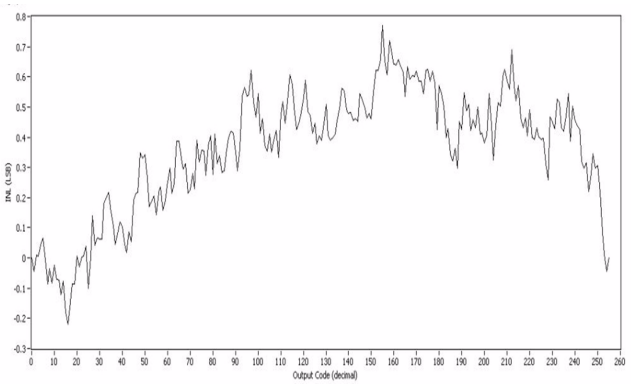
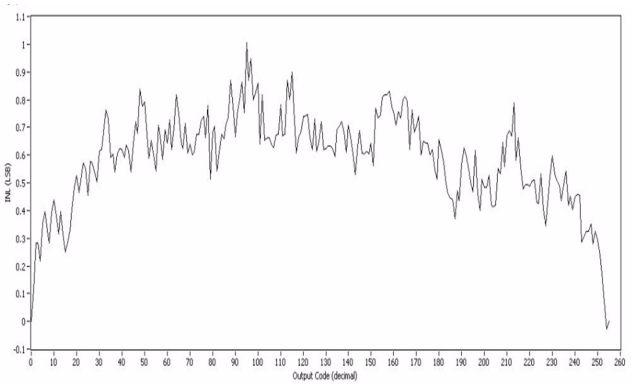


Figure 11-26. IDAC INL vs Input Code, Range = 255 µA, Sink Mode



11.5.10 Programmable Gain Amplifier

The PGA is created using a SC/CT analog block; see the PGA component datasheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, operating conditions are:

- Operating temperature = 25 °C for typical values
- Unless otherwise specified, all charts and graphs show typical values

Table 11-37. PGA DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vin	Input voltage range	Power mode = minimum	Vssa	–	Vdda	V
Vos	Input offset voltage	Power mode = high, gain = 1	–	–	10	mV
TCVos	Input offset voltage drift with temperature	Power mode = high, gain = 1	–	–	±30	µV/°C
Ge1	Gain error, gain = 1		–	–	±0.15	%
Ge16	Gain error, gain = 16		–	–	±2.5	%
Ge50	Gain error, gain = 50		–	–	±5	%
Vonl	DC output nonlinearity	Gain = 1	–	–	±0.01	% of FSR
Cin	Input capacitance		–	–	7	pF
Voh	Output voltage swing	Power mode = high, gain = 1, Rload = 100 kΩ to V_{DDA} / 2	V_{DDA} – 0.15	–	–	V
Vol	Output voltage swing	Power mode = high, gain = 1, Rload = 100 kΩ to V_{DDA} / 2	–	–	V_{SSA} + 0.15	V
Vsrc	Output voltage under load	Iload = 250 µA, Vdda ≥ 2.7V, power mode = high	–	–	300	mV
Idd	Operating current	Power mode = high	–	1.5	1.65	mA
PSRR	Power supply rejection ratio		48	–	–	dB

Figure 11-43. Voffset Histogram, 1000 Samples, Vdda = 5 V

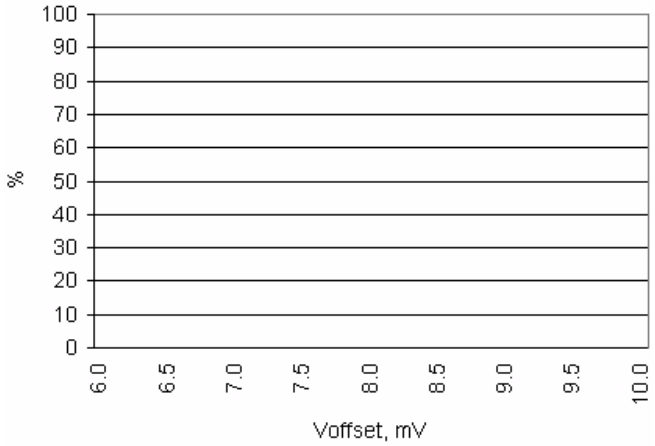


Figure 11-51. Synchronous Write Cycle Timing

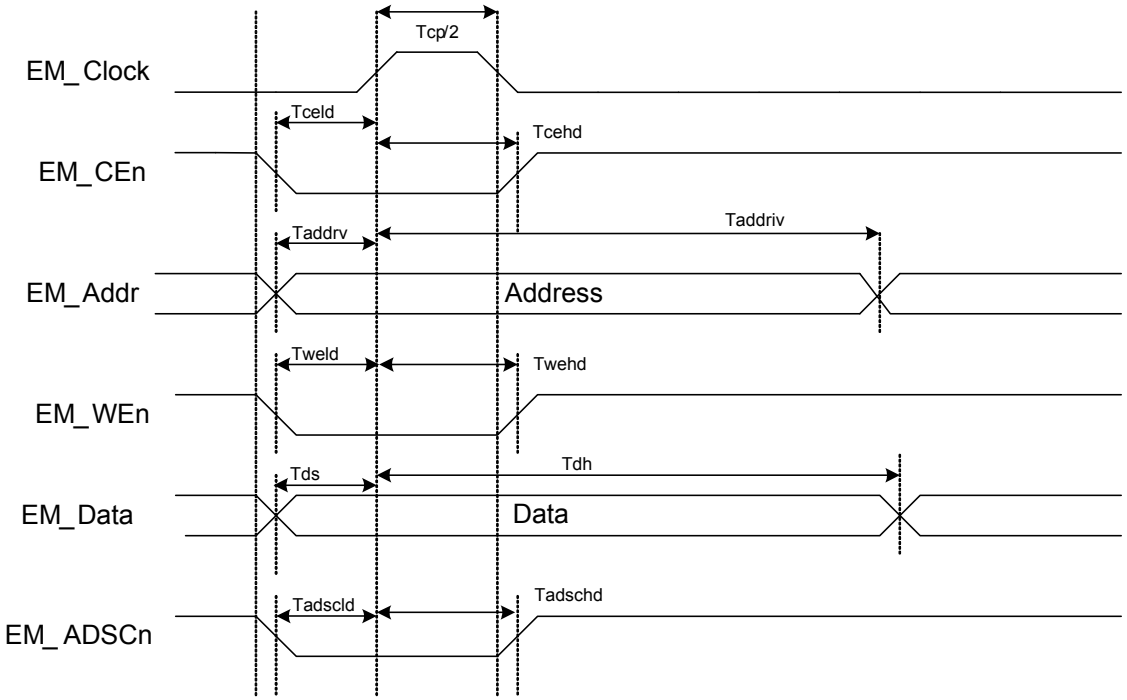


Table 11-66. Synchronous Write Cycle Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T	EMIF clock Period[45]	Vdda ≥ 3.3 V	30.3	–	–	nS
Tcp/2	EM_Clock pulse high		T/2	–	–	nS
Tceld	EM_CEn low to EM_Clock high		5	–	–	nS
Tcehd	EM_Clock high to EM_CEn high		T/2 – 5	–	–	nS
Taddrv	EM_Addr valid to EM_Clock high		5	–	–	nS
Taddriv	EM_Clock high to EM_Addr invalid		T/2 – 5	–	–	nS
Tweld	EM_WEn low to EM_Clock high		5	–	–	nS
Twehd	EM_Clock high to EM_WEn high		T/2 – 5	–	–	nS
Tds	Data valid before EM_Clock high		5	–	–	nS
Tdh	Data invalid after EM_Clock high		T	–	–	nS
Tadscld	EM_ADSCn low to EM_Clock high		5	–	–	nS
Tadschd	EM_Clock high to EM_ADSCn high		T/2 – 5	–	–	nS

Note
45. Limited by GPIO output frequency, see Table 11-10 on page 65.

11.9.6 Phase-Locked Loop

Table 11-83. PLL DC Specifications

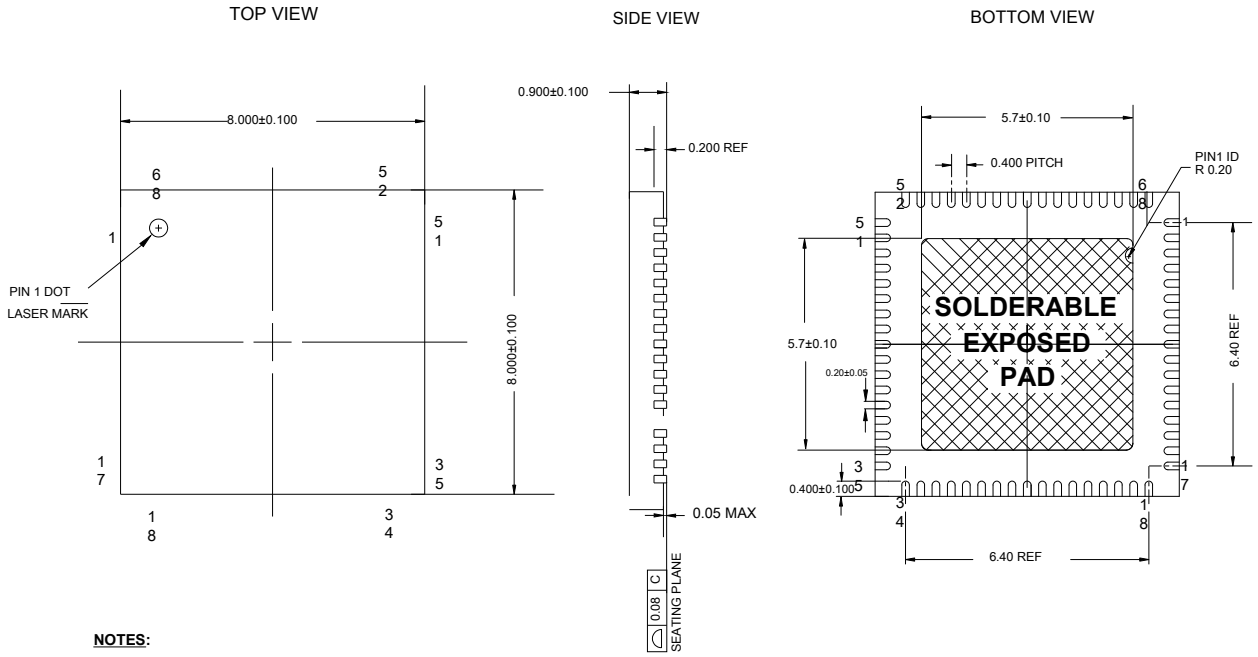
Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	PLL operating current	In = 3 MHz, Out = 67 MHz	–	400	–	µA
		In = 3 MHz, Out = 24 MHz	–	200	–	µA

Table 11-84. PLL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Fpllin	PLL input frequency[51]		1	–	48	MHz
	PLL intermediate frequency[52]	Output of prescaler	1	–	3	MHz
Fpllout	PLL output frequency[51]		24	–	67	MHz
	Lock time at startup		–	–	250	µs
Jperiod-rms	Jitter (rms)[53]		–	–	250	ps

Notes
51. This specification is guaranteed by testing the PLL across the specified range using the IMO as the source for the PLL.
52. PLL input divider, Q, must be set so that the input frequency is divided down to the intermediate frequency range. Value for Q ranges from 1 to 16.
53. Based on device characterization (Not production tested).

Figure 13-3. 68-pin QFN 8×8 with 0.4 mm Pitch Package Outline (Sawn Version)

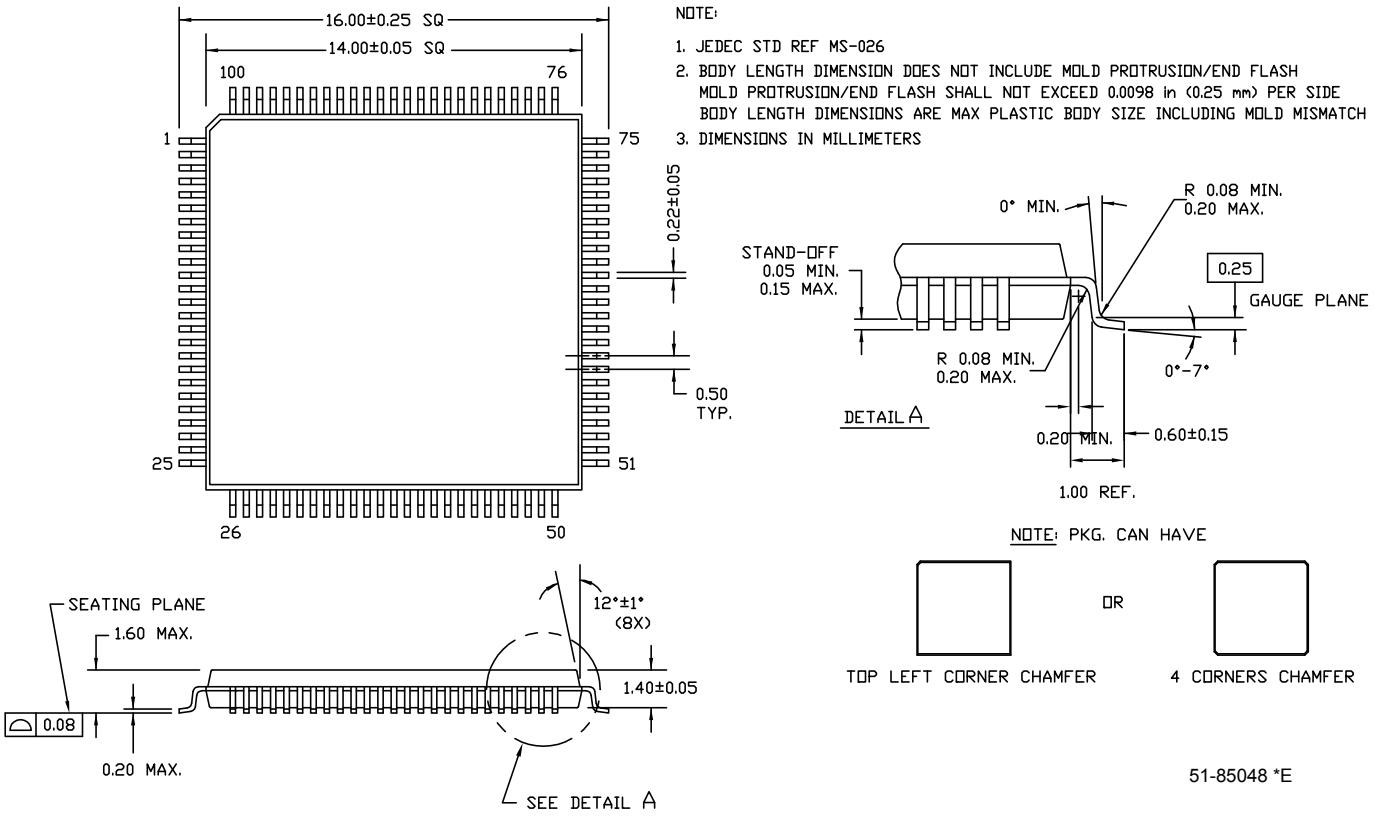


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.17g
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-09618 *C

Figure 13-4. 100-pin TQFP (14 × 14 × 1.4 mm) Package Outline



51-85048 *E

Table 14-1. Acronyms Used in this Document *(continued)*

Acronym	Description
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration datasheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA

Table 14-1. Acronyms Used in this Document *(continued)*

Acronym	Description
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

15. Reference Documents

PSoC® 3, PSoC® 5 Architecture TRM

PSoC® 3 Registers TRM

16. Document Conventions

16.1 Units of Measure

Table 16-1. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibels
fF	femtofarads
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohours
kHz	kilohertz
kΩ	kilohms
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	megaohms
Msps	megasamples per second

Description Title: PSoC® 3: CY8C38 Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-11729				
*K	2903576	04/01/2010	MKEA	Updated Vb pin in PCB Schematic. Updated Tstartup parameter in AC Specifications table. Added Load regulation and Line regulation parameters to Inductive Boost Regulator DC Specifications table. Updated I_{CC} parameter in LCD Direct Drive DC Specs table. In page 1, updated internal oscillator range under Precision programmable clocking to start from 3 MHz. Updated I_{OUT} parameter in LCD Direct Drive DC Specs table. Updated Table 6-2 and Table 6-3. Added bullets on CapSense in page 1; added CapSense column in Section 12. Removed some references to footnote [1]. Changed INC_Rn cycles from 3 to 2 (Table 4-1). Added footnote in PLL AC Specification table. Added PLL intermediate frequency row with footnote in PLL AC Specs table. Added UDBs subsection under 11.6 Digital Peripherals. Updated Figure 2-6 (PCB Layout). Updated Pin Descriptions section and modified Figures 6-6, 6-8, 6-9. Updated LVD in Tables 6-2 and 6-3; modified Low-power modes bullet in page 1. Added note to Figures 2-5 and 6-2; Updated Figure 6-2 to add capacitors for V_{DDA} and V_{DDD} pins. Updated boost converter section (6.2.2). Updated Tstartup values in Table 11-3. Removed IPOR rows from Table 11-68. Updated 6.3.1.1, Power Voltage Level Monitors. Updated section 5.2 and Table 11-2 to correct suggestion of execution from flash. Updated V_{REF} specs in Table 11-21. Updated IDAC uncompensated gain error in Table 11-25. Updated Delay from Interrupt signal input to ISR code execution from ISR code in Table11-72. Removed other line in table. Added sentence to last paragraph of section 6.1.1.3. Updated T_{RESP}, high and low-power modes, in Table 11-24. Updated f_TCK values in Table 11-73 and f_SWDCK values in Table 11-74. Updated SNR condition in Table 11-20. Corrected unit of measurement in Table 11-21. Updated sleep wakeup time in Table 6-3 and Tsleep in Table 11-3. Added 1.71 V <= V_{DDD} < 3.3 V, SWD over USBIO pins value to Table 11-74. Removed mention of hibernate reset (HRES) from page 1 features, Table 6-3, Section 6.2.1.4, Section 6.3, and Section 6.3.1.1. Changed PPOR/PRES to TBDs in Section 6.3.1.1, Section 6.4.1.6 (changed PPOR to reset), Table 11-3 (changed PPOR to PRES), Table 11-68 (changed title, values TBD), and Table 11-69 (changed PPOR_TR to PRES_TR). Added sentence saying that LVD circuits can generate a reset to Section 6.3.1.1. Changed I_{DD} values on page 1, page 5, and Table 11-2. Changed resume time value in Section 6.2.1.3. Changed ESD HBM value in Table 11-1. Changed SNR in 16-bit resolution mode value and sample rate row in Table 11-20. Removed V_{DDA} = 1.65 V rows and changed BWag value in Table 11-22. Changed V_{IOFF} values and changed CMRR value in Table 11-23. Changed INL max value in Table 11-27. Added max value to the Quiescent current specs in Tables 11-29 and 11-31. Changed occurrences of “Block” to “Row” and deleted the “ECC not included” footnote in Table 11-57. Changed max response time value in Tables 11-69 and 11-71. Changed the Startup time in Table 11-79. Added condition to intermediate frequency row in Table 11-85. Added row to Table 11-69. Added brown out note to Section 11.8.1.