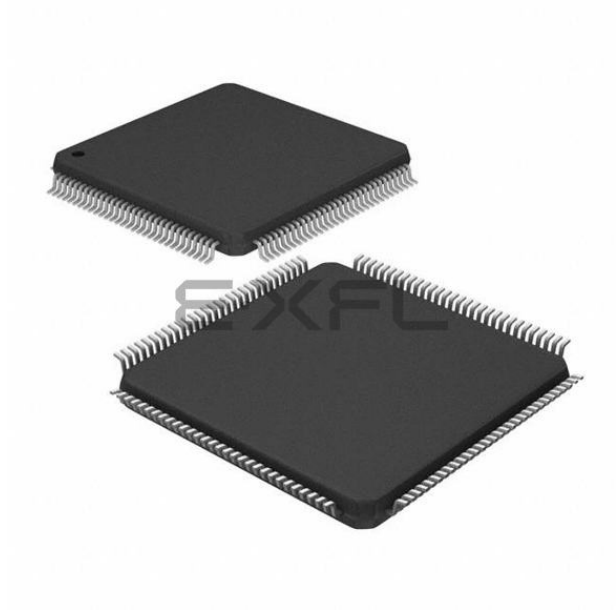
Cypress Semiconductor Corp - MB9BF406RAPMC-G-JNE2 Datasheet



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What is "Embedded - Microcontrollers"?

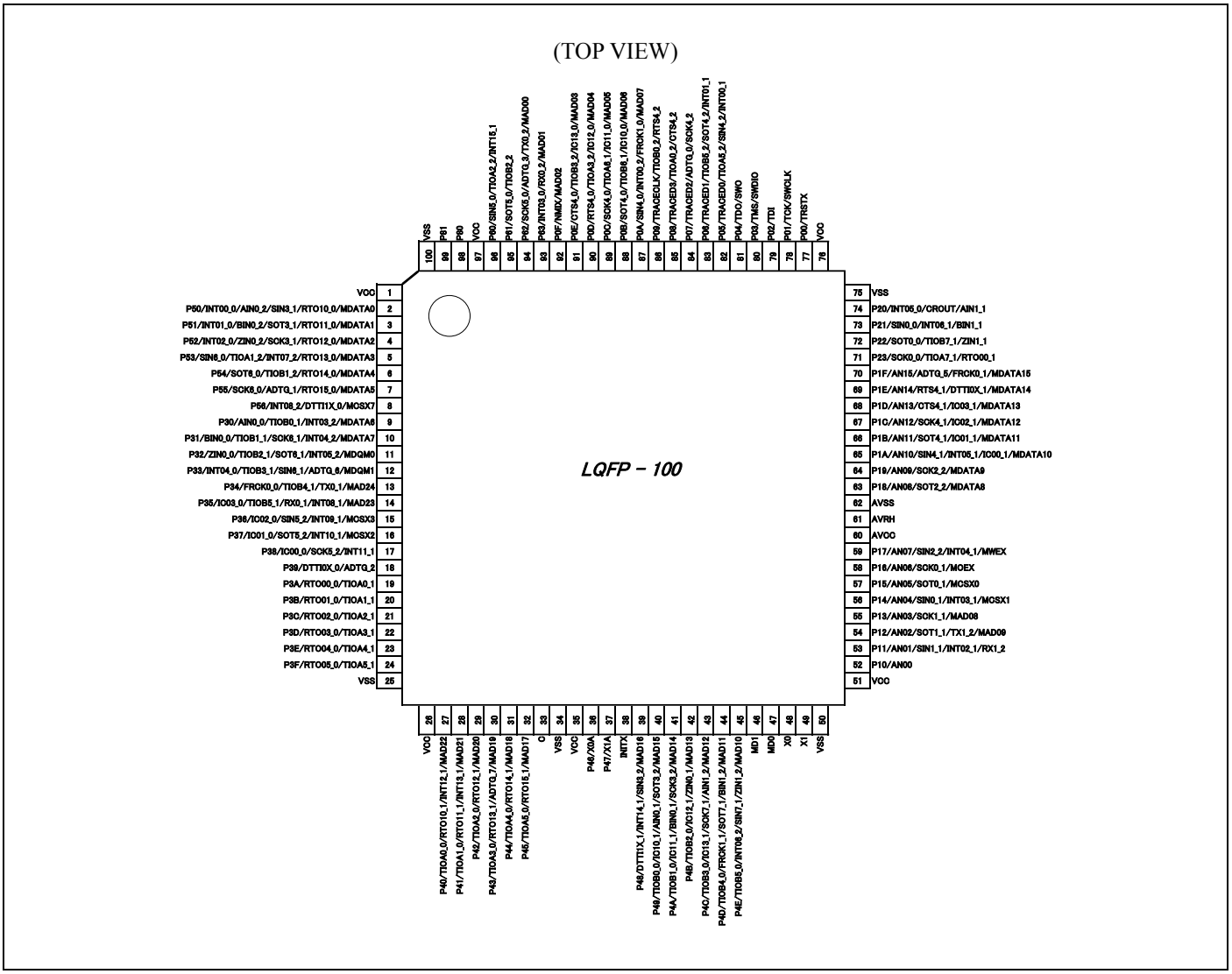
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	100
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/rochester-electronics/mb9bf406rapmc-g-jne2

3. Pin Assignment

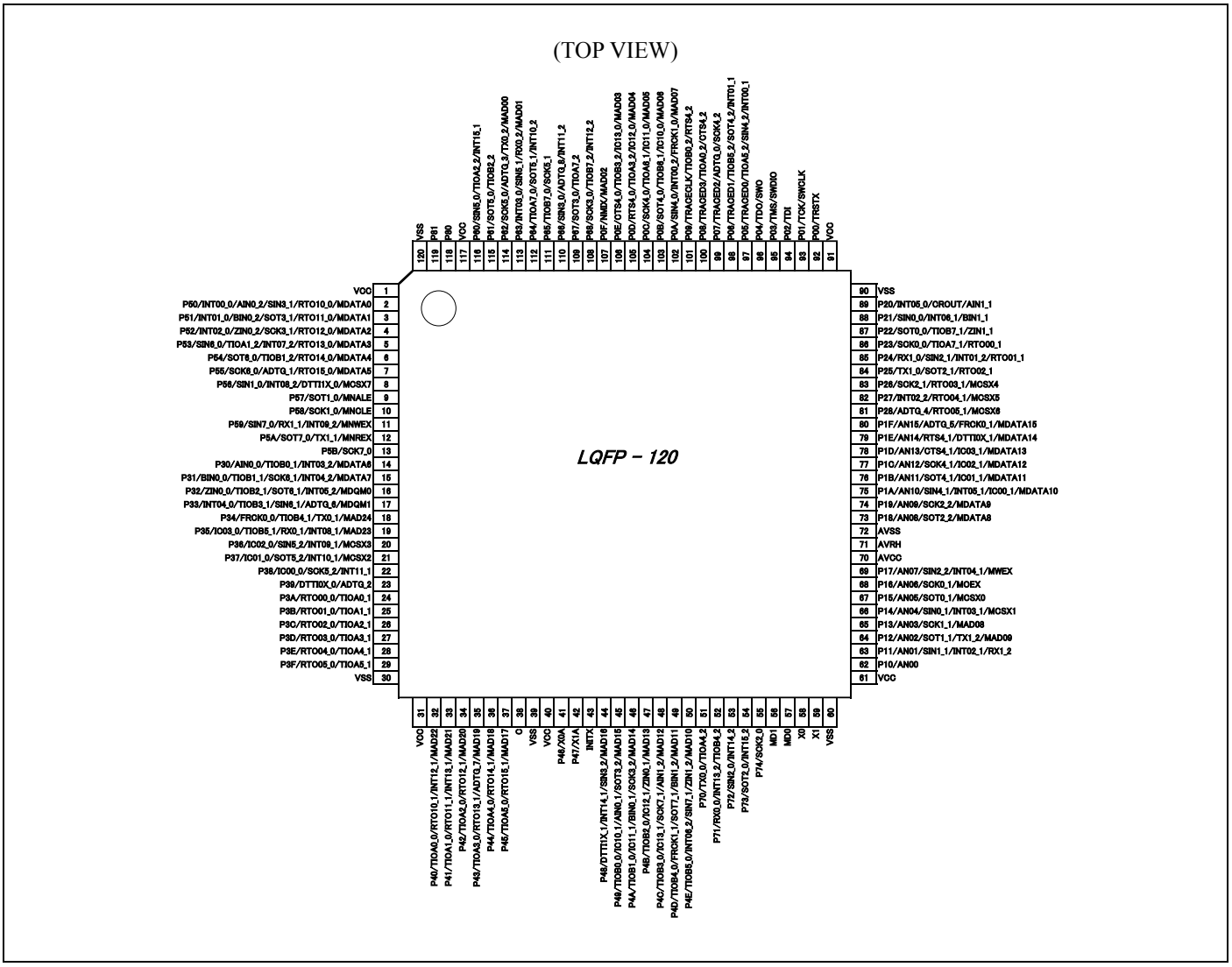
LQI100



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

LQM120



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
17	G2	22	P38 IC00_0 SCK5_2 (SCL5_2) INT11_1	E	H
18	F4	23	P39 DTTI0X_0 ADTG_2	E	I
19	G3	24	P3A RTO00_0 (PPG00_0) TIOA0_1	G	I
-	B2	-	VSS	-	
20	H1	25	P3B RTO01_0 (PPG00_0) TIOA1_1	G	I
21	H2	26	P3C RTO02_0 (PPG02_0) TIOA2_1	G	I
22	G4	27	P3D RTO03_0 (PPG02_0) TIOA3_1	G	I
23	H3	28	P3E RTO04_0 (PPG04_0) TIOA4_1	G	I
24	J2	29	P3F RTO05_0 (PPG04_0) TIOA5_1	G	I
25	L1	30	VSS	-	
26	J1	31	VCC	-	
27	J4	32	P40 TIOA0_0 RTO10_1 (PPG10_1) INT12_1 MAD22	G	H

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
28	L5	33	P41 TIOA1_0 RTO11_1 (PPG10_1) INT13_1 MAD21	G	H
29	K5	34	P42 TIOA2_0 RTO12_1 (PPG12_1) MAD20	G	I
30	J5	35	P43 TIOA3_0 RTO13_1 (PPG12_1) ADTG_7 MAD19	G	I
-	K2	-	VSS	-	
-	J3	-	VSS	-	
-	H4	-	VSS	-	
31	H5	36	P44 TIOA4_0 RTO14_1 (PPG14_1) MAD18	G	I
32	L6	37	P45 TIOA5_0 RTO15_1 (PPG14_1) MAD17	G	I
33	L2	38	C	-	
34	L4	39	VSS	-	
35	K1	40	VCC	-	
36	L3	41	P46 X0A	D	M
37	K3	42	P47 X1A	D	N
38	K4	43	INITX	B	C
39	K6	44	P48 DTTI1X_1 INT14_1 SIN3_2 MAD16	E	H

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
-	-	52	P71 RX0_0 INT13_2 TIOB4_2	E	H
-	-	53	P72 SIN2_0 INT14_2	E	H
-	-	54	P73 SOT2_0 (SDA2_0) INT15_2	E	H
-	-	55	P74 SCK2_0 (SCL2_0)	E	I
46	K9	56	MD1	C	D
47	L8	57	MD0	C	D
48	L9	58	X0	A	A
49	L10	59	X1	A	B
50	L11	60	VSS	-	
51	K11	61	VCC	-	
52	J11	62	P10 AN00	F	K
53	J10	63	P11 AN01 SIN1_1 INT02_1 RX1_2	F	L
-	K10	-	VSS	-	
-	J9	-	VSS	-	
54	J8	64	P12 AN02 SOT1_1 (SDA1_1) TX1_2 MAD09	F	K
55	H10	65	P13 AN03 SCK1_1 (SCL1_1) MAD08	F	K

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-100	BGA-112	LQFP-120			
80	A8	95	P03 TMS SWDIO	E	E
81	B8	96	P04 TDO SWO	E	E
82	C8	97	P05 TRACED0 TIOA5_2 SIN4_2 INT00_1	E	F
-	D8	-	VSS	-	
83	D9	98	P06 TRACED1 TIOB5_2 SOT4_2 (SDA4_2) INT01_1	E	F
84	A7	99	P07 TRACED2 ADTG_0 SCK4_2 (SCL4_2)	E	G
85	B7	100	P08 TRACED3 TIOA0_2 CTS4_2	E	G
86	C7	101	P09 TRACECLK TIOB0_2 RTS4_2	E	G
87	D7	102	P0A SIN4_0 INT00_2 FRCK1_0 MAD07	E	H
88	A6	103	P0B SOT4_0 (SDA4_0) TIOB6_1 IC10_0 MAD06	E	I

List of pin functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
ADC	ADTG_0	A/D converter external trigger input pin.	84	A7	99
	ADTG_1		7	D3	7
	ADTG_2		18	F4	23
	ADTG_3		94	C5	114
	ADTG_4		-	-	81
	ADTG_5		70	D11	80
	ADTG_6		12	E4	17
	ADTG_7		30	J5	35
	ADTG_8		-	-	110
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	52	J11	62
	AN01		53	J10	63
	AN02		54	J8	64
	AN03		55	H10	65
	AN04		56	H9	66
	AN05		57	H7	67
	AN06		58	G10	68
	AN07		59	G9	69
	AN08		63	G8	73
	AN09		64	F10	74
	AN10		65	F9	75
	AN11		66	E11	76
	AN12		67	E10	77
	AN13		68	F8	78
	AN14		69	E9	79
	AN15		70	D11	80
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin.	27	J4	32
	TIOA0_1		19	G3	24
	TIOA0_2		85	B7	100
	TIOB0_0	Base timer ch.0 TIOB pin.	40	J6	45
	TIOB0_1		9	E1	14
	TIOB0_2		86	C7	101
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin.	28	L5	33
	TIOA1_1		20	H1	25
	TIOA1_2		5	D1	5
	TIOB1_0	Base timer ch.1 TIOB pin.	41	L7	46
	TIOB1_1		10	E2	15
	TIOB1_2		6	D2	6
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin.	29	K5	34
	TIOA2_1		21	H2	26
	TIOA2_2		96	C4	116
	TIOB2_0	Base timer ch.2 TIOB pin.	42	K7	47
	TIOB2_1		11	E3	16
	TIOB2_2		95	B4	115

Module	Pin name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin.	30	J5	35
	TIOA3_1		22	G4	27
	TIOA3_2		90	C6	105
	TIOB3_0	Base timer ch.3 TIOB pin.	43	H6	48
	TIOB3_1		12	E4	17
	TIOB3_2		91	A5	106
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin.	31	H5	36
	TIOA4_1		23	H3	28
	TIOA4_2		-	-	51
	TIOB4_0	Base timer ch.4 TIOB pin.	44	J7	49
	TIOB4_1		13	F1	18
	TIOB4_2		-	-	52
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin.	32	L6	37
	TIOA5_1		24	J2	29
	TIOA5_2		82	C8	97
	TIOB5_0	Base timer ch.5 TIOB pin.	45	K8	50
	TIOB5_1		14	F2	19
	TIOB5_2		83	D9	98
Base Timer 6	TIOA6_1	Base timer ch.6 TIOA pin.	89	B6	104
	TIOB6_1	Base timer ch.6 TIOB pin.	88	A6	103
Base Timer 7	TIOA7_0	Base timer ch.7 TIOA pin.	-	-	112
	TIOA7_1		71	D10	86
	TIOA7_2		-	-	109
	TIOB7_0	Base timer ch.7 TIOB pin.	-	-	111
	TIOB7_1		72	E8	87
	TIOB7_2		-	-	108
CAN 0	TX0_0	CAN interface ch.0 TX output.	-	-	51
	TX0_1		13	F1	18
	TX0_2		94	C5	114
	RX0_0	CAN interface ch.0 RX input.	-	-	52
	RX0_1		14	F2	19
	RX0_2		93	D6	113
CAN 1	TX1_0	CAN interface ch.1 TX output.	-	-	84
	TX1_1		-	-	12
	TX1_2		54	J8	64
	RX1_0	CAN interface ch.1 RX input.	-	-	85
	RX1_1		-	-	11
	RX1_2		53	J10	63

Module	Pin name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
Debugger	SWCLK	Serial wire debug interface clock input.	78	B9	93
	SWDIO	Serial wire debug interface data input / output.	80	A8	95
	SWO	Serial wire viewer output.	81	B8	96
	TCK	JTAG test clock input.	78	B9	93
	TDI	JTAG test data input.	79	B11	94
	TDO	JTAG debug data output.	81	B8	96
	TMS	JTAG test mode state input/output.	80	A8	95
	TRACECLK	Trace CLK output of ETM.	86	C7	101
	TRACED0	Trace data output of ETM.	82	C8	97
	TRACED1		83	D9	98
	TRACED2		84	A7	99
	TRACED3		85	B7	100
	TRSTX	JTAG test reset Input.	77	A9	92
External Bus	MAD00	External bus interface address bus.	94	C5	114
	MAD01		93	D6	113
	MAD02		92	B5	107
	MAD03		91	A5	106
	MAD04		90	C6	105
	MAD05		89	B6	104
	MAD06		88	A6	103
	MAD07		87	D7	102
	MAD08		55	H10	65
	MAD09		54	J8	64
	MAD10		45	K8	50
	MAD11		44	J7	49
	MAD12		43	H6	48
	MAD13		42	K7	47
	MAD14		41	L7	46
	MAD15		40	J6	45
	MAD16		39	K6	44
	MAD17		32	L6	37
	MAD18		31	H5	36
	MAD19		30	J5	35
	MAD20		29	K5	34
	MAD21		28	L5	33
	MAD22		27	J4	32
	MAD23		14	F2	19
	MAD24		13	F1	18
	MCSX0	External bus interface chip select output pin.	57	H7	67
	MCSX1		56	H9	66
	MCSX2		16	G1	21
	MCSX3		15	F3	20
	MCSX4		-	-	83
	MCSX5		-	-	82
	MCSX6		-	-	81
	MCSX7		8	D5	8

Module	Pin name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
Multi Function Serial 2	SIN2_0	Multifunction serial interface ch.2 input pin.	-	-	53
	SIN2_1		-	-	85
	SIN2_2		59	G9	69
	SOT2_0 (SDA2_0)	Multifunction serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I^2C (operation mode 4).	-	-	54
	SOT2_1 (SDA2_1)		-	-	84
	SOT2_2 (SDA2_2)		63	G8	73
	SCK2_0 (SCL2_0)	Multifunction serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL2 when it is used in an I^2C (operation mode 4).	-	-	55
	SCK2_1 (SCL2_1)		-	-	83
	SCK2_2 (SCL2_2)		64	F10	74
Multi Function Serial 3	SIN3_0	Multifunction serial interface ch.3 input pin.	-	-	110
	SIN3_1		2	C1	2
	SIN3_2		39	K6	44
	SOT3_0 (SDA3_0)	Multifunction serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I^2C (operation mode 4).	-	-	109
	SOT3_1 (SDA3_1)		3	C2	3
	SOT3_2 (SDA3_2)		40	J6	45
	SCK3_0 (SCL3_0)	Multifunction serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL3 when it is used in an I^2C (operation mode 4).	-	-	108
	SCK3_1 (SCL3_1)		4	B3	4
	SCK3_2 (SCL3_2)		41	L7	46

Module	Pin name	Function	Pin No.		
			LQFP-100	BGA-112	LQFP-120
Multi Function Serial 4	SIN4_0	Multifunction serial interface ch.4 input pin.	87	D7	102
	SIN4_1		65	F9	75
	SIN4_2		82	C8	97
	SOT4_0 (SDA4_0)	Multifunction serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I^2C (operation mode 4).	88	A6	103
	SOT4_1 (SDA4_1)		66	E11	76
	SOT4_2 (SDA4_2)		83	D9	98
	SCK4_0 (SCL4_0)	Multifunction serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL4 when it is used in an I^2C (operation mode 4).	89	B6	104
	SCK4_1 (SCL4_1)		67	E10	77
	SCK4_2 (SCL4_2)		84	A7	99
	RTS4_0	Multifunction serial interface ch.4 RTS output pin.	90	C6	105
	RTS4_1		69	E9	79
	RTS4_2		86	C7	101
	CTS4_0	Multifunction serial interface ch.4 CTS input pin.	91	A5	106
	CTS4_1		68	F8	78
	CTS4_2		85	B7	100
Multi Function Serial 5	SIN5_0	Multifunction serial interface ch.5 input pin.	96	C4	116
	SIN5_1		-	-	113
	SIN5_2		15	F3	20
	SOT5_0 (SDA5_0)	Multifunction serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I^2C (operation mode 4).	95	B4	115
	SOT5_1 (SDA5_1)		-	-	112
	SOT5_2 (SDA5_2)		16	G1	21
	SCK5_0 (SCL5_0)	Multifunction serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL5 when it is used in an I^2C (operation mode 4).	94	C5	114
	SCK5_1 (SCL5_1)		-	-	111
	SCK5_2 (SCL5_2)		17	G2	22

Peripheral Address Map

Start address	End address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	Flash Memory I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer
0x4001_2000	0x4001_2FFF		Software Watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function timer unit0
0x4002_1000	0x4002_1FFF		Multi-function timer unit1
0x4002_2000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Quadrature Position/Revolution Counter
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Internal CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External Interrupt Controller
0x4003_1000	0x4003_1FFF		Interrupt Request Batch-Read Function
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_5FFF		Low Voltage Detector
0x4003_6000	0x4003_6FFF		Reserved
0x4003_7000	0x4003_7FFF		CAN prescaler
0x4003_8000	0x4003_8FFF		Multi-function serial Interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External Memory interface
0x4004_0000	0x4004_FFFF	AHB	Reserved
0x4005_0000	0x4005_FFFF		Reserved
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x4006_1FFF		Reserved
0x4006_2000	0x4006_2FFF		CAN ch.0
0x4006_3000	0x4006_3FFF		CAN ch.1
0x4006_4000	0x41FF_FFFF		Reserved

12.3 DC Characteristics

12.3.1 Current rating

(V_{CC} = AV_{CC} =2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ*3	Max*4		
RUN mode current	I_{CC}	VCC	PLL RUN mode	CPU: 80 MHz, Peripheral: 40 MHz, FLASH 2Wait FRWTR.RWT = 10 FSYNDN.SD = 000	96	118	mA	*1, *5
				CPU: 60 MHz, Peripheral: 30 MHz, FLASH 0 Wait FRWTR.RWT = 00 FSYNDN.SD = 000	76	94	mA	*1, *5
				CPU: 80 MHz, Peripheral: 40 MHz, FLASH 5 Wait FRWTR.RWT = 10 FSYNDN.SD = 011	66	82	mA	*1, *5
				CPU: 60 MHz, Peripheral: 30 MHz, FLASH 3 Wait FRWTR.RWT = 00 FSYNDN.SD = 011	52	65	mA	*1, *5
			High-speed CR RUN mode	CPU/Peripheral: 4 MHz*2 FLASH 0 Wait FRWTR.RWT = 00 FSYNDN.SD = 000	6.0	9.2	mA	*1
			Sub RUN mode	CPU/Peripheral: 32 kHz FLASH 0 Wait FRWTR.RWT = 00 FSYNDN.SD = 000	0.2	2.24	mA	*1, *6
			Low-speed CR RUN mode	CPU/Peripheral: 100 kHz FLASH 0 Wait FRWTR.RWT = 00 FSYNDN.SD = 000	0.3	2.36	mA	*1
SLEEP mode current	I_{CCS}		PLL SLEEP mode	Peripheral: 40 MHz	43	54	mA	*1, *5
			High-speed CR SLEEP mode	Peripheral: 4 MHz*2	3.5	6.2	mA	*1
			Sub SLEEP mode	Peripheral: 32 kHz	0.15	2.18	mA	*1, *6
			Low-speed CR SLEEP mode	Peripheral: 100 kHz	0.22	2.27	mA	*1

*1: When all ports are fixed.

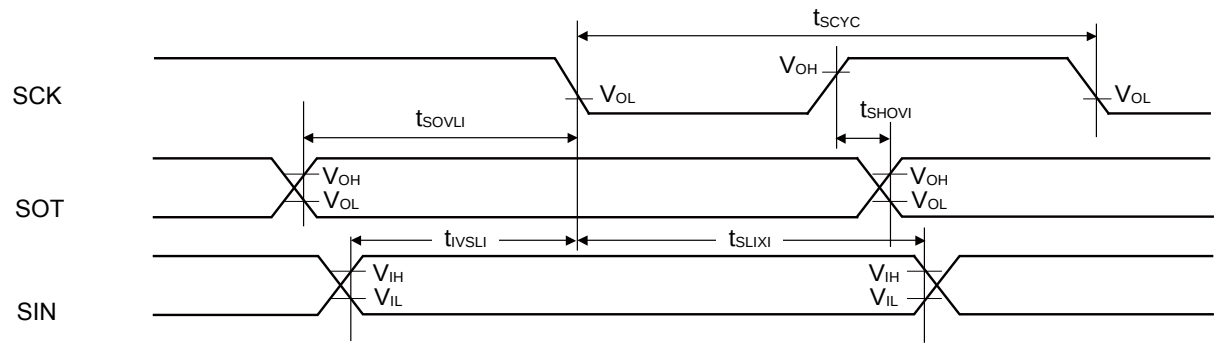
*2: When setting it to 4 MHz by trimming.

*3: T_A = +25°C, V_{CC} = 3.3 V

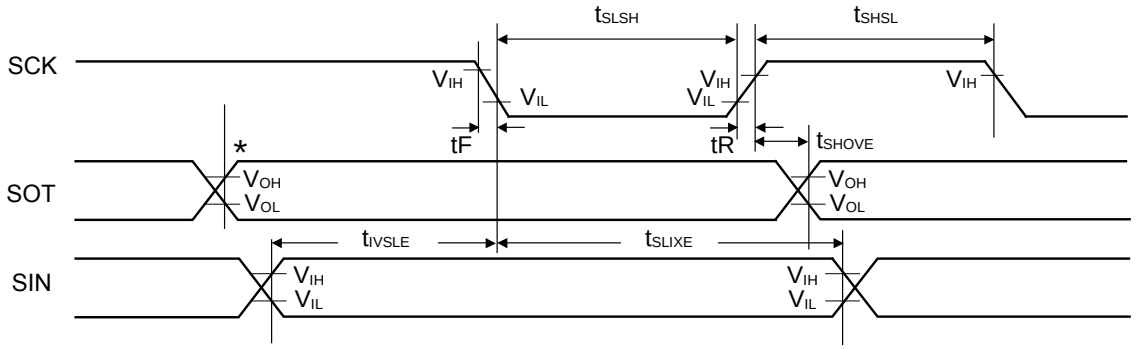
*4: T_A = +85°C, V_{CC} = 5.5 V

*5: When using the crystal oscillator of 4 MHz (Including the current consumption of the oscillation circuit)

*6: When using the crystal oscillator of 32 kHz (Including the current consumption of the oscillation circuit)



Master mode



Slave mode

*: Changes when writing to TDR register

12.4.13 I²C timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

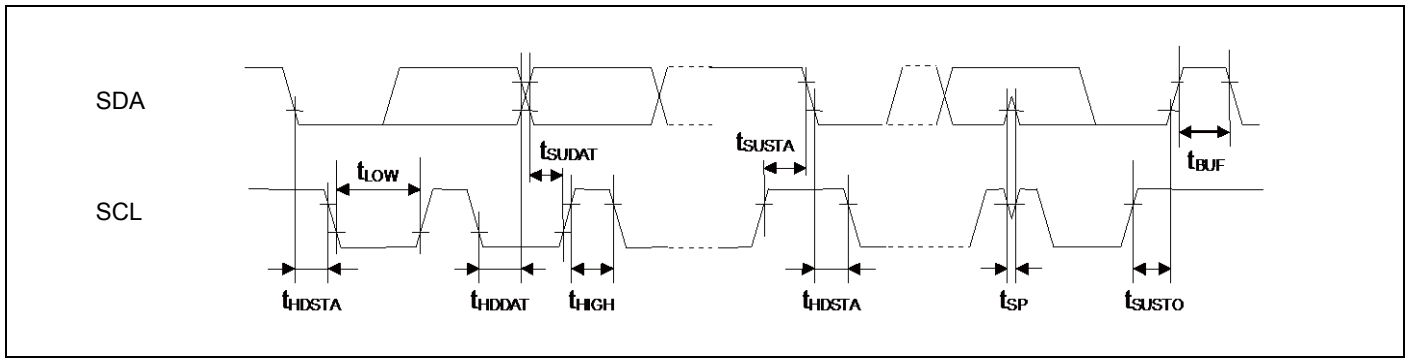
Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	F_{SCL}	C_L = 50 pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCLclock "L" width	t_{LOW}		4.7	-	1.3	-	µs	
SCLclock "H" width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	-	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	

*1: R and C represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively.
Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} must satisfy that it doesn't extend at least "L" period (t_{LOW}) of device's SCL signal.

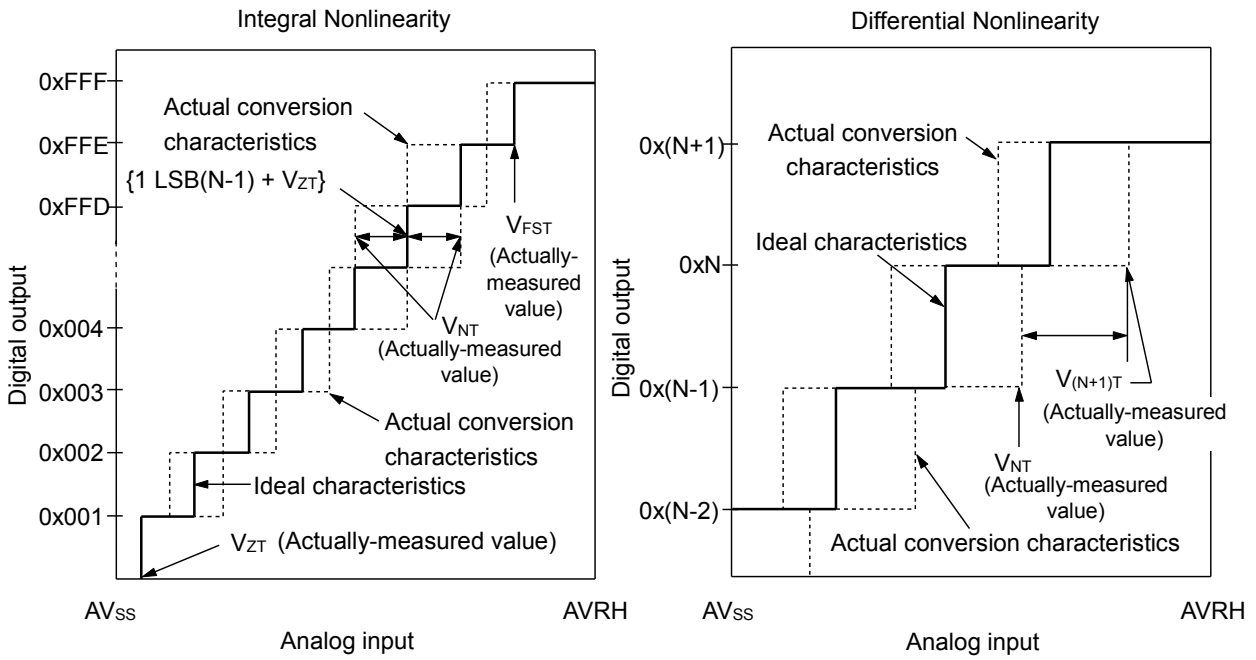
*3: Fast-mode I²C bus device can be used on Standard-mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{CYCP} is the APB bus clock cycle time.
About the APB bus number that I²C is connected to, see "Block Diagram" in this data sheet.
To use Standard-mode, set the APB bus clock at 2 MHz or more.
To use Fast-mode, set the APB bus clock at 8 MHz or more.



Definition of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.
V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

12.7 Flash Memory Write/Erase Characteristics

12.7.1 Write / Erase time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 85°C)

Parameter		Value		Unit	Remarks
		Typ*	Max*		
Sector erase time	Large Sector	1.6	7.5	s	Includes write time prior to internal erase
	Small Sector	0.4	2.1		
Half word (16 bit) write time		25	400	µs	Not including system-level overhead time.
Chip erase time		16	76.8	s	Includes write time prior to internal erase

*: The typical value is immediately after shipment, the maximum value is guarantee value under 100,000 cycle of erase/write.

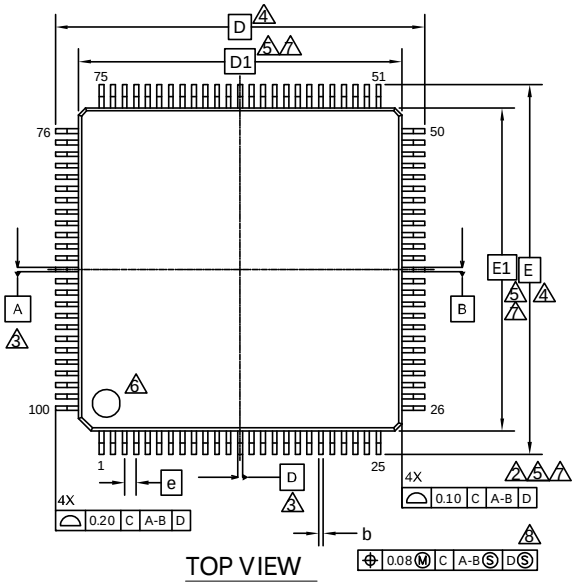
12.7.2 Erase/write cycles and data hold time

Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20 *	
10,000	10 *	
100,000	5 *	

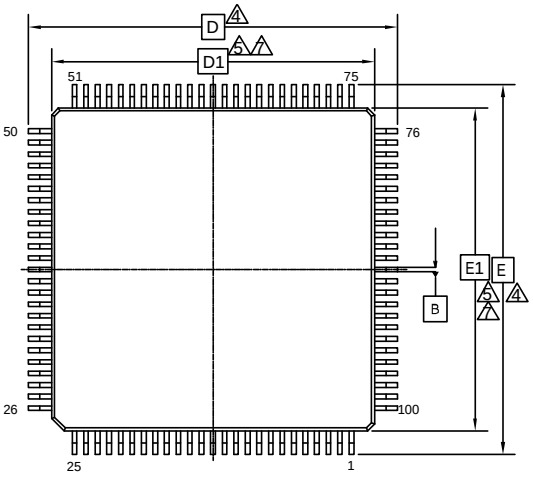
*: At average + 85°C

15. Package Dimensions

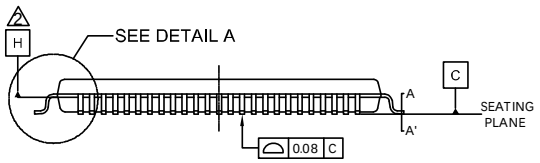
Package Type	Package Code
LQFP 100	LQI100



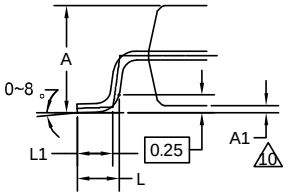
TOP VIEW



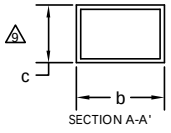
BOTTOM VIEW



SIDE VIEW



DETAIL A



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.15	—	0.27
c	0.09	—	0.20
D		16.00 BSC	
D1		14.00 BSC	
e		0.50 BSC	
E		16.00 BSC	
E1		14.00 BSC	
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

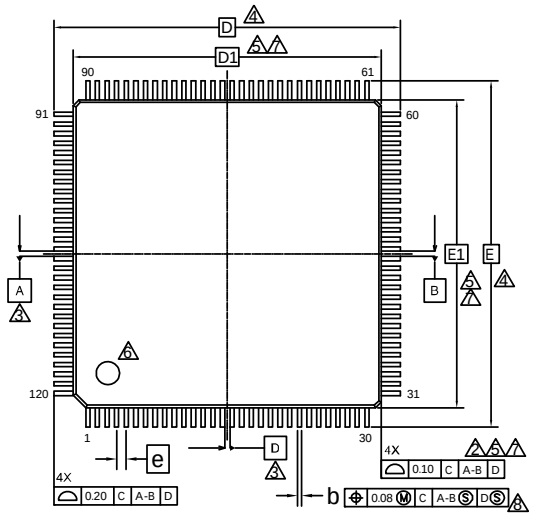
NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

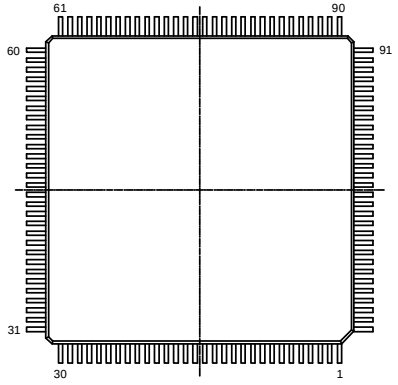
PACKAGE OUTLINE, 100 LEAD LQFP
14.0X14.0X1.7 MM LQI100 REV*A

002-11500 *A

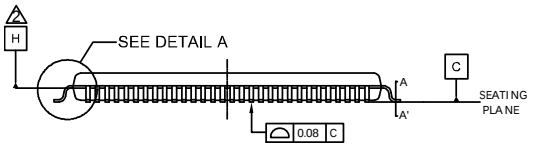
Package Type	Package Code
LQFP 120	LQM120



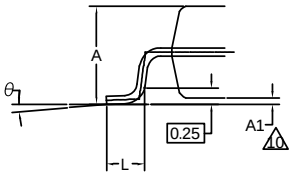
TOP VIEW



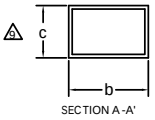
BOTTOM VIEW



SIDE VIEW



DETAIL A



SECTION A-A'

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.115	—	0.195
D		18.00 BSC	
D1		16.00 BSC	
e		0.50 BSC	
E		18.00 BSC	
E1		16.00 BSC	
L	0.45	0.60	0.75
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
11. JEDEC SPECIFICATION NO. REF: N/A.

PACKAGE OUTLINE, 120 LEAD LQFP
18.0X18.0X1.7 MM LQM120 REV**

002-16172 **

Page	Section	Change Results
67	ELECTRICAL CHARACTERISTICS 4. AC Characteristics (4-1)(4-2) Operating Conditions of Main PLL	· Added Main PLL clock frequency · Added the figure of Main PLL connection
68	ELECTRICAL CHARACTERISTICS 4. AC Characteristics (6) Power-on Reset Timing	· Added Time until releasing Power-on reset · Changed the figure of timing
74-81	ELECTRICAL CHARACTERISTICS 4. AC Characteristics (7) CSIO/UART Timing	· Modified from UART Timing to CSIO/UART Timing · Changed from Internal shift clock operation to Master mode · Changed from External shift clock operation to Slave mode
88	ELECTRICAL CHARACTERISTICS 5. 12bit A/D Converter	· Added the typical value of Integral Nonlinearity, Differential Nonlinearity, Zero transition voltage and Full-scale transition voltage · Added Conversion time at AVcc < 4.5V · Modified Stage transition time to operation permission · Modified the minimum value of Reference voltage
92	ELECTRICAL CHARACTERISTICS 7. Flash Memory Write/Erase Characteristics	Change to the erase time of include write time prior to internal erase
93-96	ELECTRICAL CHARACTERISTICS 8. Return Time from Low-Power Consumption Mode	Added Return Time from Low-Power Consumption Mode
99	ORDERING INFORMATION	Change to full part number
100	PACKAGE DIMENSIONS	Deleted FPT-100P-M20 and FPT-120P-M21

NOTE: Please see “Document History” about later revised information.