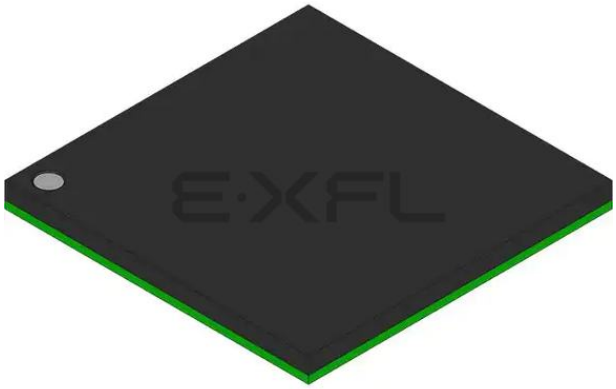

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, MPEG-4, VFP
RAM Controllers	DDR
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, Keypad, LCD
Ethernet	-
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Random Number Generator, RTIC, Secure Fusebox, Secure JTAG, Secure Memory
Package / Case	457-LFBGA
Supplier Device Package	457-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx31cvkn5d

1.2 Ordering Information

Table 1 provides the ordering information for the MCIMX31.

Table 1. Ordering Information[1]

Part Number	Silicon Revision[2, 3, 4,5]	Device Mask	Operating Temperature Range (°C)	Package[6]
MCIMX31DVKN5D!	2.0.1	M91E	–20 to 70	14 x 14 mm, 0.5 mm pitch, MAPBGA-457, Case 1581
MCIMX31LDVKN5D!	2.0.1	M91E	–20 to 70	
MCIMX31CVKN5D!	2.0.1	M91E	–40 to 85	
MCIMX31LCVKN5D!	2.0.1	M91E	–40 to 85	
MCIMX31DVMN5D!	2.0.1	M91E	–20 to 70	19 x 19 mm, 0.8 mm pitch, Case 1931
MCIMX31LDVMN5D!	2.0.1	M91E	–20 to 70	
MCIMX31CJKN5D	2.0.1	M91E	–40 to 85	14 x 14 mm, 0.5 mm pitch, MAPBGA-457, Case 1581
MCIMX31LCJKN5D	2.0.1	M91E	–40 to 85	

1 Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: Indicated by the Icon (!)

2 Information on reading the silicon revision register can be found in the IC Identification (IIM) chapter of the Reference Manual, see Section 6, “Product Documentation.”

3 Errata and fix information of the various mask sets can be found in the standard MCIMX31 Chip Errata, see Section 6, “Product Documentation.”

4 Changes in output buffer characteristics can be found in the I/O Setting Exceptions and Special Pad Descriptions table in the Reference Manual, see Section 6, “Product Documentation.”

5 JTAG functionality is not tested nor guaranteed at -40°C.

6 Case 1581 and 1931 are RoHS compliant, lead-free, MSL = 3.

1.2.1 Feature Differences Between Mask Sets

There are no silicon differences between revisions 2.0 and 2.0.1. The main difference is an updated iROM code which supports USB-HS, SD/MMC boot modes and corrects some boot mode related erratas.

4 Electrical Characteristics

This section provides the device-level and module-level electrical characteristics for the MCIMX31.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 4 for a quick reference to the individual tables and sections.

Table 4. MCIMX31 Chip-Level Conditions

For these characteristics, …	Topic appears …
Table 5, “Absolute Maximum Ratings”	on page 10
Table 7, “Thermal Resistance Data—19 × 19 mm Package”	on page 11
Table 8, “Operating Ranges”	on page 13
Table 9, “Specific Operating Ranges for Silicon Revision 2.0.1”	on page 14
Table 10, “Interface Frequency”	on page 14
Section 4.1.1, “Supply Current Specifications”	on page 16
Section 4.2, “Supply Power-Up/Power-Down Requirements and Restrictions”	on page 18

CAUTION

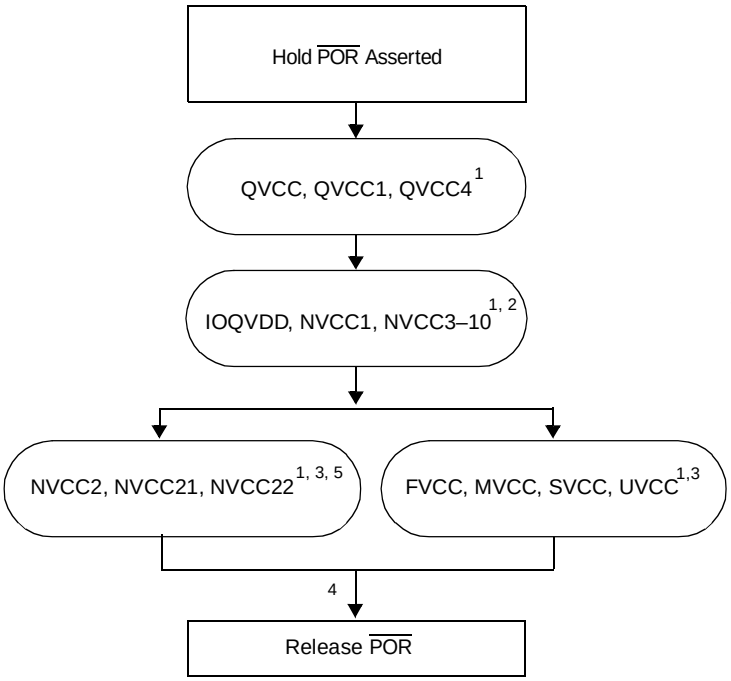
Stresses beyond those listed under Table 5 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Table 8, "Operating Ranges," on page 13 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply Voltage (Core)	$QVCC_{max}$	–0.5	1.65	V
Supply Voltage (I/O)	$NVCC_{max}$	–0.5	3.3	V
Input Voltage Range	V_{Imax}	–0.5	NVCC +0.3	V
Storage Temperature	$T_{storage}$	–40	125	^{o}C
ESD Damage Immunity:				
Human Body Model (HBM)	V_{esd}	—	1500	V
Machine Model (MM)		—	200	
Charge Device Model (CDM)		—	500	
Offset voltage allowed in run mode between core supplies.	V_{core_offset}[1]	—	15	mV

[1] The offset is the difference between all core voltage pair combinations of QVCC, QVCC1, and QVCC4.

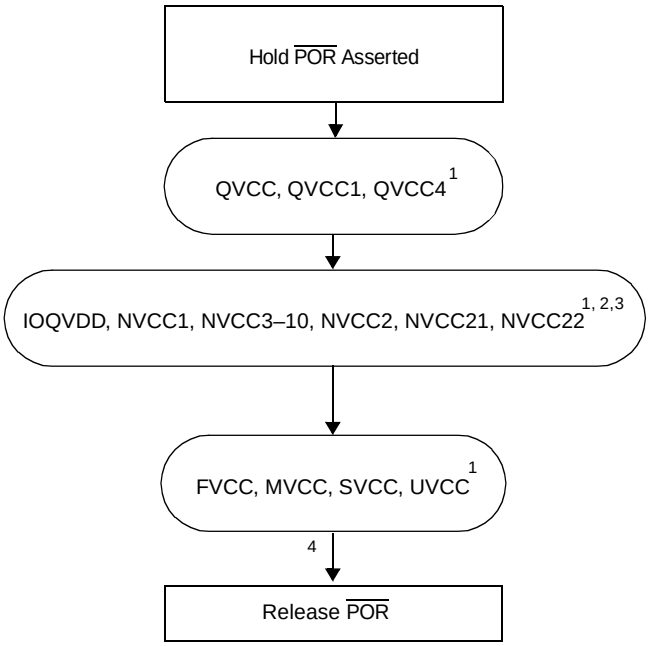
4.2.1.1 Power-Up Sequence for Silicon Revision 2.0.1



Notes:

1. The board design must guarantee that supplies reach 90% level before transition to the next state, using Power Management IC or other means.
2. The NVCC1 supply must not precede IOQVDD by more than 0.2 V until IOQVDD has reached 1.5 V. If IOQVDD is powered up first, there are no restrictions.
3. The parallel paths in the flow indicate that supply group NVCC2, NVCC21, and NVCC22, and supply group FVCC, MVCC, SVCC, and UVCC ramp-ups are independent.
4. FUSE_VDD should not be driven on power-up for Silicon Revision 2.0.1. This supply is dedicated for fuse burning (programming), and should not be driven upon boot-up.
5. Raising IOQVDD before NVCC21 produces a slight increase in current drain on IOQVDD of approximately 3–5 mA. The current increase will not damage the IC. Refer to Errata ID TLSbo91750 for details.

Figure 2. Option 1 Power-Up Sequence (Silicon Revision 2.0.1)



Notes:

1. The board design must guarantee that supplies reach 90% level before transition to the next state, using Power Management IC or other means.
2. The NVCC1 supply must not precede IOQVDD by more than 0.2 V until IOQVDD has reached 1.5 V. If IOQVDD is powered up first, there are no restrictions.
3. Raising NVCC2, NVCC21, and NVCC22 at the same time as IOQVDD does not produce the slight increase in current drain on IOQVDD (as described in Figure 2, Note 5).
4. FUSE_VDD should not be driven on power-up for Silicon Revision 2.0.1. This supply is dedicated for fuse burning (programming), and should not be driven upon boot-up.

Figure 3. Option 2 Power-Up Sequence (Silicon Revision 2.0.1)

Table 17. AC Electrical Characteristics of Fast[1] General I/O [2]

ID	Parameter	Symbol	Test Condition	Min	Typ	Max	Units
PA1	Output Transition Times (Max Drive)	tpr	25 pF 50 pF	0.68 1.34	1.33 2.6	2.07 4.06	ns
	Output Transition Times (High Drive)	tpr	25 pF 50 pF	.91 1.79	1.77 3.47	2.74 5.41	ns
	Output Transition Times (Std Drive)	tpr	25 pF 50 pF	1.36 2.68	2.64 5.19	4.12 8.11	ns

1 Fast/slow characteristic is selected per GPIO (where available) by “slew rate” control. See reference manual.

2 Use of GPIO in fast mode with the associated NVCC > 1.95 V can result in excessive overshoot and ringing.

Table 18. AC Electrical Characteristics of DDR I/O

ID	Parameter	Symbol	Test Condition	Min	Typ	Max	Units
PA1	Output Transition Times (DDR Drive)[1]	tpr	25 pF 50 pF	0.51 0.97	0.82 1.58	1.28 2.46	ns
	Output Transition Times (Max Drive)	tpr	25 pF 50 pF	0.67 1.29	1.08 2.1	1.69 3.27	ns
	Output Transition Times (High Drive)	tpr	25 pF 50 pF	.99 1.93	1.61 3.13	2.51 4.89	ns
	Output Transition Times (Std Drive)	tpr	25 pF 50 pF	1.96 3.82	3.19 6.24	4.99 9.73	ns

1 Use of DDR Drive can result in excessive overshoot and ringing.

4.3.3 Clock Amplifier Module (CAMP) Electrical Characteristics

This section outlines the Clock Amplifier Module (CAMP) specific electrical characteristics. Table 19 shows clock amplifier electrical characteristics.

Table 19. Clock Amplifier Electrical Characteristics for CKIH Input

Parameter	Min	Typ	Max	Units
Input Frequency	15	—	75	MHz
VIL (for square wave input)	0	—	0.3	V
VIH (for square wave input)	(VDD [1]– 0.25)	—	3	V
Sinusoidal Input Amplitude	0.4 [2]	—	VDD	Vp-p
Duty Cycle	45	50	55	%

1 VDD is the supply voltage of CAMP. See reference manual.

2 This value of the sinusoidal input will be measured through characterization.

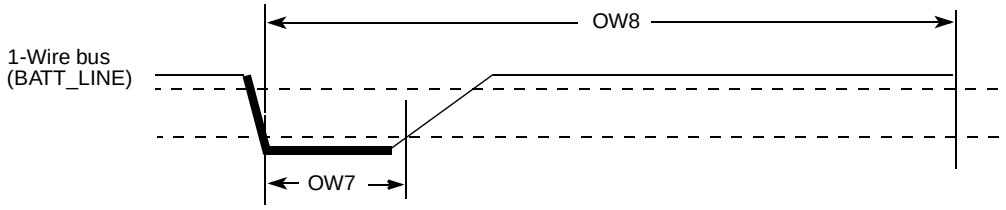


Figure 8. Write 1 Sequence Timing Diagram

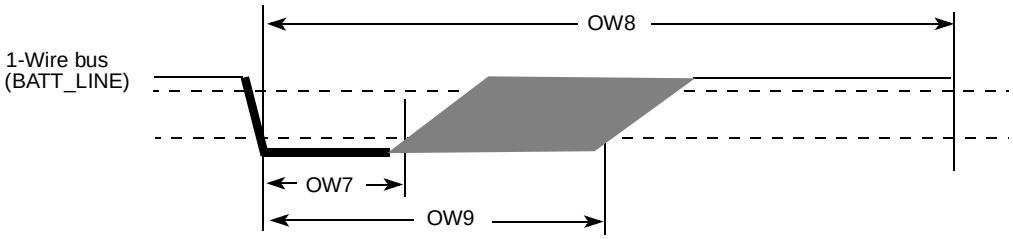


Figure 9. Read Sequence Timing Diagram

Table 22. WR1/RD Timing Parameters

ID	Parameter	Symbol	Min	Typ	Max	Units
OW7	Write 1 / Read Low Time	t_{LOW1}	1	5	15	µs
OW8	Transmission Time Slot	t_{SLOT}	60	117	120	µs
OW9	Release Time	$t_{RELEASE}$	15	—	45	µs

4.3.5 ATA Electrical Specifications (ATA Bus, Bus Buffers)

This section discusses ATA parameters. For a detailed description, refer to the ATA specification.

The user needs to use level shifters for 3.3 Volt or 5.0 Volt compatibility on the ATA interface.

The use of bus buffers introduces delay on the bus and introduces skew between signal lines. These factors make it difficult to operate the bus at the highest speed (UDMA-5) when bus buffers are used. If fast UDMA mode operation is needed, this may not be compatible with bus buffers.

Another area of attention is the slew rate limit imposed by the ATA specification on the ATA bus. According to this limit, any signal driven on the bus should have a slew rate between 0.4 and 1.2 V/ns with a 40 pF load. Not many vendors of bus buffers specify slew rate of the outgoing signals.

When bus buffers are used, the ata_data bus buffer is special. This is a bidirectional bus buffer, so a direction control signal is needed. This direction control signal is ata_buffer_en. When its high, the bus should drive from host to device. When its low, the bus should drive from device to host. Steering of the signal is such that contention on the host and device tri-state busses is always avoided.

Table 32. WEIM Bus Timing Parameters (continued)

ID	Parameter	Min	Max	Unit
WE8	Clock rise/fall to $\overline{OE}$ Invalid	–3	3	ns
WE9	Clock rise/fall to $\overline{EB}$[x] Valid	–3	3	ns
WE10	Clock rise/fall to $\overline{EB}$[x] Invalid	–3	3	ns
WE11	Clock rise/fall to $\overline{LBA}$ Valid	–3	3	ns
WE12	Clock rise/fall to $\overline{LBA}$ Invalid	–3	3	ns
WE13	Clock rise/fall to Output Data Valid	–2.5	4	ns
WE14	Clock rise to Output Data Invalid	–2.5	4	ns
WE15	Input Data Valid to Clock rise, FCE=0 FCE=1	8 2.5	—	ns
WE16	Clock rise to Input Data Invalid, FCE=0 FCE=1	–2 –2	—	ns
WE17	$\overline{ECB}$ setup time, FCE=0 FCE=1	6.5 3.5	—	ns
WE18	$\overline{ECB}$ hold time, FCE=0 FCE=1	–2 2	—	ns
WE19	$\overline{DTACK}$ setup time[1]	0	—	ns
WE20	$\overline{DTACK}$ hold time[1]	4.5	—	ns
WE21	BCLK High Level Width[2, 3]	—	T/2 – 3	ns
WE22	BCLK Low Level Width[2, 3]	—	T/2 – 3	ns
WE23	BCLK Cycle time[2]	15	—	ns

1 Applies to rising edge timing

2 BCLK parameters are being measured from the 50% VDD.

3 The actual cycle time is derived from the AHB bus clock frequency.

NOTE

High is defined as 80% of signal value and low is defined as 20% of signal value.

Test conditions: load capacitance, 25 pF. Recommended drive strength for all controls, address, and BCLK is Max drive.

Figure 27, Figure 28, Figure 29, Figure 30, Figure 31, and Figure 32 depict some examples of basic WEIM accesses to external memory devices with the timing parameters mentioned in Table 32 for specific control parameter settings.

Table 34. SDR SDRAM Write Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
SD13	Data setup time	tDS	2.0	—	ns
SD14	Data hold time	tDH	1.3	—	ns

[1] SD11 and SD12 are determined by SDRAM controller register settings.

NOTE

SDR SDRAM CLK parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 34 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

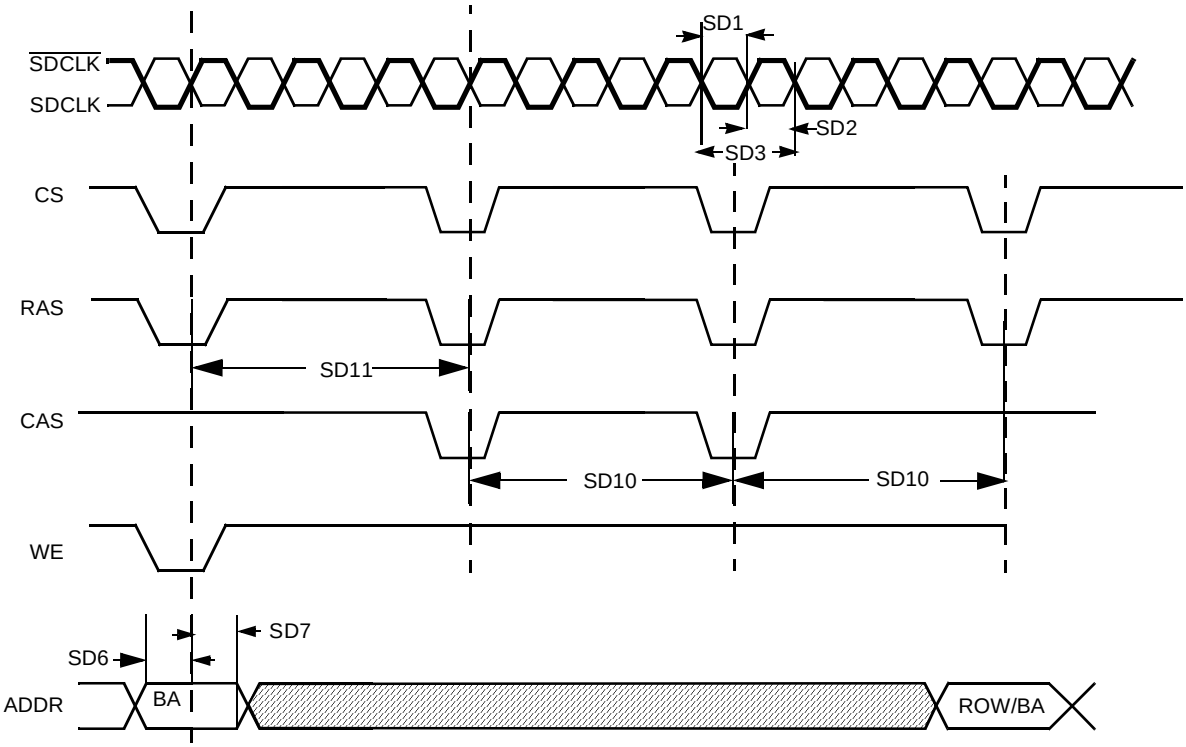


Figure 35. SDRAM Refresh Timing Diagram

Table 35. SDRAM Refresh Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	$\overline{\text{SDRAM clock low-level width}}$	tCL	3.4	4.1	ns

4.3.14 IPU—Sensor Interfaces

4.3.14.1 Supported Camera Sensors

Table 43 lists the known supported camera sensors at the time of publication.

Table 43. Supported Camera Sensors[1]

Vendor	Model
Conexant	CX11646, CX20490[2], CX20450[2]
Agilant	HDCP–2010, ADCS–1021[2], ADCS–1021[2]
Toshiba	TC90A70
ICMedia	ICM202A, ICM102[2]
iMagic	IM8801
Transchip	TC5600, TC5600J, TC5640, TC5700, TC6000
Fujitsu	MB86S02A
Micron	MI–SOC–0133
Matsushita	MN39980
STMicro	W6411, W6500, W6501[2], W6600[2], W6552[2], STV0974[2]
OmniVision	OV7620, OV6630
Sharp	LZ0P3714 (CCD)
Motorola	MC30300 (Python)[2], SCM20014[2], SCM20114[2], SCM22114[2], SCM20027[2]
National Semiconductor	LM9618[2]

1 Freescale Semiconductor does not recommend one supplier over another and in no way suggests that these are the only camera suppliers.

2 These sensors not validated at time of publication.

4.3.14.2 Functional Description

There are three timing modes supported by the IPU.

4.3.14.2.1 Pseudo BT.656 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the SENSB_VSYNC and SENSB_HSYNC signals. The timing syntax is defined by the BT.656 standard.

This operation mode follows the recommendations of ITU BT.656 specifications. The only control signal used is SENSB_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering SENSB_VSYNC and SENSB_HSYNC signals for internal use.

NOTE

HSP_CLK is the High-Speed Port Clock, which is the input to the Image Processing Unit (IPU). Its frequency is controlled by the Clock Control Module (CCM) settings. The HSP_CLK frequency must be greater than or equal to the AHB clock frequency.

The SCREEN_WIDTH, SCREEN_HEIGHT, H_SYNC_WIDTH, V_SYNC_WIDTH, BGXP, BGYP and V_SYNC_WIDTH_L parameters are programmed via the SDC_HOR_CONF, SDC_VER_CONF, SDC_BG_POS Registers. The FW and FH parameters are programmed for the corresponding DMA channel. The DISP3_IF_CLK_PER_WR, HSP_CLK_PERIOD and DISP3_IF_CLK_CNT_D parameters are programmed via the DI_DISP3_TIME_CONF, DI_HSP_CLK_PER and DI_DISP_ACC_CC Registers.

Figure 48 depicts the synchronous display interface timing for access level, and Table 47 lists the timing parameters. The DISP3_IF_CLK_DOWN_WR and DISP3_IF_CLK_UP_WR parameters are set via the DI_DISP3_TIME_CONF Register.

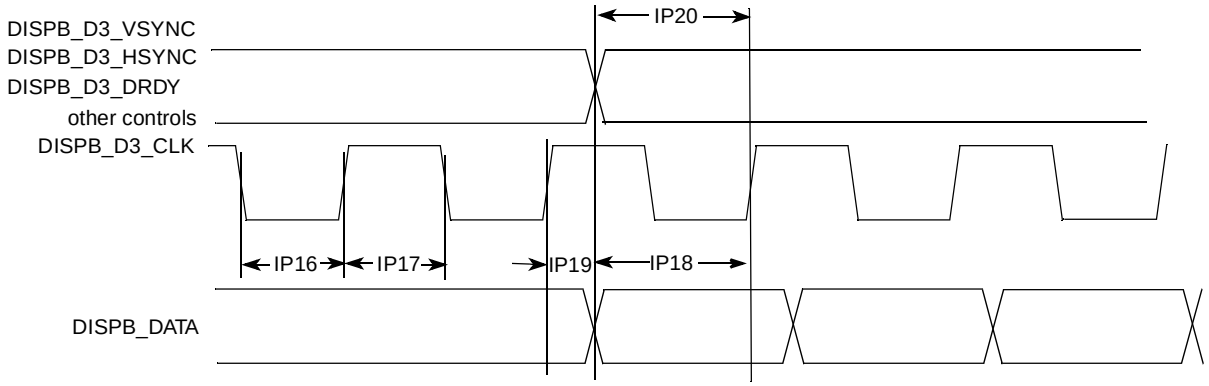


Figure 48. Synchronous Display Interface Timing Diagram—Access Level

Table 47. Synchronous Display Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min	Typ[1]	Max	Units
IP16	Display interface clock low time	Tckl	Tdicd–Tdicu–1.5	Tdicd[2]–Tdicu[3]	Tdicd–Tdicu+1.5	ns
IP17	Display interface clock high time	Tckh	Tdicp–Tdicd+Tdicu–1.5	Tdicp–Tdicd+Tdicu	Tdicp–Tdicd+Tdicu+1.5	ns
IP18	Data setup time	Tdsu	Tdicd–3.5	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp–Tdicd–3.5	Tdicp–Tdicu	—	ns
IP20	Control signals setup time to display interface clock	Tcsu	Tdicd–3.5	Tdicu	—	ns

1 The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

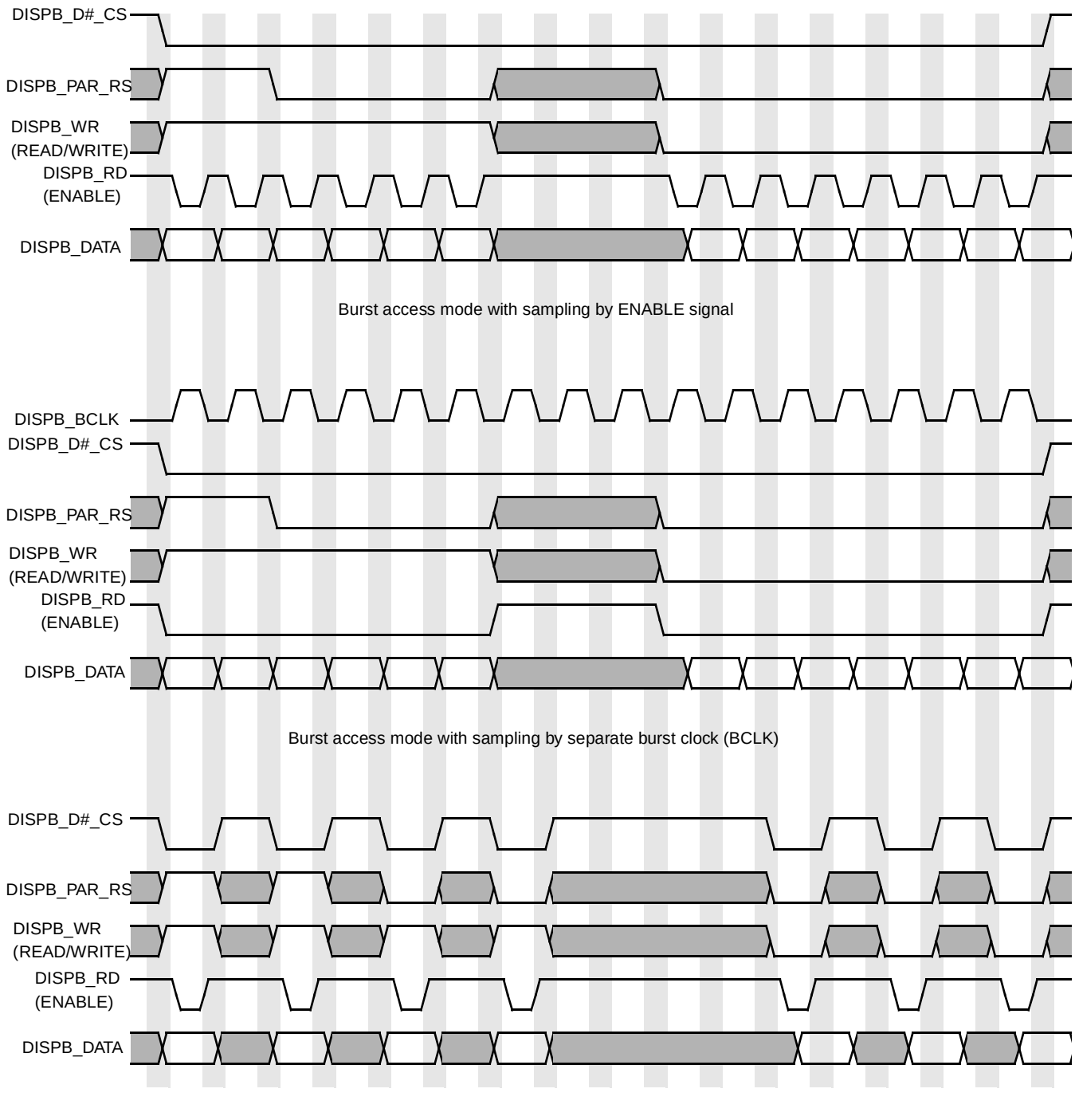


Figure 54. Asynchronous Parallel System 68k Interface (Type 2) Burst Mode TIming Diagram

Display read operation can be performed with wait states when each read access takes up to four display interface clock cycles according to the DISP0_RD_WAIT_ST parameter in the DI_DISP0_TIME_CONF_3, DI_DISP1_TIME_CONF_3, DI_DISP2_TIME_CONF_3 Registers. Figure 55 shows timing of the parallel interface with read wait states.

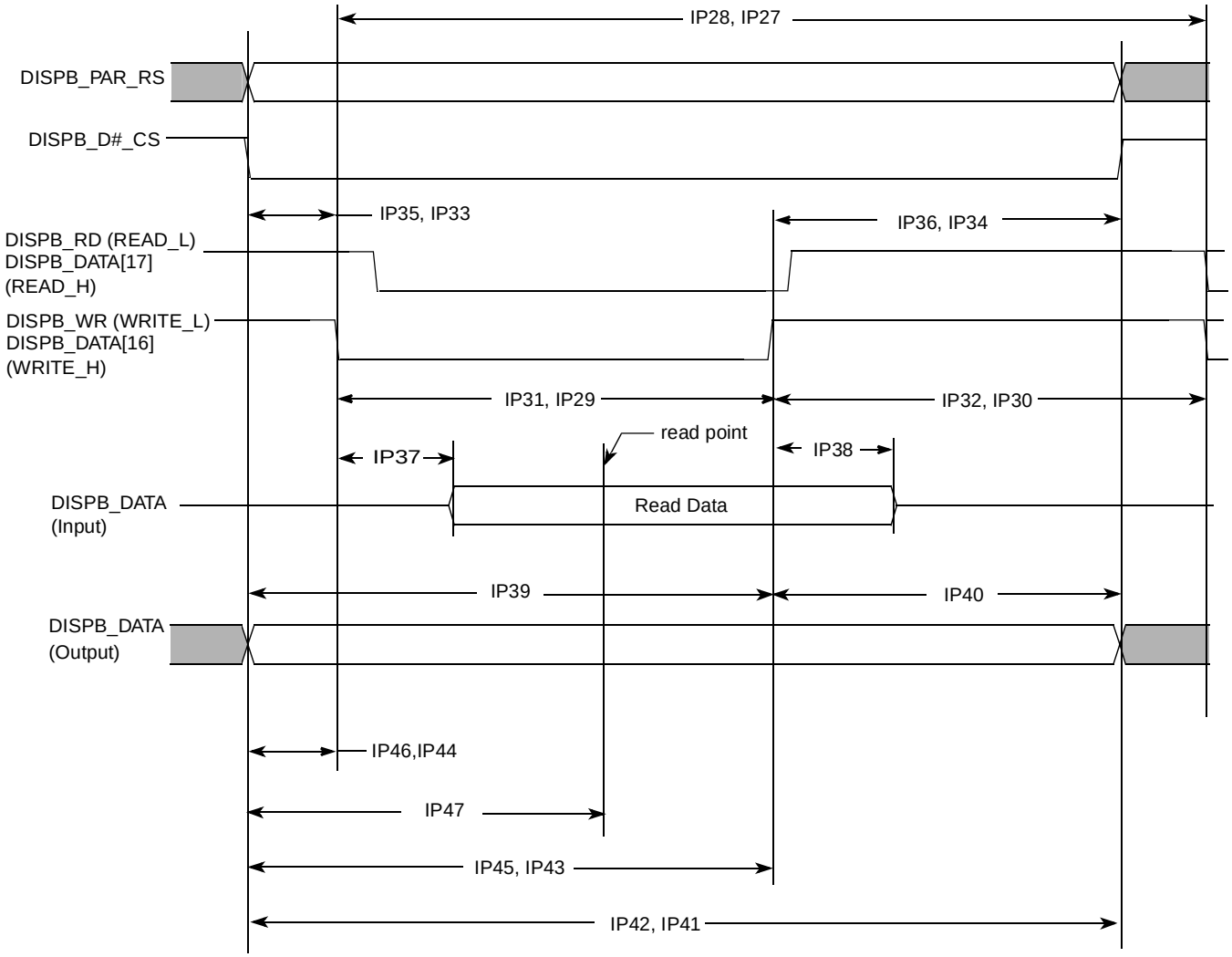


Figure 57. Asynchronous Parallel System 80 Interface (Type 2) Timing Diagram

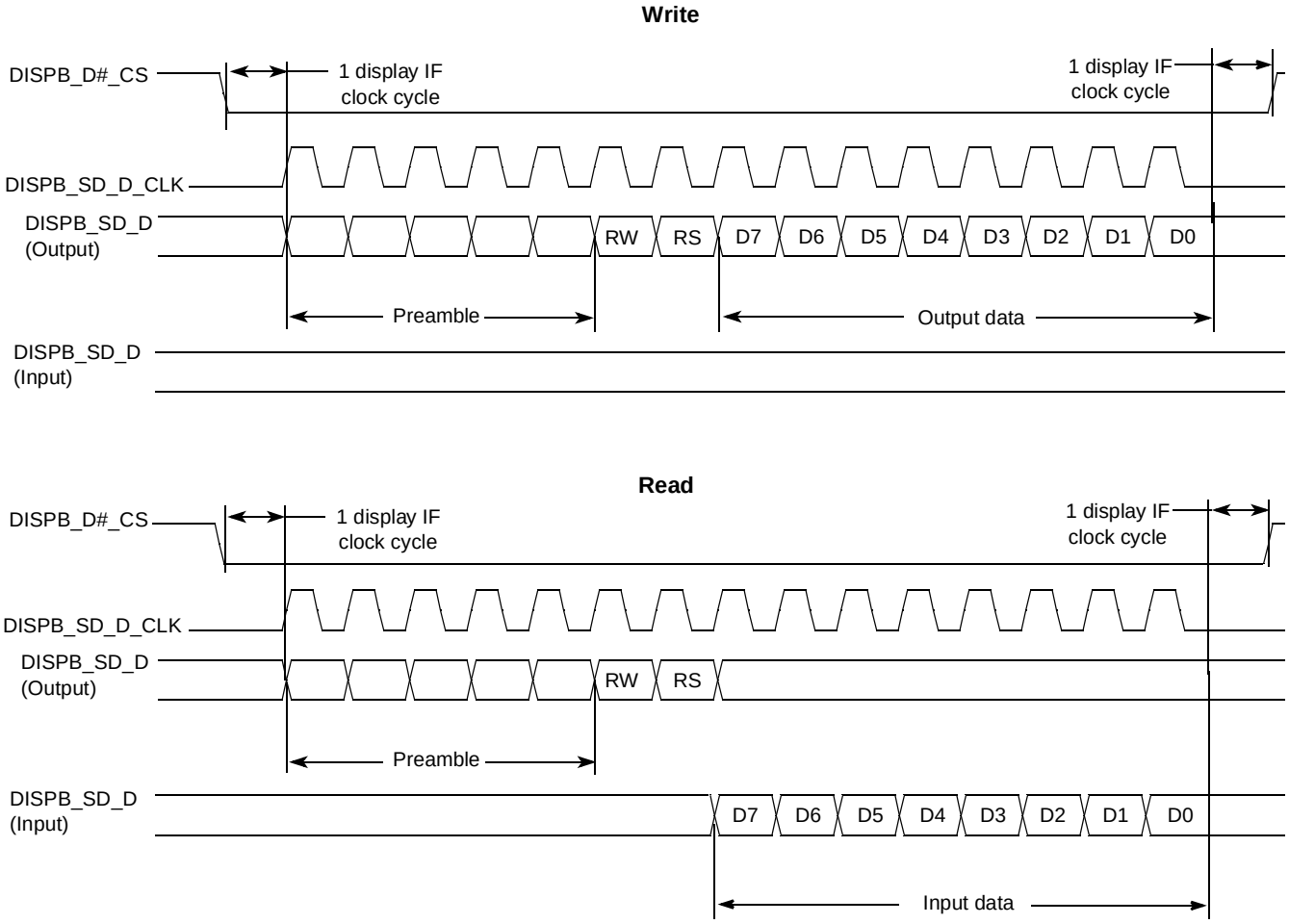


Figure 61. 4-Wire Serial Interface Timing Diagram

Figure 62 depicts timing of the 5-wire serial interface (Type 1). For this interface, a separate RS line is added. When a burst is transmitted within single active chip select interval, the RS can be changed at boundaries of words.

Figure 63 depicts timing of the 5-wire serial interface (Type 2). For this interface, a separate RS line is added. When a burst is transmitted within single active chip select interval, the RS can be changed at boundaries of words.

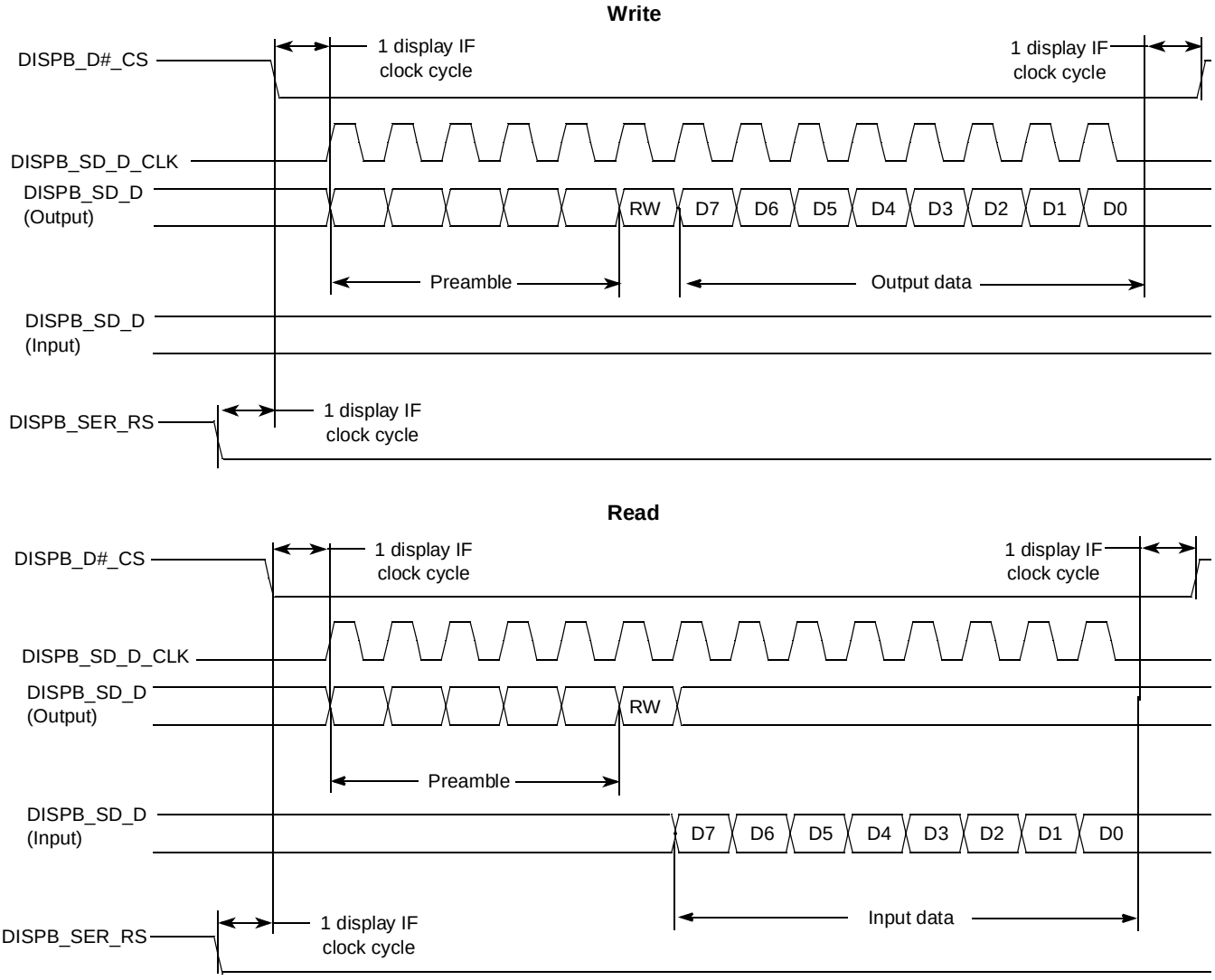


Figure 63. 5-Wire Serial Interface (Type 2) Timing Diagram

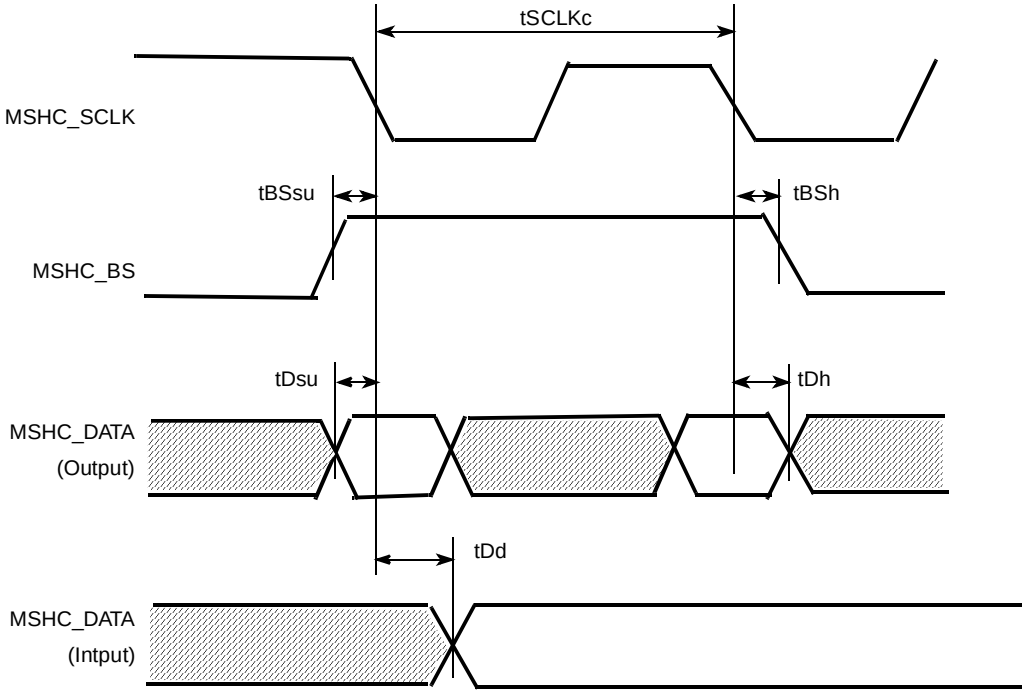


Figure 67. Transfer Operation Timing Diagram (Parallel)

NOTE

The Memory Stick Host Controller is designed to meet the timing requirements per Sony's *Memory Stick Pro Format Specifications* document. Tables in this section details the specifications requirements for parallel and serial modes, and not the MCIMX31 timing.

Table 51. Serial Interface Timing Parameters[1]

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_SCLK	Cycle	tSCLKc	50	—	ns
	H pulse length	tSCLKwh	15	—	ns
	L pulse length	tSCLKwl	15	—	ns
	Rise time	tSCLKr	—	10	ns
	Fall time	tSCLKf	—	10	ns
MSHC_BS	Setup time	tBSsu	5	—	ns
	Hold time	tBSh	5	—	ns
MSHC_DATA	Setup time	tDsu	5	—	ns
	Hold time	tDh	5	—	ns
	Output delay time	tDd	—	15	ns

1 Timing is guaranteed for NVCC from 2.7 through 3.1 V and up to a maximum overdrive NVCC of 3.3 V. See NVCC restrictions described in Table 8, "Operating Ranges," on page 13.

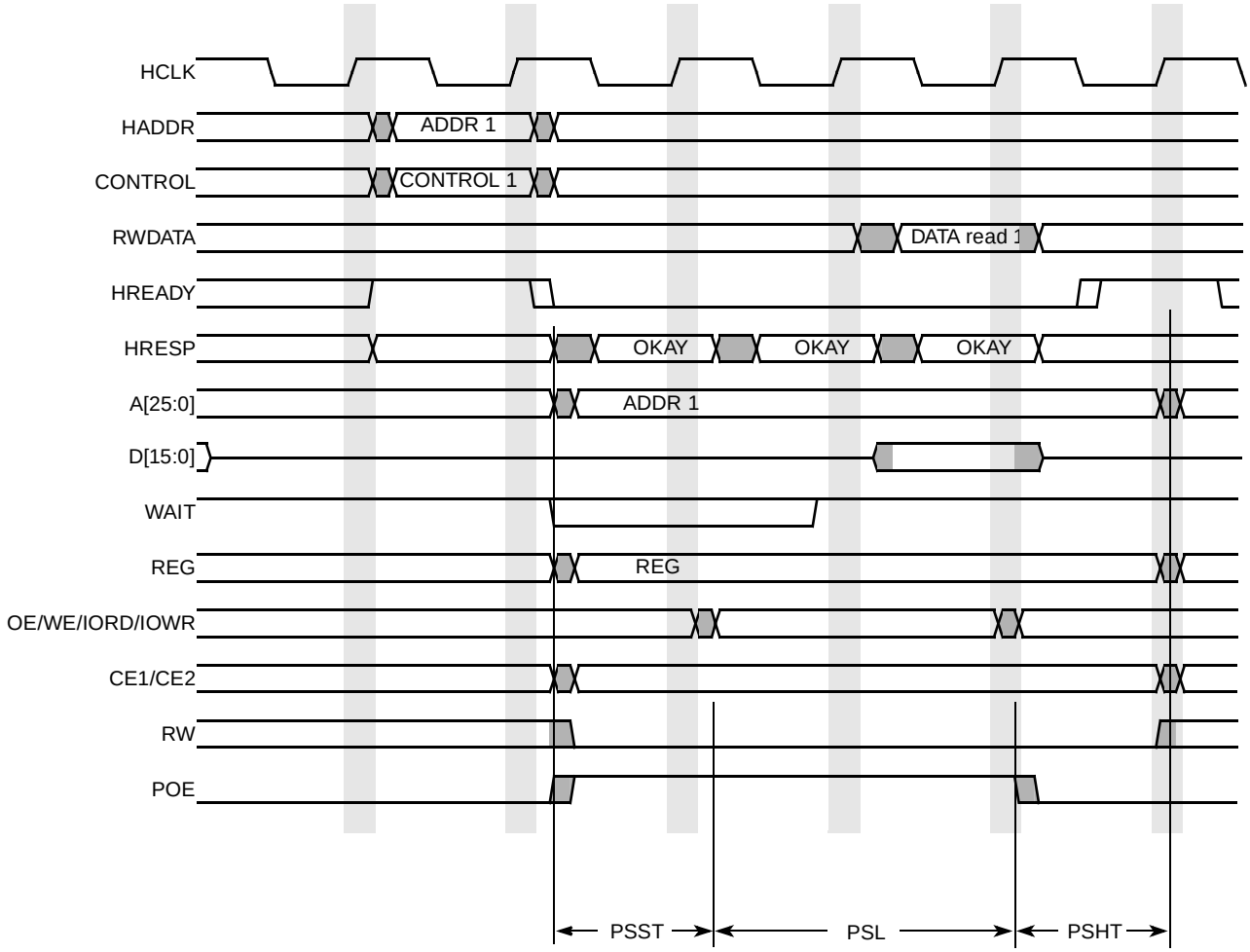


Figure 69. Read Accesses Timing Diagram—PSHT=1, PSST=1

Table 53. PCMCIA Write and Read Timing Parameters

Symbol	Parameter	Min	Max	Unit
PSHT	PCMCIA strobe hold time	0	63	clock
PSST	PCMCIA strobe set up time	1	63	clock
PSL	PCMCIA strobe length	1	128	clock

4.3.18 PWM Electrical Specifications

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Table 60. SSI Receiver with Internal Clock Timing Parameters

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6	ns
SS7	(Rx) CK high to FS (bl) high	—	15.0	ns
SS9	(Rx) CK high to FS (bl) low	—	15.0	ns
SS11	(Rx) CK high to FS (wl) high	—	15.0	ns
SS13	(Rx) CK high to FS (wl) low	—	15.0	ns
SS20	SRXD setup time before (Rx) CK low	10.0	—	ns
SS21	SRXD hold time after (Rx) CK low	0	—	ns
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6	—	ns
SS49	Oversampling clock rise time	—	3	ns
SS50	Oversampling clock low period	6	—	ns
SS51	Oversampling clock fall time	—	3	ns

Table 62. SSI Receiver with External Clock Timing Parameters (continued)

ID	Parameter	Min	Max	Unit
SS28	(Rx) CK high to FS (bl) high	–10.0	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10.0	—	ns
SS32	(Rx) CK high to FS (wl) high	–10.0	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10.0	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10.0	—	ns
SS41	SRXD hold time after (Rx) CK low	2.0	—	ns

4.3.23 USB Electrical Specifications

This section describes the electrical information of the USBOTG port. The OTG port supports both serial and parallel interfaces.

The high speed (HS) interface is supported via the ULPI (Ultra Low Pin Count Interface). Figure 84 depicts the USB ULPI timing diagram, and Table 63 lists the timing parameters.

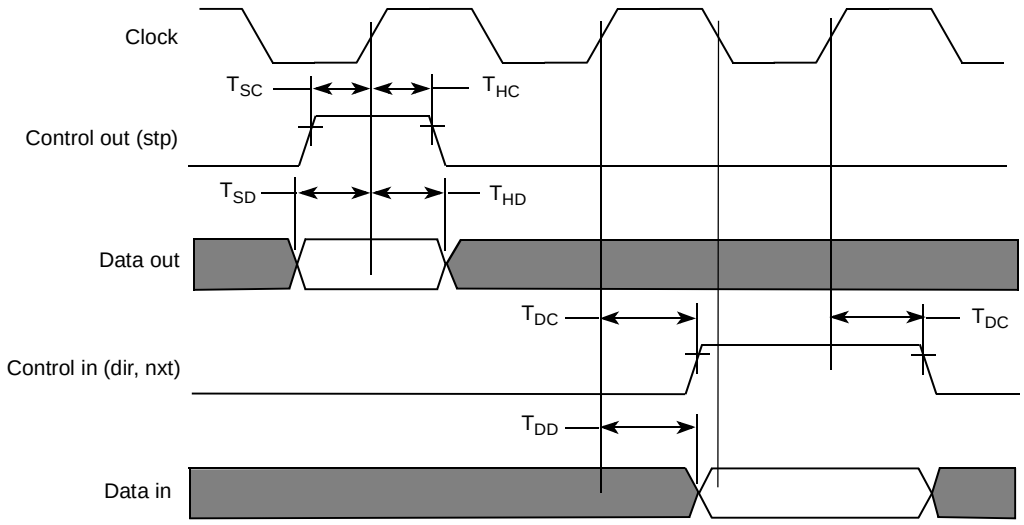


Figure 84. USB ULPI Interface Timing Diagram

Table 63. USB ULPI Interface Timing Specification[1]

Parameter	Symbol	Min	Max	Units
Setup time (control in, 8-bit data in)	T_{SC}, T_{SD}	6	—	ns
Hold time (control in, 8-bit data in)	T_{HC}, T_{HD}	0	—	ns
Output delay (control out, 8-bit data out)	T_{DC}, T_{DD}	—	9	ns

1 Timing parameters are given as viewed by transceiver side.

Table 65. 14 x 14 BGA Signal ID by Ball Grid Location (continued)

Signal ID	Ball Location
CSPI3_SCLK	E1
CSPI3_SPI_RDY	G6
CTS1	B11
CTS2	G13
D0	AB2
D1	Y3
D10	Y1
D11	U7
D12	W2
D13	V3
D14	W1
D15	U6
D2	AB1
D3	W6
D3_CLS	R20
D3_REV	T26
D3_SPL	U25
D4	AA2
D5	V7
D6	AA1
D7	W3
D8	Y2
D9	V6
DCD_DCE1	B12
DCD_DTE1	B13
$\overline{DE}$	C18
DQM0	AE19
DQM1	AD19
DQM2	AA20
DQM3	AE18
DRDY0	N26
DSR_DCE1	A11
DSR_DTE1	A12
DTR_DCE1	C11
DTR_DCE2	F12
DTR_DTE1	C12
DVFS0	E25
DVFS1	G24
EB0	W21
EB1	Y24
ECB	AD23
FPSHIFT	N21
GPIO1_0	F18
GPIO1_1	B23
GPIO1_2	C20
LD7	W25

Signal ID	Ball Location
GPIO1_3	F25
GPIO1_4	F19
GPIO1_5 (PWR RDY)	B24
GPIO1_6	A23
GPIO3_0	K21
GPIO3_1	H26
HSYNC	N25
I2C_CLK	J24
I2C_DAT	H25
IOIS16	J3
KEY_COL0	C15
KEY_COL1	B17
KEY_COL2	G15
KEY_COL3	A17
KEY_COL4	C16
KEY_COL5	B18
KEY_COL6	F15
KEY_COL7	A18
KEY_ROW0	F13
KEY_ROW1	B15
KEY_ROW2	C14
KEY_ROW3	A15
KEY_ROW4	G14
KEY_ROW5	B16
KEY_ROW6	F14
KEY_ROW7	A16
L2PG	See VPG1
LBA	AE22
LCS0	P26
LCS1	P21
LD0	T24
LD1	U26
LD10	V24
LD11	Y25
LD12	Y26
LD13	V21
LD14	AA25
LD15	W24
LD16	AA26
LD17	V20
LD2	T21
LD3	V25
LD4	T20
LD5	V26
LD6	U24
SCK6	T2

Table 68. 19 x 19 BGA Signal ID by Ball Grid Location (continued)

Signal ID	Ball Location
BOOT_MODE0	F17
BOOT_MODE1	C21
BOOT_MODE2	D20
BOOT_MODE3	F18
BOOT_MODE4	E20
CAPTURE	D18
CAS	AA20
CE_CONTROL	D12
CKIH	F23
CSPI3_SCLK	H7
CSPI3_SPI_RDY	F4
CTS1	A9
CTS2	C12
D0	U6
D1	W4
D10	V1
D11	U4
D12	U3
D13	R6
D14	U2
D15	U1
D2	W3
D3	V4
D3_CLS	P20
D3_REV	P21
D3_SPL	N17
D4	T7
D5	W2
D6	V3
D7	W1
D8	T6
D9	V2
DCD_DCE1	C10
DCD_DTE1	D11
$\overline{DE}$	D16
DQM0	AB19
DQM1	Y16
DQM2	AA18
DQM3	AB18
DRDY0	M17
DSR_DCE1	B10
DSR_DTE1	A11
DTR_DCE1	F10
DTR_DCE2	C11
DTR_DTE1	A10
DVFS0	E22
CSPI2_MISO	B4
CSPI2_MOSI	D5
CSPI2_SCLK	B5
CSPI2_SPI_RDY	D6
CSPI2_SS0	C5
CSPI2_SS1	A4
CSPI2_SS2	F7
CSPI3_MISO	D2
CSPI3_MOSI	E4
GPIO1_3	G20
GPIO1_4	D21
GPIO1_5 (PWR RDY)	D19
GPIO1_6	G18
GPIO3_0	G23
GPIO3_1	K17
HSYNC	L23
I2C_CLK	J18
I2C_DAT	K18
IOIS16	J7
KEY_COL0	A15
KEY_COL1	B15
KEY_COL2	D14
KEY_COL3	C15
KEY_COL4	F13
KEY_COL5	A16
KEY_COL6	B16
KEY_COL7	A17
KEY_ROW0	A13
KEY_ROW1	B13
KEY_ROW2	C13
KEY_ROW3	A14
KEY_ROW4	F12
KEY_ROW5	D13
KEY_ROW6	B14
KEY_ROW7	C14
L2PG	See VPG1
LBA	V17
LCS0	M22
LCS1	N23
LD0	R23
LD1	R22
LD10	U22
LD11	R18
LD12	U20
LD13	V23
LD14	V22

6 Product Documentation

This Data Sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com.

MCIMX31 Product Brief (order number MCIMX31PB)

MCIMX31 Reference Manual (order number MCIMX31RM)

MCIMX31 Chip Errata (order number MCIMX31CE)

The Freescale manuals are available on the Freescale Semiconductors Web site at http://www.freescale.com/imx. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered. ARM Ltd. documentation is available from http://www.arm.com.

7 Revision History

Table 71 summarizes revisions to this document since the release of Rev. 4.1.

Table 71. Revision History

Rev.	Location	Revision
4.3	Table 1, "Ordering Information," on page 3	Added a footnote and new part numbers for silicon revision 2.0.1.
4.2	Global	Replaced all references to silicon 2.0 with silicon revision 2.0.1.
4.2	Table 1, "Ordering Information," on page 3	Added new part numbers for revision 2.0.1.
4.2	Section 1.2.1, “Feature Differences Between Mask Sets	Updated for revision 2.0.1.
4.2	Table 8, "Operating Ranges," on page 13	Updated Core Operating voltage ranges and respective footnotes.
4.2	Table 12, "Current Consumption for –40×C to 85×C, for Silicon Revision 2.0.1," on page 16	Updated for silicon revision 2.0.1.
4.2	Table 13, "Current Consumption for –20×C to 70×C, for Silicon Revision 2.0.1," on page 17	Updated values for silicon revision 2.0.1.
4.2	Section 3, “Signal Descriptions	Removed reference to the TTM_PAD as it is no longer connected.