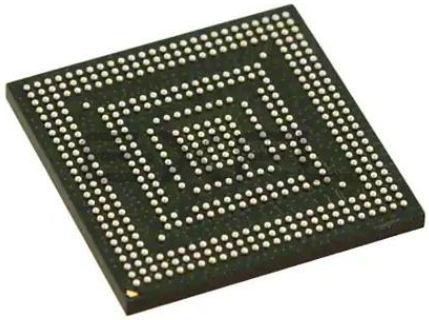

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, MPEG-4, VFP
RAM Controllers	DDR
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, Keypad, LCD
Ethernet	-
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Random Number Generator, RTIC, Secure Fusebox, Secure JTAG, Secure Memory
Package / Case	457-LFBGA
Supplier Device Package	457-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx31cvkn5dr2

1.2 Ordering Information

Table 1 provides the ordering information for the MCIMX31.

Table 1. Ordering Information[1]

Part Number	Silicon Revision[2, 3, 4,5]	Device Mask	Operating Temperature Range (°C)	Package[6]
MCIMX31DVKN5D!	2.0.1	M91E	–20 to 70	14 x 14 mm, 0.5 mm pitch, MAPBGA-457, Case 1581
MCIMX31LDVKN5D!	2.0.1	M91E	–20 to 70	
MCIMX31CVKN5D!	2.0.1	M91E	–40 to 85	
MCIMX31LCVKN5D!	2.0.1	M91E	–40 to 85	
MCIMX31DVMN5D!	2.0.1	M91E	–20 to 70	19 x 19 mm, 0.8 mm pitch, Case 1931
MCIMX31LDVMN5D!	2.0.1	M91E	–20 to 70	
MCIMX31CJKN5D	2.0.1	M91E	–40 to 85	14 x 14 mm, 0.5 mm pitch, MAPBGA-457, Case 1581
MCIMX31LCJKN5D	2.0.1	M91E	–40 to 85	

1 Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: Indicated by the Icon (!)

2 Information on reading the silicon revision register can be found in the IC Identification (IIM) chapter of the Reference Manual, see Section 6, “Product Documentation.”

3 Errata and fix information of the various mask sets can be found in the standard MCIMX31 Chip Errata, see Section 6, “Product Documentation.”

4 Changes in output buffer characteristics can be found in the I/O Setting Exceptions and Special Pad Descriptions table in the Reference Manual, see Section 6, “Product Documentation.”

5 JTAG functionality is not tested nor guaranteed at -40°C.

6 Case 1581 and 1931 are RoHS compliant, lead-free, MSL = 3.

1.2.1 Feature Differences Between Mask Sets

There are no silicon differences between revisions 2.0 and 2.0.1. The main difference is an updated iROM code which supports USB-HS, SD/MMC boot modes and corrects some boot mode related erratas.

2.2 Module Inventory

Table 3 shows an alphabetical listing of the modules in the multimedia applications processor. For extended descriptions of the modules, see the reference manual. A cross-reference is provided to the electrical specifications and timing information for each module with external signal connections.

Table 3. Digital and Analog Modules

Block Mnemonic	Block Name	Functional Grouping	Brief Description	Section/ Page
1-Wire®	1-Wire Interface	Connectivity Peripheral	The 1-Wire module provides bi-directional communication between the ARM11 core and external 1-Wire devices.	4.3.4/24
ATA	Advanced Technology (AT) Attachment	Connectivity Peripheral	The ATA block is an AT attachment host interface. It is designed to interface with IDE hard disc drives and ATAPI optical disc drives.	4.3.5/25
AUDMUX	Digital Audio Multiplexer	Multimedia Peripheral	The AUDMUX interconnections allow multiple, simultaneous audio/voice/data flows between the ports in point-to-point or point-to-multipoint configurations.	4.3.6/34
CAMP	Clock Amplifier Module	Clock	The CAMP converts a square wave/sinusoidal input into a rail-to-rail square wave. The output of CAMP feeds the predivider.	4.3.3/23
CCM	Clock Control Module	Clock	The CCM provides clock, reset, and power management control for the MCIMX31.	—
CSPI	Configurable Serial Peripheral Interface (x 3)	Connectivity Peripheral	The CSPI is equipped with data FIFOs and is a master/slave configurable serial peripheral interface module, capable of interfacing to both SPI master and slave devices.	4.3.7/34
DPLL	Digital Phase Lock Loop	Clock	The DPLLs produce high-frequency on-chip clocks with low frequency and phase jitters. **Note:** External clock sources provide the reference frequencies.	4.3.8/35
ECT	Embedded Cross Trigger	Debug	The ECT is composed of three CTIs (Cross Trigger Interface) and one CTM (Cross Trigger Matrix—key in the multi-core and multi-peripheral debug strategy.	—
EMI	External Memory Interface	Memory Interface (EMI)	The EMI includes • Multi-Master Memory Interface (M3IF) • Enhanced SDRAM Controller (ESDCTL) • NAND Flash Controller (NFC) • Wireless External Interface Module (WEIM)	— 4.3.9.3/44, 4.3.9.1/36, 4.3.9.2/39
EPIT	Enhanced Periodic Interrupt Timer	Timer Peripheral	The EPIT is a 32-bit “set and forget” timer which starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention.	—
ETM	Embedded Trace Macrocell	Debug/Trace	The ETM (from ARM, Ltd.) supports real-time instruction and data tracing by way of ETM auxiliary I/O port.	4.3.10/52
FIR	Fast InfraRed Interface	Connectivity Peripheral	This FIR is capable of establishing a 0.576 Mbit/s, 1.152 Mbit/s or 4 Mbit/s half duplex link via a LED and IR detector. It supports 0.576 Mbit/s, 1.152 Mbit/s medium infrared (MIR) physical layer protocol and 4Mbit/s fast infrared (FIR) physical layer protocol defined by IrDA, Rev. 1.4.	4.3.11/53

4 Electrical Characteristics

This section provides the device-level and module-level electrical characteristics for the MCIMX31.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 4 for a quick reference to the individual tables and sections.

Table 4. MCIMX31 Chip-Level Conditions

For these characteristics, …	Topic appears …
Table 5, “Absolute Maximum Ratings”	on page 10
Table 7, “Thermal Resistance Data—19 × 19 mm Package”	on page 11
Table 8, “Operating Ranges”	on page 13
Table 9, “Specific Operating Ranges for Silicon Revision 2.0.1”	on page 14
Table 10, “Interface Frequency”	on page 14
Section 4.1.1, “Supply Current Specifications”	on page 16
Section 4.2, “Supply Power-Up/Power-Down Requirements and Restrictions”	on page 18

CAUTION

Stresses beyond those listed under Table 5 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Table 8, "Operating Ranges," on page 13 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply Voltage (Core)	$QVCC_{max}$	–0.5	1.65	V
Supply Voltage (I/O)	$NVCC_{max}$	–0.5	3.3	V
Input Voltage Range	V_{Imax}	–0.5	NVCC +0.3	V
Storage Temperature	$T_{storage}$	–40	125	^{o}C
ESD Damage Immunity:				
Human Body Model (HBM)	V_{esd}	—	1500	V
Machine Model (MM)		—	200	
Charge Device Model (CDM)		—	500	
Offset voltage allowed in run mode between core supplies.	V_{core_offset}[1]	—	15	mV

[1] The offset is the difference between all core voltage pair combinations of QVCC, QVCC1, and QVCC4.

Table 14. GPIO DC Electrical Parameters (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Low-level output current, fast slew rate	I_{OL_F}	V_{OL}=0.2*NVCC Std Drive High Drive Max Drive	 4 6 8	—	—	mA
High-Level DC input voltage	V_{IH}	—	0.7*NVCC	—	NVCC	V
Low-Level DC input voltage	V_{IL}	—	0	—	0.3*QVCC	V
Input Hysteresis	V_{HYS}	Hysteresis enabled	0.25	—	—	V
Schmitt trigger VT+	V_T +	Hysteresis enabled	0.5*QVCC	—	—	V
Schmitt trigger VT–	V_T –	Hysteresis enabled	—	—	0.5*QVCC	V
Pull-up resistor (100 kΩ PU)	R_{PU}	—	—	100	—	kΩ
Pull-down resistor (100 kΩ PD)	R_{PD}	—	—	100	—	
Input current (no PU/PD)	I_{IN}	V_I = NVCC or GND	—	—	±1	µA
Input current (100 kΩ PU)	I_{IN}	V_I = 0 V_I = NVCC	—	—	25 0.1	µA µA
Input current (100 kΩ PD)	I_{IN}	V_I = 0 V_I = NVCC	—	—	0.25 28	µA µA
Tri-state leakage current	I_{OZ}	V_I = NVCC or GND I/O = High Z	—	—	±2	µA

The MCIMX31 I/O parameters appear in Table 15 for DDR (Double Data Rate). See Table 8, "Operating Ranges," on page 13 for temperature and supply voltage ranges.

NOTE

NVCC for Table 15 refers to NVCC2, NVCC21, and NVCC22.

Table 15. DDR (Double Data Rate) I/O DC Electrical Parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
High-level output voltage	V_{OH}	I_{OH} = –1 mA	NVCC –0.12	—	—	V
		I_{OH} = specified Drive	0.8*NVCC	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 1 mA	—	—	0.08	V
		I_{OL} = specified Drive	—	—	0.2*NVCC	V
High-level output current	I_{OH}	V_{OH}=0.8*NVCC Std Drive High Drive Max Drive DDR Drive[1]	 –3.6 –7.2 –10.8 –14.4	—	—	mA
Low-level output current	I_{OL}	V_{OL}=0.2*NVCC Std Drive High Drive Max Drive DDR Drive[1]	 3.6 7.2 10.8 14.4	—	—	mA

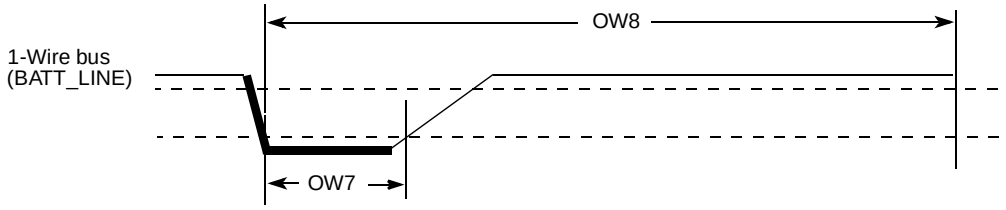

Figure 8. Write 1 Sequence Timing Diagram

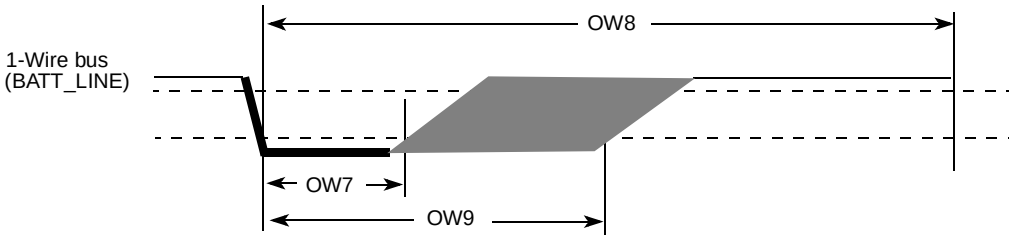

Figure 9. Read Sequence Timing Diagram

Table 22. WR1/RD Timing Parameters

ID	Parameter	Symbol	Min	Typ	Max	Units
OW7	Write 1 / Read Low Time	t_{LOW1}	1	5	15	µs
OW8	Transmission Time Slot	t_{SLOT}	60	117	120	µs
OW9	Release Time	$t_{RELEASE}$	15	—	45	µs

4.3.5 ATA Electrical Specifications (ATA Bus, Bus Buffers)

This section discusses ATA parameters. For a detailed description, refer to the ATA specification.

The user needs to use level shifters for 3.3 Volt or 5.0 Volt compatibility on the ATA interface.

The use of bus buffers introduces delay on the bus and introduces skew between signal lines. These factors make it difficult to operate the bus at the highest speed (UDMA-5) when bus buffers are used. If fast UDMA mode operation is needed, this may not be compatible with bus buffers.

Another area of attention is the slew rate limit imposed by the ATA specification on the ATA bus. According to this limit, any signal driven on the bus should have a slew rate between 0.4 and 1.2 V/ns with a 40 pF load. Not many vendors of bus buffers specify slew rate of the outgoing signals.

When bus buffers are used, the ata_data bus buffer is special. This is a bidirectional bus buffer, so a direction control signal is needed. This direction control signal is ata_buffer_en. When its high, the bus should drive from host to device. When its low, the bus should drive from device to host. Steering of the signal is such that contention on the host and device tri-state busses is always avoided.

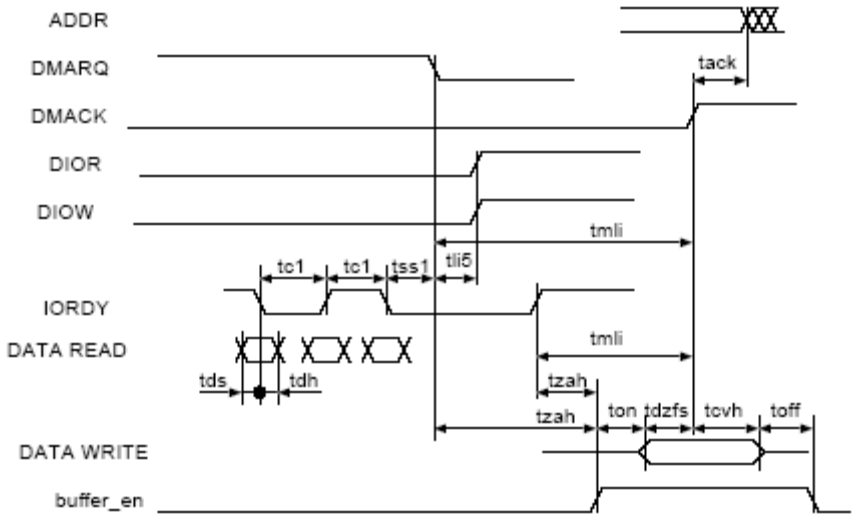

Figure 16. UDMA In Device Terminates Transfer Timing Diagram

Table 27. UDMA In Burst Timing Parameters

ATA Parameter	Parameter from Figure 14, Figure 15, Figure 16	Description	Controlling Variable
tack	tack	tack (min) = (time_ack * T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min) = (time_env * T) – (tskew1 + tskew2) tenv (max) = (time_env * T) + (tskew1 + tskew2)	time_env
tds	tds1	tds – (tskew3) – ti_ds > 0	tskew3, ti_ds, ti_dh should be low enough
tdh	tdh1	tdh – (tskew3) – ti_dh > 0	
tcyc	tc1	(tcyc – tskew) > T	T big enough
trp	trp	trp (min) = time_rp * T – (tskew1 + tskew2 + tskew6)	time_rp
—	tx1[1]	(time_rp * T) – (tco + tsu + 3T + 2 *tbuf + 2*tcable2) > trfs (drive)	time_rp
tmli	tmli1	tmli1 (min) = (time_mlix + 0.4) * T	time_mlix
tzah	tzah	tzah (min) = (time_zah + 0.4) * T	time_zah
tdzfs	tdzfs	tdzfs = (time_dzfs * T) – (tskew1 + tskew2)	time_dzfs
tcvh	tcvh	tcvh = (time_cvh *T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on * T – tskew1 toff = time_off * T – tskew1	—

1 There is a special timing requirement in the ATA host that requires the internal DIOW to go only high 3 clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

2. Make ton and toff big enough to avoid bus contention

4.3.6 AUDMUX Electrical Specifications

The AUDMUX provides a programmable interconnect logic for voice, audio and data routing between internal serial interfaces (SSI) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is hence governed by the SSI module. Please refer to their respective electrical specifications.

4.3.7 CSPI Electrical Specifications

This section describes the electrical information of the CSPI.

4.3.7.1 CSPI Timing

Figure 20 and Figure 21 depict the master mode and slave mode timings of CSPI, and Table 29 lists the timing parameters.

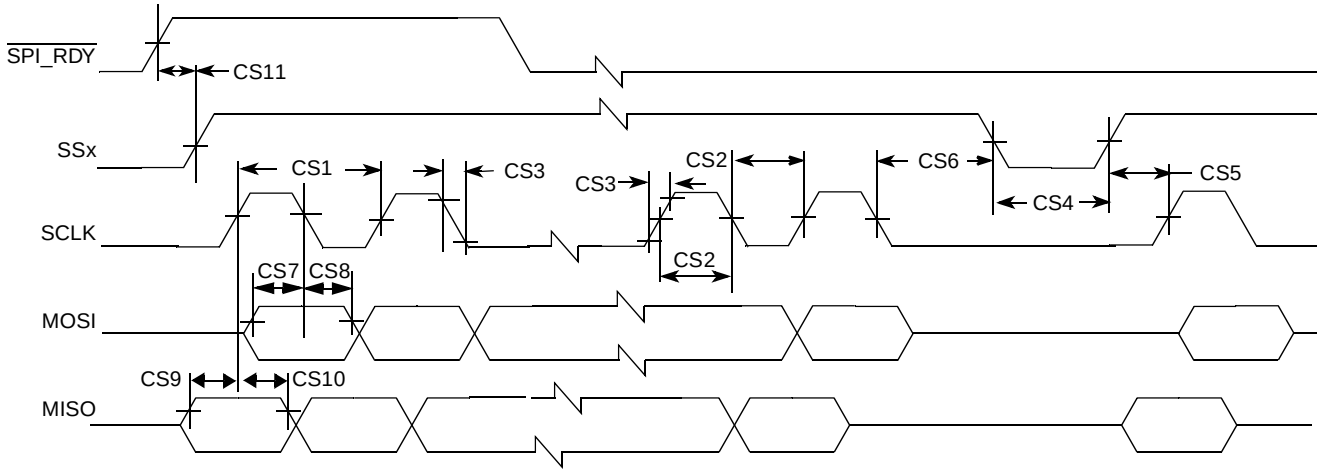

Figure 20. CSPI Master Mode Timing Diagram

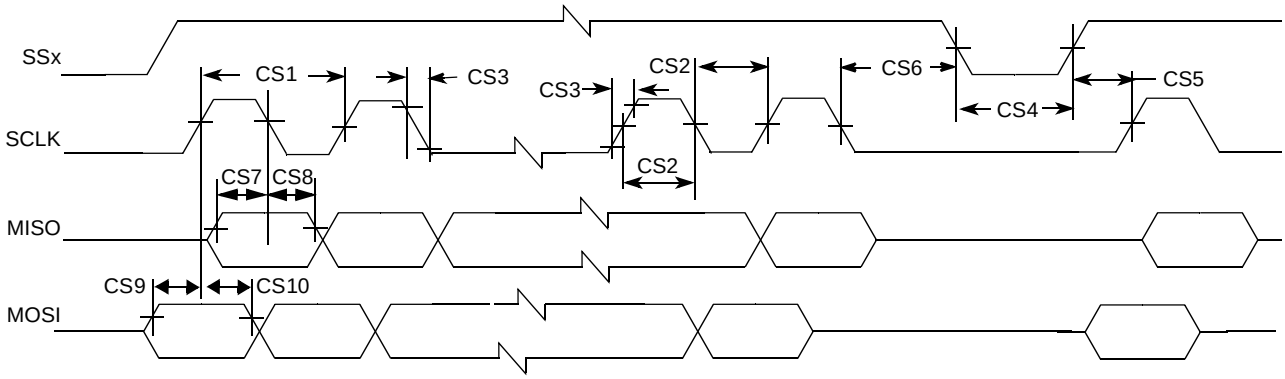

Figure 21. CSPI Slave Mode Timing Diagram

Table 34. SDR SDRAM Write Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
SD13	Data setup time	tDS	2.0	—	ns
SD14	Data hold time	tDH	1.3	—	ns

[1] SD11 and SD12 are determined by SDRAM controller register settings.

NOTE

SDR SDRAM CLK parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 34 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

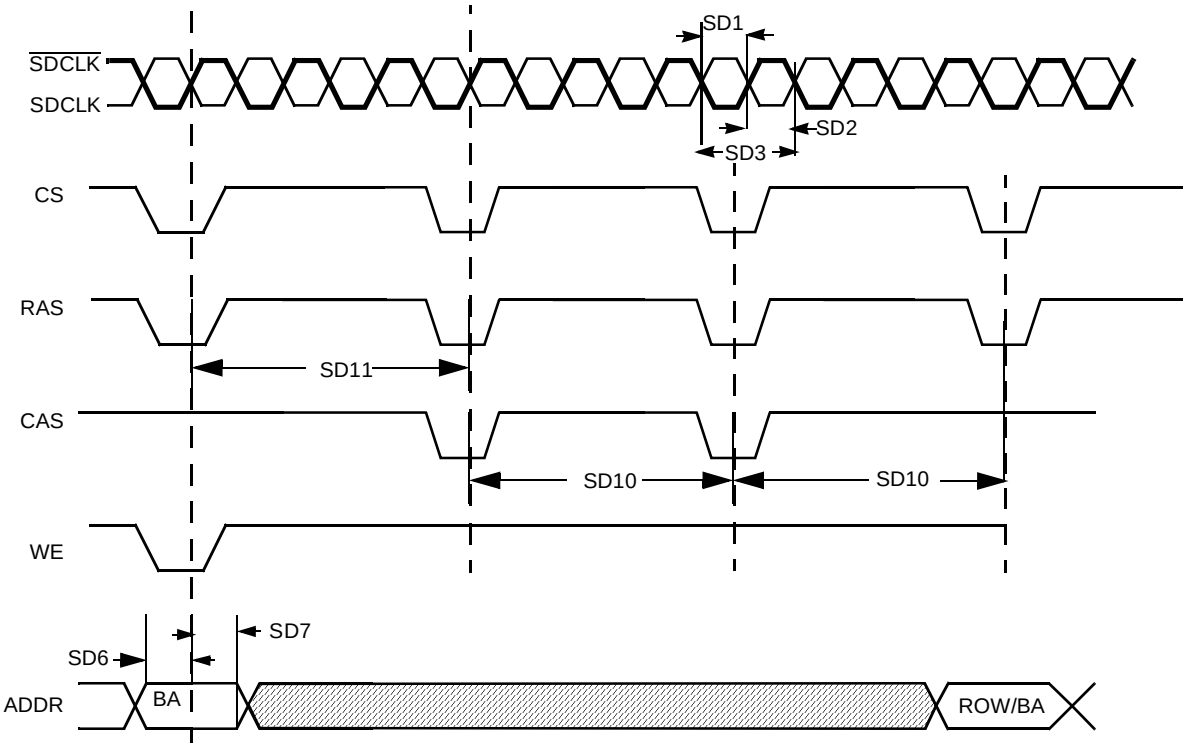

Figure 35. SDRAM Refresh Timing Diagram

Table 35. SDRAM Refresh Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	$\overline{\text{SDRAM clock low-level width}}$	tCL	3.4	4.1	ns

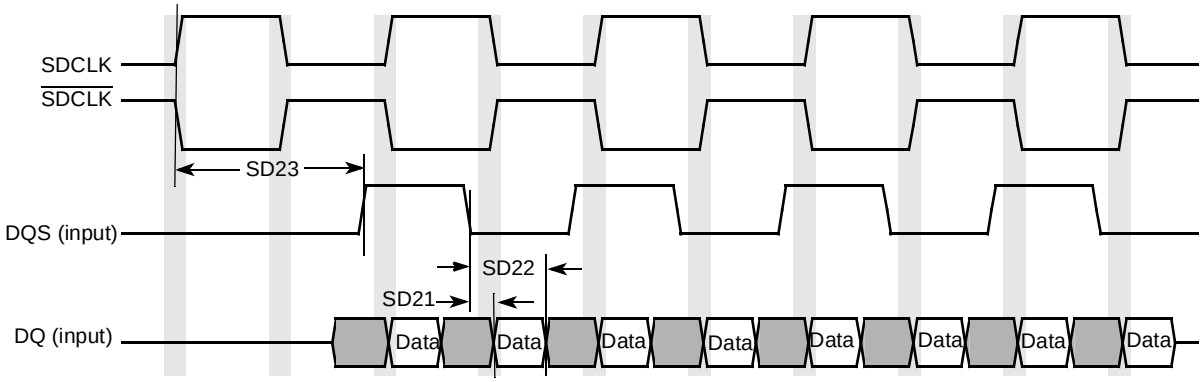

Figure 38. Mobile DDR SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram

Table 38. Mobile DDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
SD21	DQS – DQ Skew (defines the Data valid window in read cycles related to DQS).	tDQSQ	—	0.85	ns
SD22	DQS DQ HOLD time from DQS	tQH	2.3	—	ns
SD23	DQS output access time from SDCLK posedge	tDQSCK	—	6.7	ns

NOTE

SDRAM CLK and DQS related parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 38 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

4.3.10 ETM Electrical Specifications

ETM is an ARM protocol. The timing specifications in this section are given as a guide for a TPA that supports TRACECLK frequencies up to 133 MHz.

Figure 39 depicts the TRACECLK timings of ETM, and Table 39 lists the timing parameters.

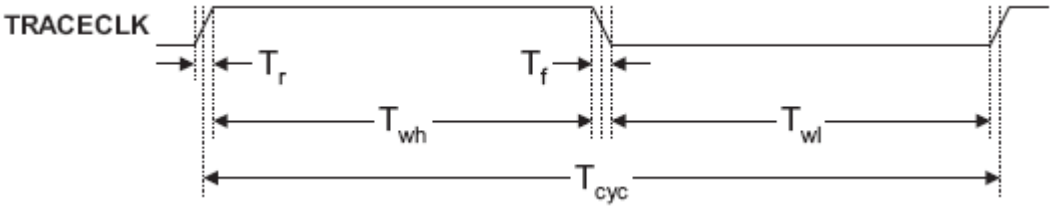

Figure 39. ETM TRACECLK Timing Diagram

4.3.14 IPU—Sensor Interfaces

4.3.14.1 Supported Camera Sensors

Table 43 lists the known supported camera sensors at the time of publication.

Table 43. Supported Camera Sensors[1]

Vendor	Model
Conexant	CX11646, CX20490[2], CX20450[2]
Agilant	HDCP–2010, ADCS–1021[2], ADCS–1021[2]
Toshiba	TC90A70
ICMedia	ICM202A, ICM102[2]
iMagic	IM8801
Transchip	TC5600, TC5600J, TC5640, TC5700, TC6000
Fujitsu	MB86S02A
Micron	MI–SOC–0133
Matsushita	MN39980
STMicro	W6411, W6500, W6501[2], W6600[2], W6552[2], STV0974[2]
OmniVision	OV7620, OV6630
Sharp	LZ0P3714 (CCD)
Motorola	MC30300 (Python)[2], SCM20014[2], SCM20114[2], SCM22114[2], SCM20027[2]
National Semiconductor	LM9618[2]

1 Freescale Semiconductor does not recommend one supplier over another and in no way suggests that these are the only camera suppliers.

2 These sensors not validated at time of publication.

4.3.14.2 Functional Description

There are three timing modes supported by the IPU.

4.3.14.2.1 Pseudo BT.656 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the SENSB_VSYNC and SENSB_HSYNC signals. The timing syntax is defined by the BT.656 standard.

This operation mode follows the recommendations of ITU BT.656 specifications. The only control signal used is SENSB_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering SENSB_VSYNC and SENSB_HSYNC signals for internal use.

Table 45. Supported Display Components[1]

Type	Vendor	Model
TFT displays (memory-less)	Sharp (HR-TFT Super Mobile LCD family)	LQ035Q7 DB02, LM019LC1Sxx
	Samsung (QCIF and QVGA TFT modules for mobile phones)	LTS180S1-HF1, LTS180S3-HF1, LTS350Q1-PE1, LTS350Q1-PD1, LTS220Q1-HE1[2]
	Toshiba (LTM series)	LTM022P806[2], LTM04C380K[2], LTM018A02A[2], LTM020P332[2], LTM021P337[2], LTM019P334[2], LTM022A783[2], LTM022A05ZZ[2]
	NEC	NL6448BC20-08E, NL8060BC31-27
Display controllers	Epson	S1D15xxx series, S1D19xxx series, S1D13713, S1D13715
	Solomon Systech	SSD1301 (OLED), SSD1828 (LDCD)
	Hitachi	HD66766, HD66772
	ATI	W2300
Smart display modules	Epson	L1F10043 T[2], L1F10044 T[2], L1F10045 T[2], L2D22002[2], L2D20014[2], L2F50032[2], L2D25001 T[2]
	Hitachi	120 160 65K/4096 C-STN (#3284 LTD-1398-2) based on HD 66766 controller
	Densitron Europe LTD	All displays with MPU 80/68K series interface and serial peripheral interface
	Sharp	LM019LC1Sxx
	Sony	ACX506AKM
Digital video encoders (for TV)	Analog Devices	ADV7174/7179
	Crystal (Cirrus Logic)	CS49xx series
	Focus	FS453/4

1 Freescale Semiconductor does not recommend one supplier over another and in no way suggests that these are the only display component suppliers.

2 These display components not validated at time of publication.

4.3.15.2 Synchronous Interfaces

4.3.15.2.1 Interface to Active Matrix TFT LCD Panels, Functional Description

Figure 45 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DISPB_D3_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, DISPB_D3_CLK runs continuously.
- DISPB_D3_HSYNC causes the panel to start a new line.
- DISPB_D3_VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.

- DISPB_D3_DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.

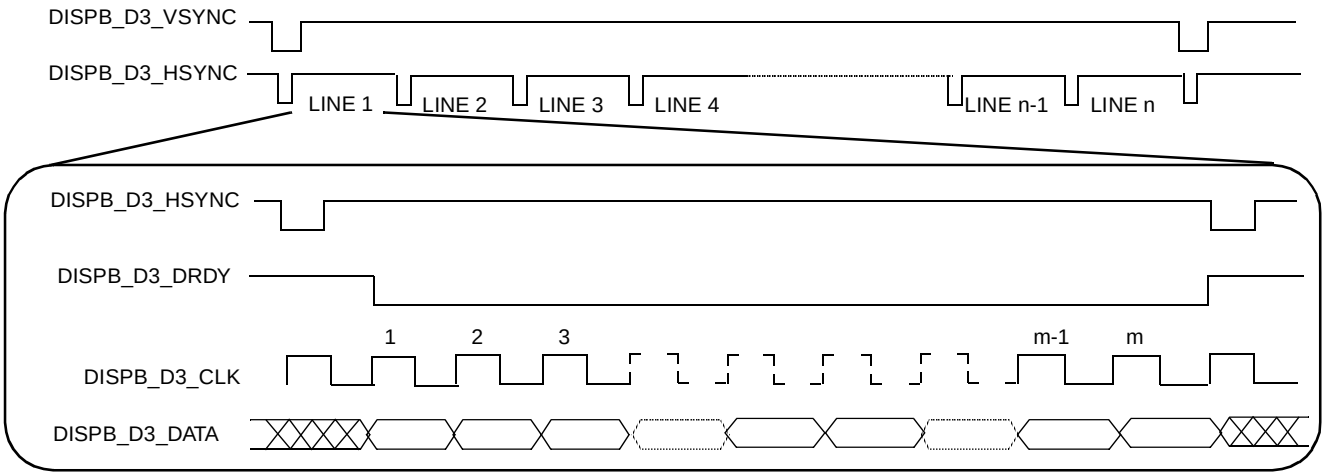

Figure 45. Interface Timing Diagram for TFT (Active Matrix) Panels

4.3.15.2.2 Interface to Active Matrix TFT LCD Panels, Electrical Characteristics

Figure 46 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All figure parameters shown are programmable. The timing images correspond to inverse polarity of the DISPB_D3_CLK signal and active-low polarity of the DISPB_D3_HSYNC, DISPB_D3_VSYNC and DISPB_D3_DRDY signals.

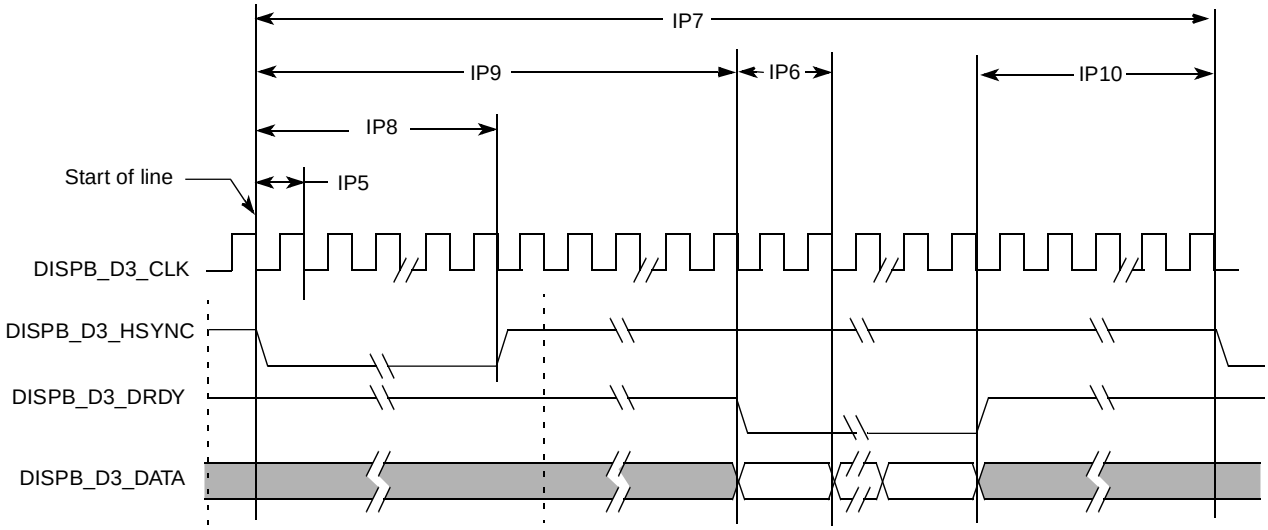

Figure 46. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 47 depicts the vertical timing (timing of one frame). All figure parameters shown are programmable.

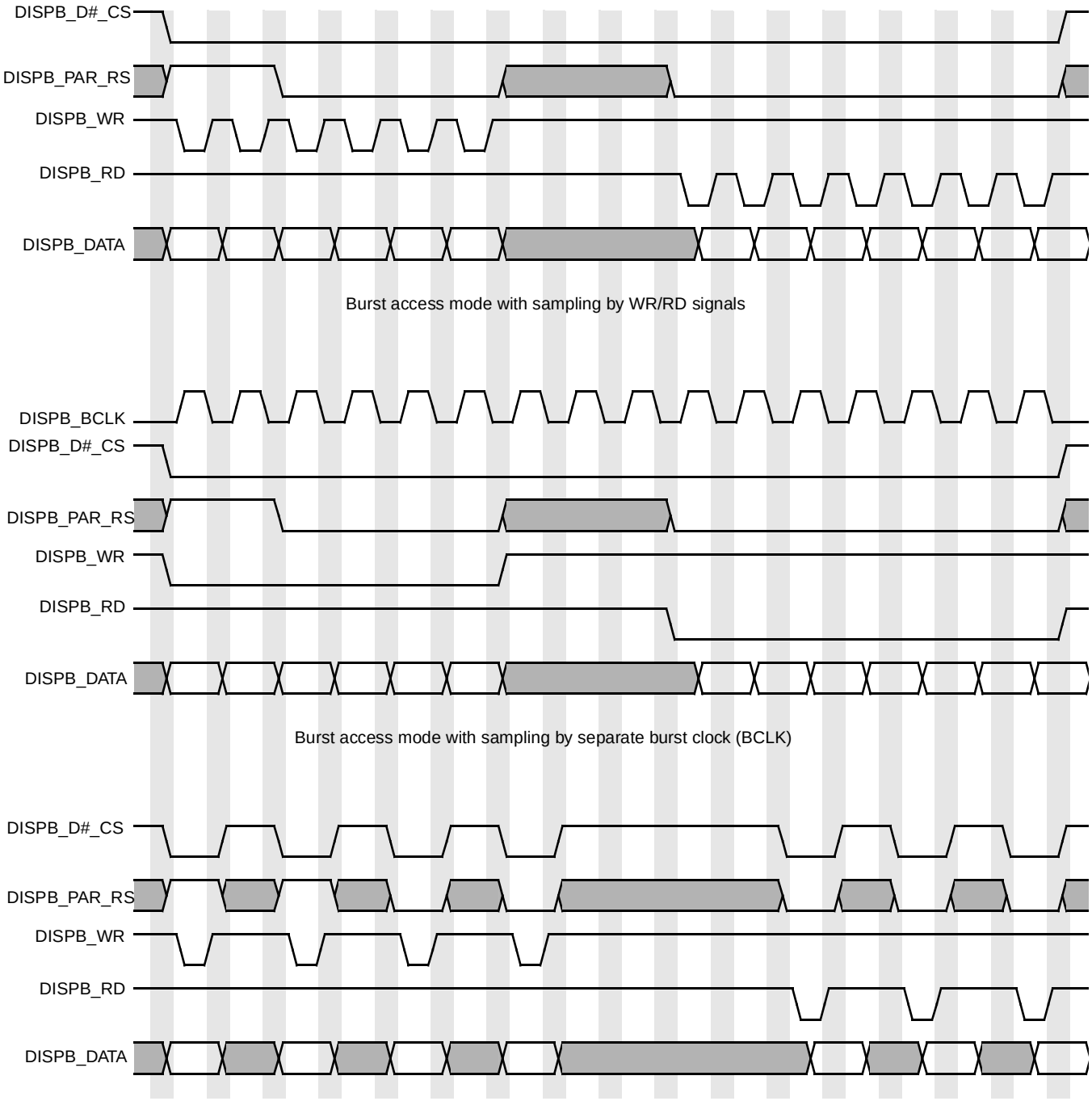

Figure 52. Asynchronous Parallel System 80 Interface (Type 2) Burst Mode Timing Diagram

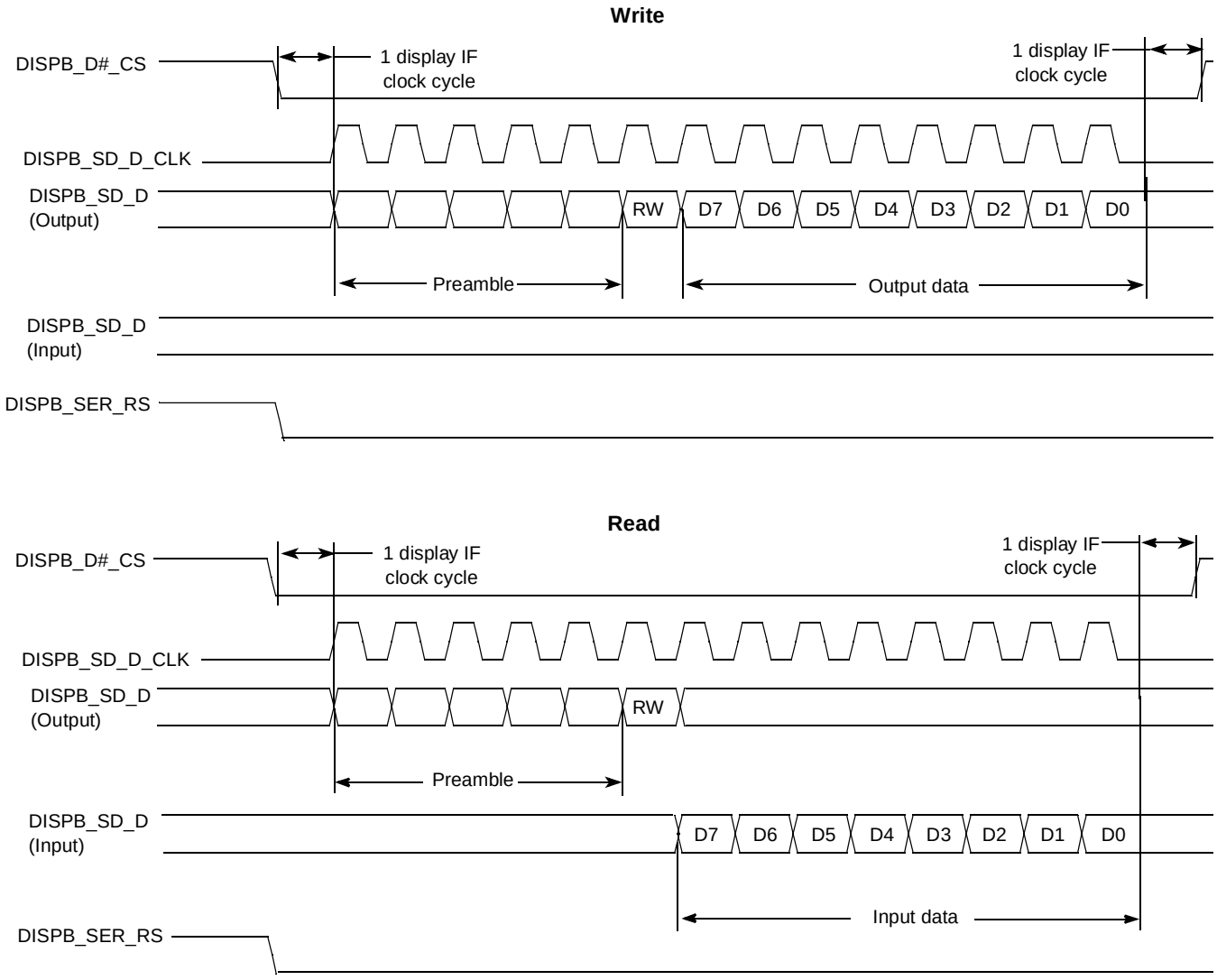

Figure 62. 5-Wire Serial Interface (Type 1) Timing Diagram

Table 52. Parallel Interface Timing Parameters[1]

Signal	Parameter	Symbol	Standards		Unit
			Min	Max	
MSHC_SCLK	Cycle	tSCLKc	25	—	ns
	H pulse length	tSCLKwh	5	—	ns
	L pulse length	tSCLKwl	5	—	ns
	Rise time	tSCLKr	—	10	ns
	Fall time	tSCLKf	—	10	ns
MSHC_BS	Setup time	tBSsu	8	—	ns
	Hold time	tBSh	1	—	ns
MSHC_DATA	Setup time	tDsu	8	—	ns
	Hold time	tDh	1	—	ns
	Output delay time	tDd	—	15	ns

1 Timing is guaranteed for NVCC from 2.7 through 3.1 V and up to a maximum overdrive NVCC of 3.3 V. See NVCC restrictions described in Table 8, "Operating Ranges," on page 13.

4.3.17 Personal Computer Memory Card International Association (PCMCIA)

Figure 68 and Figure 69 depict the timings pertaining to the PCMCIA module, each of which is an example of one clock of strobe set-up time and one clock of strobe hold time. Table 53 lists the timing parameters.

4.3.20.3 Power Down Sequence

Power down sequence for SIM interface is as follows:

1. SIMPD port detects the removal of the SIM Card
2. RST goes Low
3. CLK goes Low
4. TX goes Low
5. VEN goes Low

Each of this steps is done in one CKIL period (usually 32 kHz). Power down can be started because of a SIM Card removal detection or launched by the processor. Figure 75 and Table 57 show the usual timing requirements for this sequence, with Fckil = CKIL frequency value.

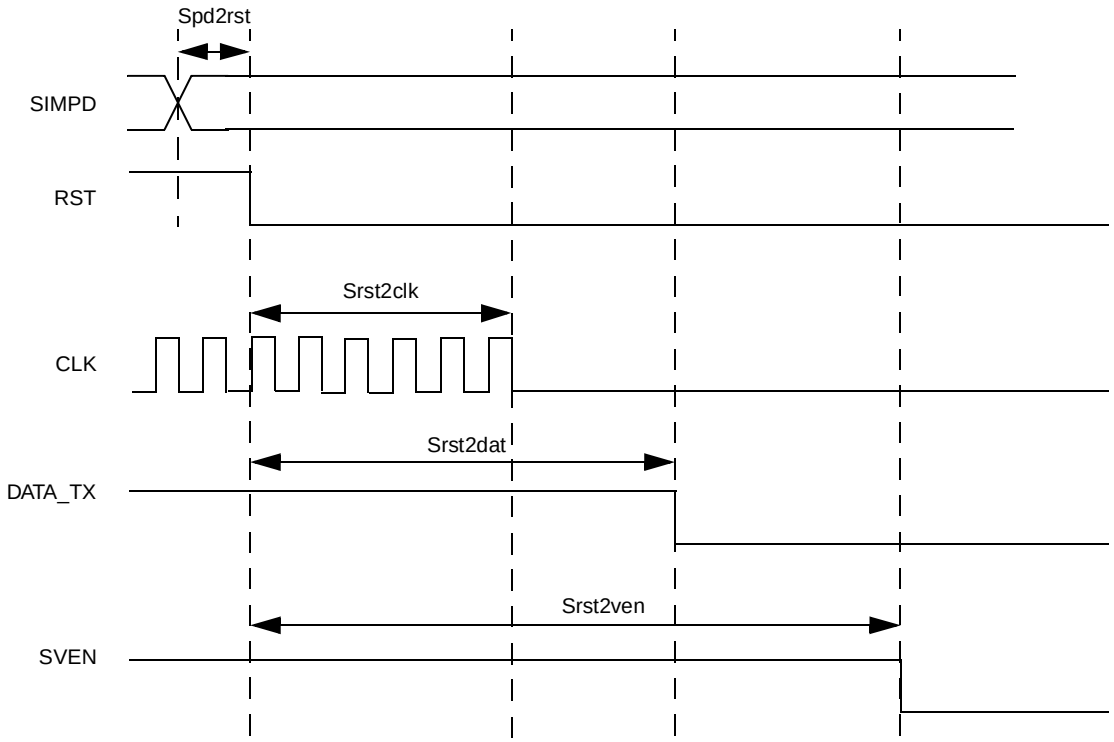

Figure 75. SmartCard Interface Power Down AC Timing

Table 57. Timing Requirements for Power Down Sequence

Num	Description	Symbol	Min	Max	Unit
1	SIM reset to SIM clock stop	$S_{rst2clk}$	0.9*1/FCKIL	0.8	µs
2	SIM reset to SIM TX data low	$S_{rst2dat}$	1.8*1/FCKIL	1.2	µs
3	SIM reset to SIM Voltage Enable Low	$S_{rst2ven}$	2.7*1/FCKIL	1.8	µs
4	SIM Presence Detect to SIM reset Low	S_{pd2rst}	0.9*1/FCKIL	25	ns

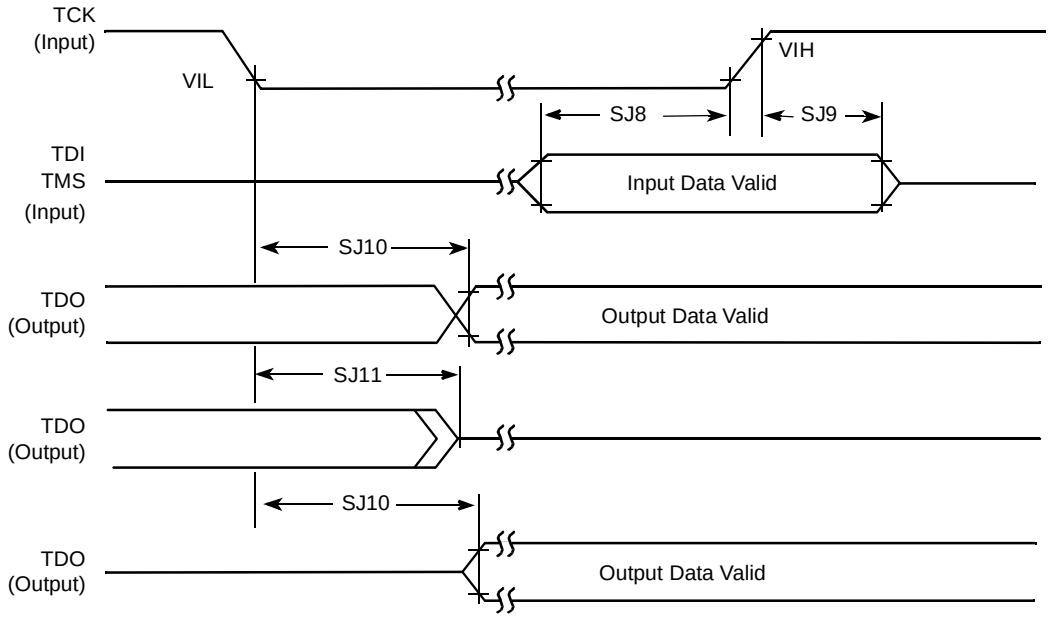

Figure 78. Test Access Port Timing Diagram

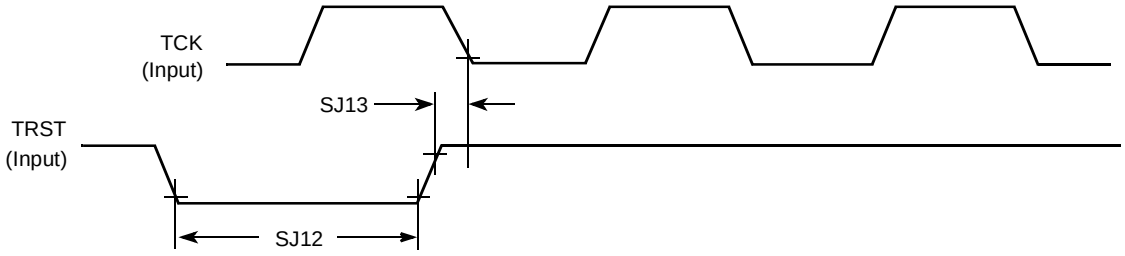

Figure 79. $\overline{\text{TRST}}$ Timing Diagram

Table 58. SJC Timing Parameters

ID	Parameter	All Frequencies		Unit
		Min	Max	
SJ1	TCK cycle time	100[1]	—	ns
SJ2	TCK clock pulse width measured at V_M[2]	40	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	10	—	ns
SJ5	Boundary scan input data hold time	50	—	ns
SJ6	TCK low to output data valid	—	50	ns
SJ7	TCK low to output high impedance	—	50	ns
SJ8	TMS, TDI data set-up time	10	—	ns
SJ9	TMS, TDI data hold time	50	—	ns
SJ10	TCK low to TDO data valid	—	44	ns

Table 61. SSI Transmitter with External Clock Timing Parameters

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	–10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	–10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

5.1.3.2 BGA Signal ID by Ball Grid Location–14 x 14 0.5 mm

Table 65 shows the device connection list for signals only, alpha-sorted by signal identification.

Table 65. 14 x 14 BGA Signal ID by Ball Grid Location

Signal ID	Ball Location
A0	AD6
A1	AF5
A10	AF18
A11	AC3
A12	AD3
A13	AD4
A14	AF17
A15	AF16
A16	AF15
A17	AF14
A18	AF13
A19	AF12
A2	AB5
A20	AF11
A21	AF10
A22	AF9
A23	AF8
A24	AF7
A25	AF6
A3	AE4
A4	AA3
A5	AF4
A6	AB3
A7	AE3
A8	AD5
A9	AF3
ATA_CS0	J6
ATA_CS1	F2
ATA_DIOR	E2
ATA_DIOW	H6
ATA_DMACK	F1
$\overline{\text{ATA\_RESET}}$	H3
BATT_LINE	F7
BCLK	AB26
BOOT_MODE0	F20
BOOT_MODE1	C21
BOOT_MODE2	D24
BOOT_MODE3	C22
BOOT_MODE4	D26
CAPTURE	A22
CAS	AD20
CE_CONTROL	A14
CKIH	F24

Signal ID	Ball Location
CKIL	H21
CLKO	C23
CLKSS	G26
COMPARE	G18
CONTRAST	R24
CS0	AE23
CS1	AF23
CS2	AE21
CS3	AD22
CS4	AF24
CS5	AF22
CSI_D10	M24
CSI_D11	L26
CSI_D12	M21
CSI_D13	M25
CSI_D14	M20
CSI_D15	M26
CSI_D4	L21
CSI_D5	K25
CSI_D6	L24
CSI_D7	K26
CSI_D8	L20
CSI_D9	L25
CSI_HSYNC	K20
CSI_MCLK	K24
CSI_PIXCLK	J26
CSI_VSYNC	J25
CSPI1_MISO	P7
CSPI1_MOSI	P2
CSPI1_SCLK	N2
CSPI1_SPI_RDY	N3
CSPI1_SS0	P3
CSPI1_SS1	P1
CSPI1_SS2	P6
CSPI2_MISO	A4
CSPI2_MOSI	E3
CSPI2_SCLK	C7
CSPI2_SPI_RDY	B6
CSPI2_SS0	B5
CSPI2_SS1	C6
CSPI2_SS2	A5
CSPI3_MISO	G3
CSPI3_MOSI	D2

Table 67. 19 x 19 BGA No Connects[1]

Signal	Ball Location
NC	N7
NC	P7
NC	U21

1 These contacts are not used and must be floated by the user.

5.2.3.2 BGA Signal ID by Ball Grid Location—19 x 19 0.8 mm

Table 68. 19 x 19 BGA Signal ID by Ball Grid Location

Signal ID	Ball Location
A0	Y6
A1	AC5
A10	V15
A11	AB3
A12	AA3
A13	Y3
A14	Y15
A15	Y14
A16	V14
A17	Y13
A18	V13
A19	Y12
A2	AB5
A20	V12
A21	Y11
A22	V11
A23	Y10
A24	Y9
A25	Y8
A3	AA5
A4	Y5
A5	AC4
A6	AB4
A7	AA4
A8	Y4
A9	AC3
ATA_CS0	E1
ATA_CS1	G4
ATA_DIOR	E3
ATA_DIOW	H6
ATA_DMACK	E2
$\overline{\text{ATA\_RESET}}$	F3
BATT_LINE	F6
BCLK	W20

Signal ID	Ball Location
CKIL	E21
CLKO	C20
CLKSS	H17
COMPARE	A20
CONTRAST	N21
CS0	U17
CS1	Y22
CS2	Y18
CS3	Y19
CS4	Y20
CS5	AA21
CSI_D10	K21
CSI_D11	K22
CSI_D12	K23
CSI_D13	L20
CSI_D14	L18
CSI_D15	L21
CSI_D4	J20
CSI_D5	J21
CSI_D6	L17
CSI_D7	J22
CSI_D8	J23
CSI_D9	K20
CSI_HSYNC	H22
CSI_MCLK	H20
CSI_PIXCLK	H23
CSI_VSYNC	H21
CSPI1_MISO	N2
CSPI1_MOSI	N1
CSPI1_SCLK	M4
CSPI1_SPI_RDY	M1
CSPI1_SS0	M2
CSPI1_SS1	N6
CSPI1_SS2	M3