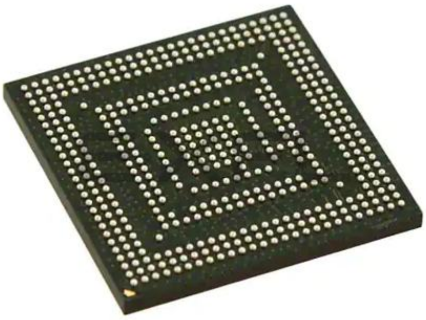

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, MPEG-4, VFP
RAM Controllers	DDR
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, Keypad, LCD
Ethernet	-
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V
Operating Temperature	-20°C ~ 70°C (TA)
Security Features	Random Number Generator, RTIC, Secure Fusebox, Secure JTAG, Secure Memory
Package / Case	457-LFBGA
Supplier Device Package	457-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx31dvkn5dr2

Table 3. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Functional Grouping	Brief Description	Section/ Page
SCC	Security Controller Module	Security	The SCC is a hardware component composed of two blocks—the Secure RAM module, and the Security Monitor. The Secure RAM provides a way of securely storing sensitive information.	—
SDHC	Secured Digital Host Controller	Connectivity Peripheral	The SDHC controls the MMC (MultiMediaCard), SD (Secure Digital) memory, and I/O cards by sending commands to cards and performing data accesses to and from the cards.	4.3.19/87
SDMA	Smart Direct Memory Access	System Control Peripheral	The SDMA controller maximizes the system's performance by relieving the ARM core of the task of bulk data transfer from memory to memory or between memory and on-chip peripherals.	—
SIM	Subscriber Identification Module	Connectivity Peripheral	The SIM interfaces to an external Subscriber Identification Card. It is an asynchronous serial interface adapted for Smart Card communication for e-commerce applications.	4.3.20/88
SJC	Secure JTAG Controller	Debug	The SJC provides debug and test control with maximum security and provides a flexible architecture for future derivatives or future multi-cores architecture.	4.3.21/92
SSI	Synchronous Serial Interface	Multimedia Peripheral	The SSI is a full-duplex, serial port that allows the device to communicate with a variety of serial devices, such as standard codecs, Digital Signal Processors (DSPs), microprocessors, peripherals, and popular industry audio codecs that implement the inter-IC sound bus standard (I2S) and Intel AC97 standard.	4.3.22/94
UART	Universal Asynchronous Receiver/Trans mitter	Connectivity Peripheral	The UART provides serial communication capability with external devices through an RS-232 cable or through use of external circuitry that converts infrared signals to electrical signals (for reception) or transforms electrical signals to signals that drive an infrared LED (for transmission) to provide low speed IrDA compatibility.	—
USB	Universal Serial Bus— 2 Host Controllers and 1 OTG (On-The-Go)	Connectivity Peripherals	• USB Host 1 is designed to support transceiverless connection to the on-board peripherals in Low Speed and Full Speed mode, and connection to the ULPI (UTMI+ Low-Pin Count) and Legacy Full Speed transceivers. • USB Host 2 is designed to support transceiverless connection to the Cellular Modem Baseband Processor. • The USB-OTG controller offers HS/FS/LS capabilities in Host mode and HS/FS in device mode. In Host mode, the controller supports direct connection of a FS/LS device (without external hub). In device (bypass) mode, the OTG port functions as gateway between the Host 1 Port and the OTG transceiver.	4.3.23/102
WDOG	Watchdog Timer Module	Timer Peripheral	The WDOG module protects against system failures by providing a method for the system to recover from unexpected events or programming errors.	—

NOTES

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.2 Supply Power-Up/Power-Down Requirements and Restrictions

Any MCIMX31 board design must comply with the power-up and power-down sequence guidelines as described in this section to guarantee reliable operation of the device. Any deviation from these sequences may result in any or all of the following situations:

- Cause excessive current during power up phase
- Prevent the device from booting
- Cause irreversible damage to the MCIMX31 (worst-case scenario)

4.2.1 Powering Up

The Power On Reset ($\overline{\text{POR}}$) pin must be kept asserted (low) throughout the power up sequence. Power up logic must guarantee that all power sources reach their target values prior to the release (de-assertion) of $\overline{\text{POR}}$. Figure 2 and Figure 3 show the power-up sequence for silicon Revision 2.0.1.

NOTE

Stages need to be performed in the order shown; however, *within* each stage, supplies can be powered up in any order. For example, supplies IOQVDD, NVCC1, and NVCC3 through NVCC10 do not need to be powered up in the order shown.

CAUTION

NVCC6 and NVCC9 must be at the same voltage potential. These supplies are connected together on-chip to optimize ESD damage immunity.

4.3.5.1 Timing Parameters

In the timing equations, some timing parameters are used. These parameters depend on the implementation of the ATA interface on silicon, the bus buffer used, the cable delay and cable skew. Table 23 shows ATA timing parameters.

Table 23. ATA Timing Parameters

Name	Description	Value/ Contributing Factor[1]
T	Bus clock period (ipg_clk_ata)	peripheral clock frequency
ti_ds	Set-up time ata_data to ata_iordy edge (UDMA-in only) UDMA0 UDMA1 UDMA2, UDMA3 UDMA4 UDMA5	 15 ns 10 ns 7 ns 5 ns 4 ns
ti_dh	Hold time ata_iordy edge to ata_data (UDMA-in only) UDMA0, UDMA1, UDMA2, UDMA3, UDMA4 UDMA5	 5.0 ns 4.6 ns
tco	Propagation delay bus clock L-to-H to ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data, ata_buffer_en	12.0 ns
tsu	Set-up time ata_data to bus clock L-to-H	8.5 ns
tsui	Set-up time ata_iordy to bus clock H-to-L	8.5 ns
thi	Hold time ata_iordy to bus clock H to L	2.5 ns
tskew1	Max difference in propagation delay bus clock L-to-H to any of following signals ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en	7 ns
tskew2	Max difference in buffer propagation delay for any of following signals ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en	transceiver
tskew3	Max difference in buffer propagation delay for any of following signals ata_iordy, ata_data (read)	transceiver
tbuf	Max buffer propagation delay	transceiver
tcable1	Cable propagation delay for ata_data	cable
tcable2	Cable propagation delay for control signals ata_dior, ata_diow, ata_iordy, ata_dmack	cable
tskew4	Max difference in cable propagation delay between ata_iordy and ata_data (read)	cable
tskew5	Max difference in cable propagation delay between (ata_dior, ata_diow, ata_dmack) and ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_data(write)	cable
tskew6	Max difference in cable propagation delay without accounting for ground bounce	cable

1 Values provided where applicable.

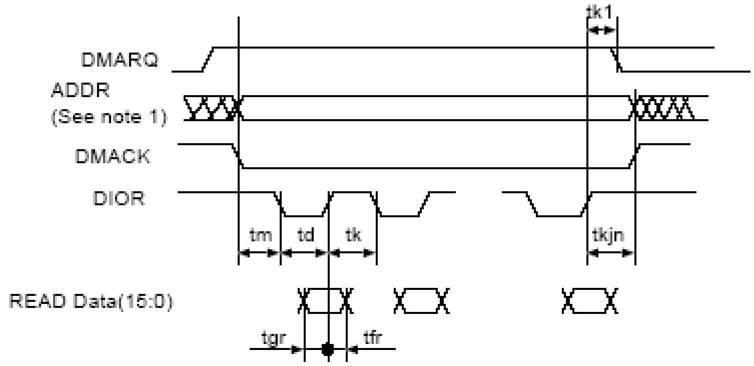

Figure 12. MDMA Read Timing Diagram

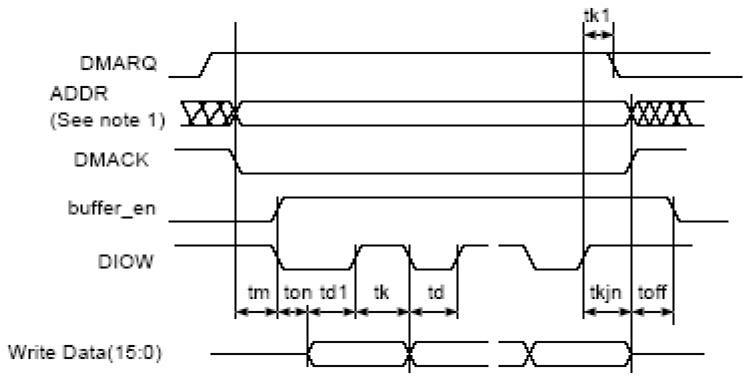

Figure 13. MDMA Write Timing Diagram

Table 26. MDMA Read and Write Timing Parameters

ATA Parameter	Parameter from Figure 12, Figure 13	Value	Controlling Variable
tm, ti	tm	tm (min) = ti (min) = time_m * T – (tskew1 + tskew2 + tskew5)	time_m
td	td, td1	td1.(min) = td (min) = time_d * T – (tskew1 + tskew2 + tskew6)	time_d
tk	tk	tk.(min) = time_k * T – (tskew1 + tskew2 + tskew6)	time_k
t0	—	t0 (min) = (time_d + time_k) * T	time_d, time_k
tg(read)	tgr	tgr (min-read) = tco + tsu + tbuf + tbuf + tcable1 + tcable2 tgr.(min-drive) = td – te(drive)	time_d
tf(read)	tfr	tfr (min-drive) = 0	—
tg(write)	—	tg (min-write) = time_d * T – (tskew1 + tskew2 + tskew5)	time_d
tf(write)	—	tf (min-write) = time_k * T – (tskew1 + tskew2 + tskew6)	time_k
tL	—	tL (max) = (time_d + time_k–2)*T – (tsu + tco + 2*tbuf + 2*tcable2)	time_d, time_k
tn, tj	tkjn	tn= tj= tkjn = (max(time_k,. time_jn) * T – (tskew1 + tskew2 + tskew6)	time_jn
—	ton toff	ton = time_on * T – tskew1 toff = time_off * T – tskew1	—

Table 29. CSPI Interface Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
CS1	SCLK Cycle Time	t_{clk}	60	—	ns
CS2	SCLK High or Low Time	t_{SW}	30	—	ns
CS3	SCLK Rise or Fall	$t_{RISE/FALL}$	—	7.6	ns
CS4	SSx pulse width	t_{CSLH}	25	—	ns
CS5	SSx Lead Time (CS setup time)	t_{SCS}	25	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	25	—	ns
CS7	Data Out Setup Time	t_{Smosi}	5	—	ns
CS8	Data Out Hold Time	t_{Hmosi}	5	—	ns
CS9	Data In Setup Time	t_{Smiso}	6	—	ns
CS10	Data In Hold Time	t_{Hmiso}	5	—	ns
CS11	$\overline{\text{SPI\_RDY}}$ Setup Time[1]	t_{SRDY}	—	—	ns

[1] SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.3.8 DPLL Electrical Specifications

The three PLL's of the MCIMX31 (MCU, USB, and Serial PLL) are all based on same DPLL design. The characteristics provided herein apply to all of them, except where noted explicitly. The PLL characteristics are provided based on measurements done for both sources—external clock source (CKIH), and FPM (Frequency Pre-Multiplier) source.

4.3.8.1 Electrical Specifications

Table 30 lists the DPLL specification.

Table 30. DPLL Specifications

Parameter	Min	Typ	Max	Unit	Comments
CKIH frequency	15	26[1]	75[2]	MHz	—
CKIL frequency (Frequency Pre-multiplier (FPM) enable mode)	—	32; 32.768, 38.4	—	kHz	FPM lock time ≈ 480 µs.
Predivision factor (PD bits)	1	—	16	—	—
PLL reference frequency range after Predivider	15	—	35	MHz	15 ≤ CKIH frequency/PD ≤ 35 MHz 15 ≤ FPM output/PD ≤ 35 MHz
PLL output frequency range: MPLL and SPLL UPLL	 52 190	—	 532 240	MHz	—
Maximum allowed reference clock phase noise.	—	—	± 100	ps	—
Frequency lock time (FOL mode or non-integer MF)	—	—	398	—	Cycles of divided reference clock.

Table 30. DPLL Specifications (continued)

Parameter	Min	Typ	Max	Unit	Comments
Phase lock time	—	—	100	µs	In addition to the frequency
Maximum allowed PLL supply voltage ripple	—	—	25	mV	$F_{modulation}$ < 50 kHz
Maximum allowed PLL supply voltage ripple	—	—	20	mV	50 kHz < $F_{modulation}$ < 300 kHz
Maximum allowed PLL supply voltage ripple	—	—	25	mV	$F_{modulation}$ > 300 kHz
PLL output clock phase jitter	—	—	5.2	ns	Measured on CLKO pin
PLL output clock period jitter	—	—	420	ps	Measured on CLKO pin

[1] The user or board designer must take into account that the use of a frequency other than 26 MHz would require adjustment to the DPTC–DVFS table, which is incorporated into operating system code.

[2] The PLL reference frequency must be ≤ 35 MHz. Therefore, for frequencies between 35 MHz and 70 MHz, program the predivider to divide by 2 or more. If the CKIH frequency is above 70 MHz, program the predivider to 3 or more. For PD bit description, see the reference manual.

4.3.9 EMI Electrical Specifications

This section provides electrical parametrics and timings for EMI module.

4.3.9.1 NAND Flash Controller Interface (NFC)

The NFC supports normal timing mode, using two flash clock cycles for one access of $\overline{\text{RE}}$ and $\overline{\text{WE}}$. AC timings are provided as multiplications of the clock cycle and fixed delay. Figure 22, Figure 23, Figure 24, and Figure 25 depict the relative timing requirements among different signals of the NFC at module level, for normal mode, and Table 31 lists the timing parameters.

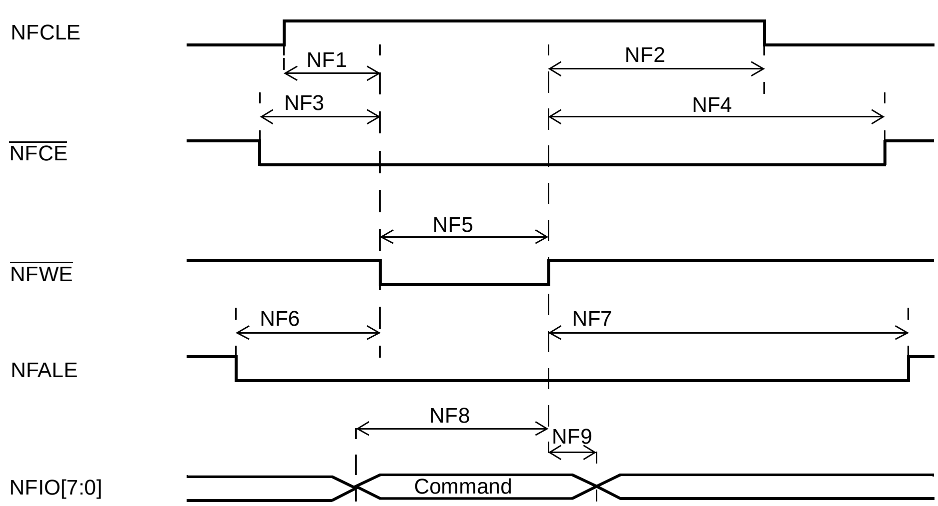

Figure 22. Command Latch Cycle Timing DIagram

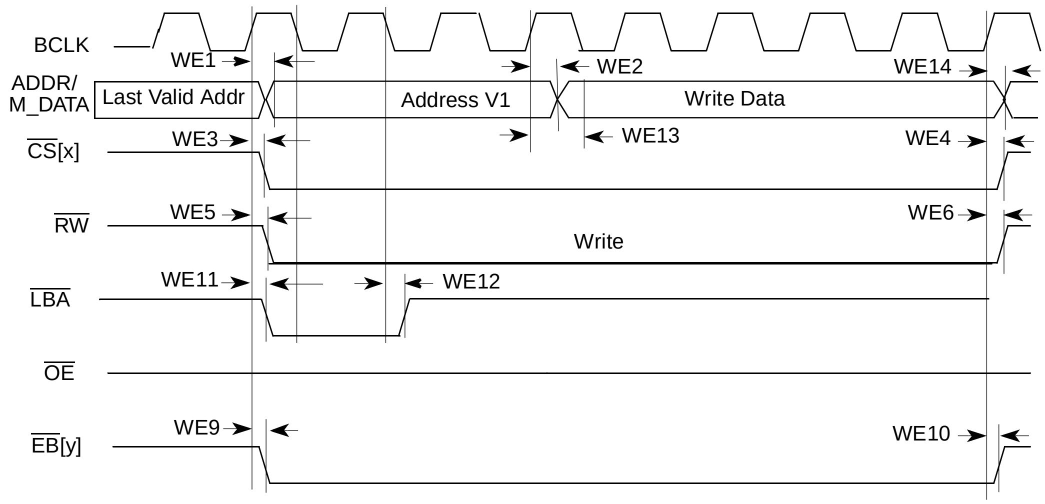

Figure 31. Muxed A/D Mode Timing Diagram for Asynchronous Write Access—WSC=7, LBA=1, LBN=1, LAH=1

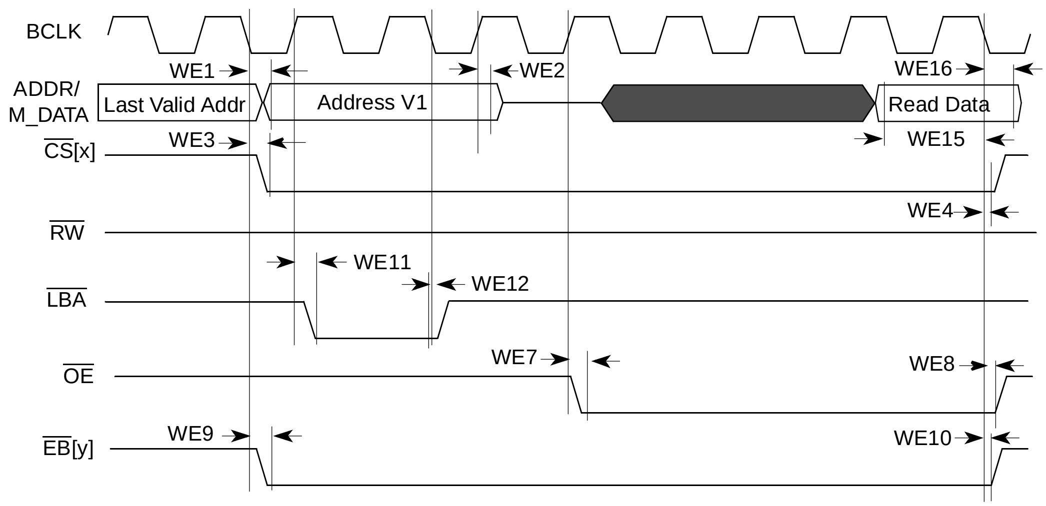

Figure 32. Muxed A/D Mode Timing Diagram for Asynchronous Read Access—WSC=7, LBA=1, LBN=1, LAH=1, OEA=7

4.3.9.3 ESDCTL Electrical Specifications

Figure 33, Figure 34, Figure 35, Figure 36, Figure 37, and Figure 38 depict the timings pertaining to the ESDCTL module, which interfaces Mobile DDR or SDR SDRAM. Table 33, Table 34, Table 35, Table 36, Table 37, and Table 38 list the timing parameters.

Table 33. DDR/SDR SDRAM Read Cycle Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
SD9	Data out hold time[1]	tOH	1.8	—	ns
SD10	Active to read/write command period	tRC	10	—	clock

[1] Timing parameters are relevant only to SDR SDRAM. For the specific DDR SDRAM data related timing parameters, see Table 37 and Table 38.

NOTE

SDR SDRAM CLK parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value. SD1 + SD2 does not exceed 7.5 ns for 133 MHz.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 33 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

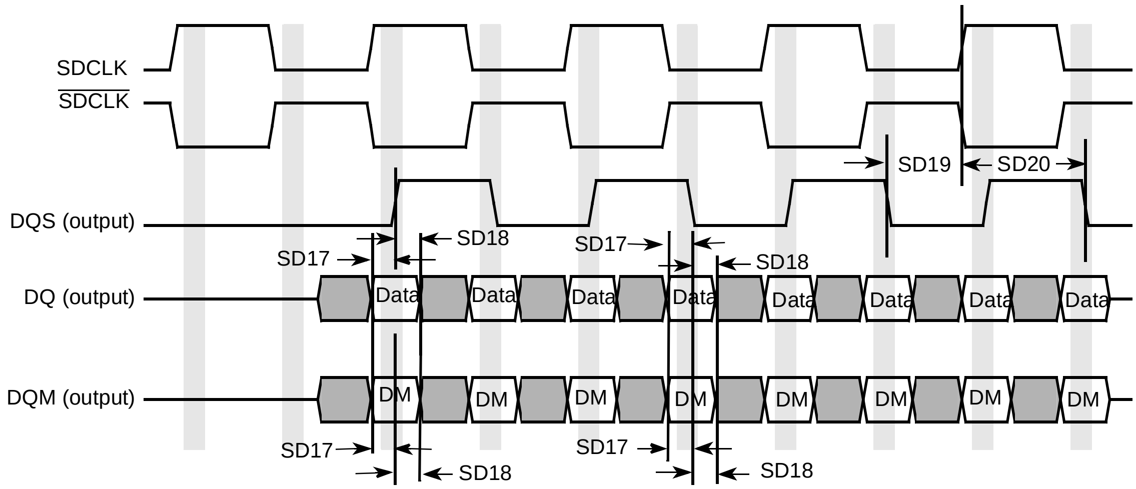

Figure 37. Mobile DDR SDRAM Write Cycle Timing Diagram

Table 37. Mobile DDR SDRAM Write Cycle Timing Parameters[1]

ID	Parameter	Symbol	Min	Max	Unit
SD17	DQ and DQM setup time to DQS	tDS	0.95	—	ns
SD18	DQ and DQM hold time to DQS	tDH	0.95	—	ns
SD19	Write cycle DQS falling edge to SDCLK output delay time.	tDSS	1.8	—	ns
SD20	Write cycle DQS falling edge to SDCLK output hold time.	tDSH	1.8	—	ns

[1] Test condition: Measured using delay line 5 programmed as follows: ESDCDLY5[15:0] = 0x0703.

NOTE

SDRAM CLK and DQS related parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 37 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

The timing described in Figure 43 is that of a Motorola sensor. Some other sensors may have a slightly different timing. The CSI can be programmed to support rising/falling-edge triggered SENSB_VSYNC; active-high/low SENSB_HSYNC; and rising/falling-edge triggered SENSB_PIX_CLK.

4.3.14.3 Electrical Characteristics

Figure 44 depicts the sensor interface timing, and Table 44 lists the timing parameters.

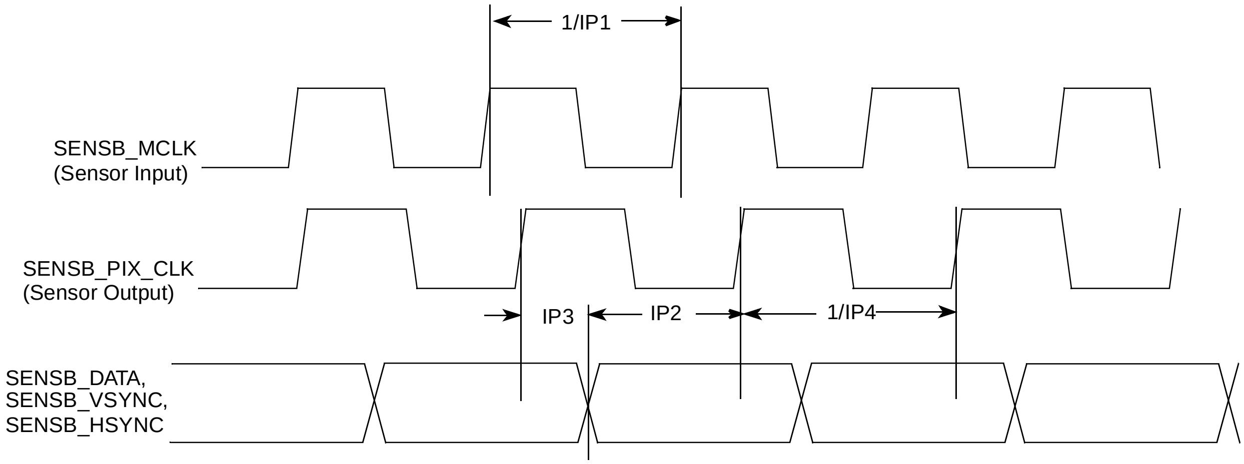

Figure 44. Sensor Interface Timing Diagram

Table 44. Sensor Interface Timing Parameters[1]

ID	Parameter	Symbol	Min.	Max.	Units
IP1	Sensor input clock frequency	Fmck	0.01	133	MHz
IP2	Data and control setup time	Tsu	5	—	ns
IP3	Data and control holdup time	Thd	3	—	ns
IP4	Sensor output (pixel) clock frequency	Fpck	0.01	133	MHz

[1] The timing specifications for Figure 44 are referenced to the rising edge of SENS_PIX_CLK when the SENS_PIX_CLK_POL bit in the CSI_SENS_CONF register is cleared. When the SENS_PIX_CLK_POL is set, the clock is inverted and all timing specifications will remain the same but are referenced to the falling edge of the clock.

4.3.15 IPU—Display Interfaces

4.3.15.1 Supported Display Components

Table 45 lists the known supported display components at the time of publication.

Table 45. Supported Display Components[1]

Type	Vendor	Model
TFT displays (memory-less)	Sharp (HR-TFT Super Mobile LCD family)	LQ035Q7 DB02, LM019LC1Sxx
	Samsung (QCIF and QVGA TFT modules for mobile phones)	LTS180S1-HF1, LTS180S3-HF1, LTS350Q1-PE1, LTS350Q1-PD1, LTS220Q1-HE1[2]
	Toshiba (LTM series)	LTM022P806[2], LTM04C380K[2], LTM018A02A[2], LTM020P332[2], LTM021P337[2], LTM019P334[2], LTM022A783[2], LTM022A05ZZ[2]
	NEC	NL6448BC20-08E, NL8060BC31-27
Display controllers	Epson	S1D15xxx series, S1D19xxx series, S1D13713, S1D13715
	Solomon Systech	SSD1301 (OLED), SSD1828 (LDCD)
	Hitachi	HD66766, HD66772
	ATI	W2300
Smart display modules	Epson	L1F10043 T[2], L1F10044 T[2], L1F10045 T[2], L2D22002[2], L2D20014[2], L2F50032[2], L2D25001 T[2]
	Hitachi	120 160 65K/4096 C-STN (#3284 LTD-1398-2) based on HD 66766 controller
	Densitron Europe LTD	All displays with MPU 80/68K series interface and serial peripheral interface
	Sharp	LM019LC1Sxx
	Sony	ACX506AKM
Digital video encoders (for TV)	Analog Devices	ADV7174/7179
	Crystal (Cirrus Logic)	CS49xx series
	Focus	FS453/4

[1] Freescale Semiconductor does not recommend one supplier over another and in no way suggests that these are the only display component suppliers.

[2] These display components not validated at time of publication.

4.3.15.2 Synchronous Interfaces

4.3.15.2.1 Interface to Active Matrix TFT LCD Panels, Functional Description

Figure 45 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DISPB_D3_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, DISPB_D3_CLK runs continuously.
- DISPB_D3_HSYNC causes the panel to start a new line.
- DISPB_D3_VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.

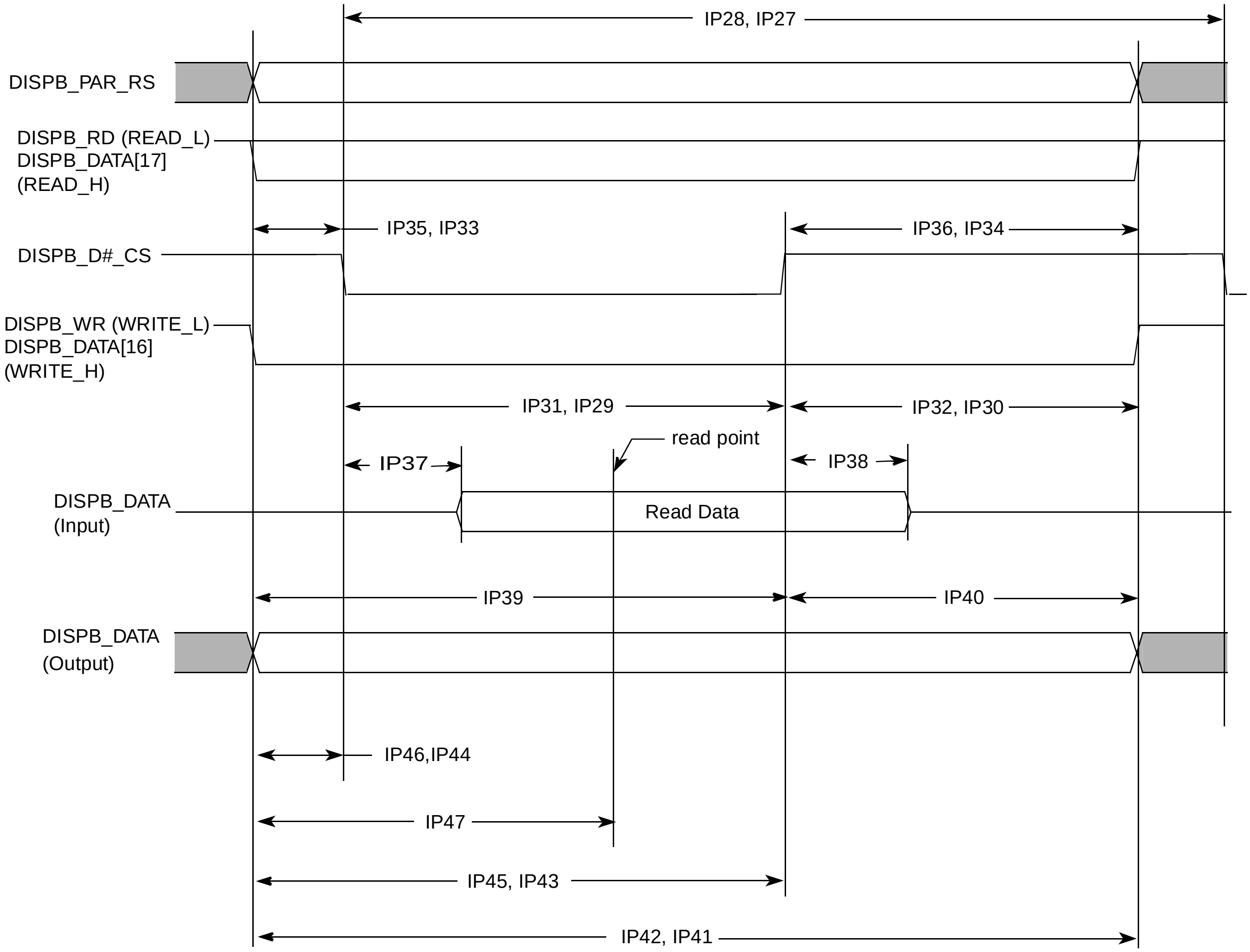

Figure 56. Asynchronous Parallel System 80 Interface (Type 1) Timing Diagram

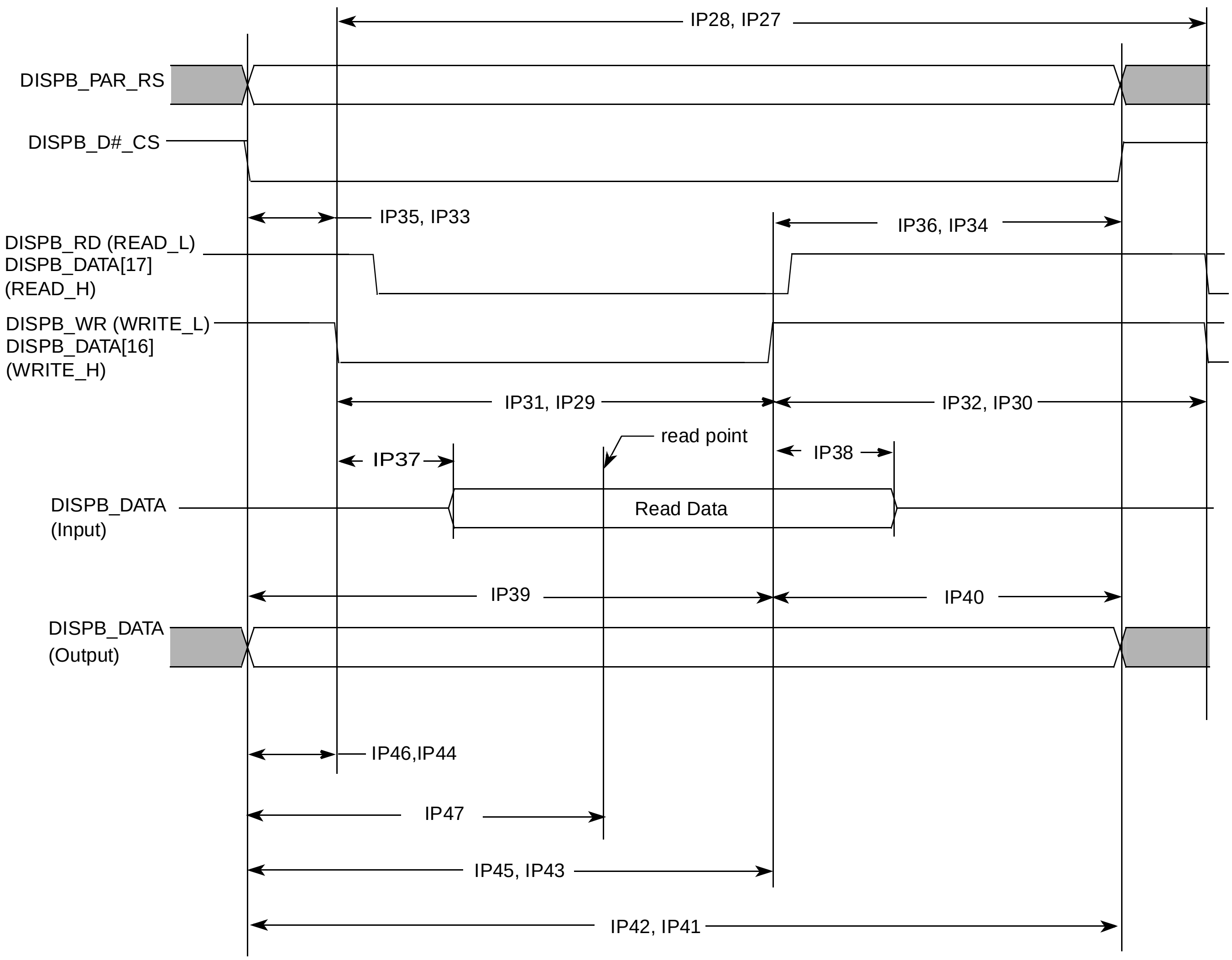

Figure 57. Asynchronous Parallel System 80 Interface (Type 2) Timing Diagram

Table 61. SSI Transmitter with External Clock Timing Parameters

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	–10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	–10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

Table 65. 14 x 14 BGA Signal ID by Ball Grid Location (continued)

Signal ID	Ball Location
LD8	U21
LD9	W26
M_GRANT	Y21
M_REQUEST	AC25
MA10	AC1
MCUPG	See VPG0
NFALE	V1
NFCE	T6
NFCLE	U3
NFRB	U1
NFRE	V2
NFWE	T7
NFWP	U2
OE	AB25
PAR_RS	R21
PC_BVD1	H2
PC_BVD2	K6
PC_CD1	L7
PC_CD2	K1
PC_POE	J7
PC_PWRON	K3
PC_READY	J2
PC_RST	H1
PC_RW	G2
PC_VS1	J1
PC_VS2	K7
PC_WAIT	L6
POR	H24
POWER_FAIL	E26
PWMO	G1
RAS	AF19
READ	P20
RESET_IN	J21
RI_DCE1	F11
RI_DTE1	G12
RTCK	C17
RTS1	G11
RTS2	B14
RW	AB22
RXD1	A10
RXD2	A13
SCK3	R2
SCK4	C4
SCK5	D3
SDCKE0	AD21
SDCKE1	AF21

Signal ID	Ball Location
SCLK0	B22
SD_D_CLK	P24
SD_D_I	N20
SD_D_IO	P25
SD0	AD18
SD1	AE17
SD1_CLK	M7
SD1_CMD	L2
SD1_DATA0	M6
SD1_DATA1	L1
SD1_DATA2	L3
SD1_DATA3	K2
SD10	AE15
SD11	AE14
SD12	AD14
SD13	AA14
SD14	AE13
SD15	AD13
SD16	AA13
SD17	AD12
SD18	AA12
SD19	AE11
SD2	AA19
SD20	AE10
SD21	AA11
SD22	AE9
SD23	AA10
SD24	AE8
SD25	AD10
SD26	AE7
SD27	AA9
SD28	AA8
SD29	AD9
SD3	AA18
SD30	AE6
SD31	AA7
SD4	AD17
SD5	AA17
SD6	AE16
SD7	AA16
SD8	AD15
SD9	AA15
SDBA0	AD7
SDBA1	AE5
TRSTB	B20
TTM_PAD	U20

Table 67. 19 x 19 BGA No Connects[1]

Signal	Ball Location
NC	N7
NC	P7
NC	U21

[1] These contacts are not used and must be floated by the user.

5.2.3.2 BGA Signal ID by Ball Grid Location—19 x 19 0.8 mm

Table 68. 19 x 19 BGA Signal ID by Ball Grid Location

Signal ID	Ball Location	Signal ID	Ball Location
A0	Y6	CKIL	E21
A1	AC5	CLKO	C20
A10	V15	CLKSS	H17
A11	AB3	COMPARE	A20
A12	AA3	CONTRAST	N21
A13	Y3	CS0	U17
A14	Y15	CS1	Y22
A15	Y14	CS2	Y18
A16	V14	CS3	Y19
A17	Y13	CS4	Y20
A18	V13	CS5	AA21
A19	Y12	CSI_D10	K21
A2	AB5	CSI_D11	K22
A20	V12	CSI_D12	K23
A21	Y11	CSI_D13	L20
A22	V11	CSI_D14	L18
A23	Y10	CSI_D15	L21
A24	Y9	CSI_D4	J20
A25	Y8	CSI_D5	J21
A3	AA5	CSI_D6	L17
A4	Y5	CSI_D7	J22
A5	AC4	CSI_D8	J23
A6	AB4	CSI_D9	K20
A7	AA4	CSI_HSYNC	H22
A8	Y4	CSI_MCLK	H20
A9	AC3	CSI_PIXCLK	H23
ATA_CS0	E1	CSI_VSYNC	H21
ATA_CS1	G4	CSPI1_MISO	N2
ATA_DIOR	E3	CSPI1_MOSI	N1
ATA_DIOW	H6	CSPI1_SCLK	M4
ATA_DMACK	E2	CSPI1_SPI_RDY	M1
$\overline{\mathrm{ATA\_RESET}}$	F3	CSPI1_SS0	M2
BATT_LINE	F6	CSPI1_SS1	N6
BCLK	W20	CSPI1_SS2	M3

Table 68. 19 x 19 BGA Signal ID by Ball Grid Location (continued)

Signal ID	Ball Location
BOOT_MODE0	F17
BOOT_MODE1	C21
BOOT_MODE2	D20
BOOT_MODE3	F18
BOOT_MODE4	E20
CAPTURE	D18
CAS	AA20
CE_CONTROL	D12
CKIH	F23
CSPI3_SCLK	H7
CSPI3_SPI_RDY	F4
CTS1	A9
CTS2	C12
D0	U6
D1	W4
D10	V1
D11	U4
D12	U3
D13	R6
D14	U2
D15	U1
D2	W3
D3	V4
D3_CLS	P20
D3_REV	P21
D3_SPL	N17
D4	T7
D5	W2
D6	V3
D7	W1
D8	T6
D9	V2
DCD_DCE1	C10
DCD_DTE1	D11
$\overline{\text{DE}}$	D16
DQM0	AB19
DQM1	Y16
DQM2	AA18
DQM3	AB18
DRDY0	M17
DSR_DCE1	B10
DSR_DTE1	A11
DTR_DCE1	F10
DTR_DCE2	C11
DTR_DTE1	A10
DVFS0	E22

Signal ID	Ball Location
CSPI2_MISO	B4
CSPI2_MOSI	D5
CSPI2_SCLK	B5
CSPI2_SPI_RDY	D6
CSPI2_SS0	C5
CSPI2_SS1	A4
CSPI2_SS2	F7
CSPI3_MISO	D2
CSPI3_MOSI	E4
GPIO1_3	G20
GPIO1_4	D21
GPIO1_5 (PWR RDY)	D19
GPIO1_6	G18
GPIO3_0	G23
GPIO3_1	K17
HSYNC	L23
I2C_CLK	J18
I2C_DAT	K18
IOIS16	J7
KEY_COL0	A15
KEY_COL1	B15
KEY_COL2	D14
KEY_COL3	C15
KEY_COL4	F13
KEY_COL5	A16
KEY_COL6	B16
KEY_COL7	A17
KEY_ROW0	A13
KEY_ROW1	B13
KEY_ROW2	C13
KEY_ROW3	A14
KEY_ROW4	F12
KEY_ROW5	D13
KEY_ROW6	B14
KEY_ROW7	C14
L2PG	See VPG1
LBA	V17
LCS0	M22
LCS1	N23
LD0	R23
LD1	R22
LD10	U22
LD11	R18
LD12	U20
LD13	V23
LD14	V22

6 Product Documentation

This Data Sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com.

MCIMX31 Product Brief (order number MCIMX31PB)

MCIMX31 Reference Manual (order number MCIMX31RM)

MCIMX31 Chip Errata (order number MCIMX31CE)

The Freescale manuals are available on the Freescale Semiconductors Web site at http://www.freescale.com/imx. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered. ARM Ltd. documentation is available from http://www.arm.com.

7 Revision History

Table 71 summarizes revisions to this document since the release of Rev. 4.1.

Table 71. Revision History

Rev.	Location	Revision
4.3	Table 1, "Ordering Information," on page 3	Added a footnote and new part numbers for silicon revision 2.0.1.
4.2	Global	Replaced all references to silicon 2.0 with silicon revision 2.0.1.
4.2	Table 1, "Ordering Information," on page 3	Added new part numbers for revision 2.0.1.
4.2	Section 1.2.1, “Feature Differences Between Mask Sets	Updated for revision 2.0.1.
4.2	Table 8, "Operating Ranges," on page 13	Updated Core Operating voltage ranges and respective footnotes.
4.2	Table 12, "Current Consumption for –40×C to 85×C, for Silicon Revision 2.0.1," on page 16	Updated for silicon revision 2.0.1.
4.2	Table 13, "Current Consumption for –20×C to 70×C, for Silicon Revision 2.0.1," on page 17	Updated values for silicon revision 2.0.1.
4.2	Section 3, “Signal Descriptions	Removed reference to the TTM_PAD as it is no longer connected.

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