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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, MPEG-4, VFP
RAM Controllers	DDR
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, Keypad, LCD
Ethernet	-
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V
Operating Temperature	-20°C ~ 70°C (TA)
Security Features	Random Number Generator, RTIC, Secure Fusebox, Secure JTAG, Secure Memory
Package / Case	473-LFBGA
Supplier Device Package	473-LFBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx31dvmn5dr2

1.3 Block Diagram

Figure 1 shows the MCIMX31 simplified interface block diagram.

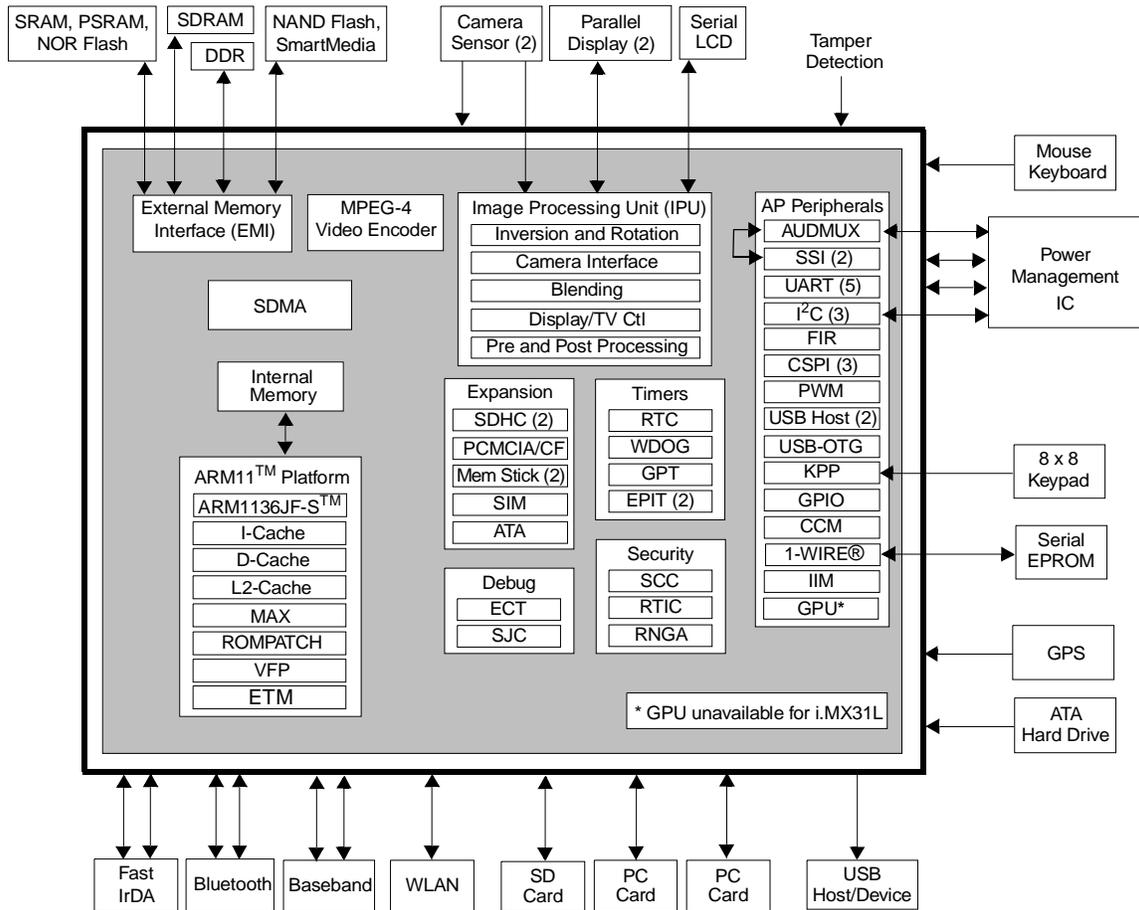


Figure 1. MCIMX31 Simplified Interface Block Diagram

2 Functional Description and Application Information

2.1 ARM11 Microprocessor Core

The CPU of the MCIMX31 is the ARM1136JF-S core based on the ARM v6 architecture. It supports the ARM Thumb® instruction sets, features Jazelle® technology (which enables direct execution of Java byte codes), and a range of SIMD DSP instructions that operate on 16-bit or 8-bit data values in 32-bit registers.

The ARM1136JF-S processor core features:

- Integer unit with integral EmbeddedICE™ logic
- Eight-stage pipeline
- Branch prediction with return stack
- Low-interrupt latency

Table 3. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Functional Grouping	Brief Description	Section/ Page
Fusebox	Fusebox	ROM	The Fusebox is a ROM that is factory configured by Freescale.	4.3.12/53 See also Table 11
GPIO	General Purpose I/O Module	Pins	The GPIO provides several groups of 32-bit bidirectional, general purpose I/O. This peripheral provides dedicated general-purpose signals that can be configured as either inputs or outputs.	—
GPT	General Purpose Timer	Timer Peripheral	The GPT is a multipurpose module used to measure intervals or generate periodic output.	—
GPU	Graphics Processing Unit	Multimedia Peripheral	The GPU provides hardware acceleration for 2D and 3D graphics algorithms.	—
I ² C	Inter IC Communication	Connectivity Peripheral	The I ² C provides serial interface for controlling the Sensor Interface and other external devices. Data rates of up to 100 Kbits/s are supported.	4.3.13/54
IIM	IC Identification Module	ID	The IIM provides an interface for reading device identification.	—
IPU	Image Processing Unit	Multimedia Peripheral	The IPU processes video and graphics functions in the MCIMX31 and interfaces to video, still image sensors, and displays.	4.3.14/55 , 4.3.15/57
KPP	Keypad Port	Connectivity Peripheral	The KPP is used for keypad matrix scanning or as a general purpose I/O. This peripheral simplifies the software task of scanning a keypad matrix.	—
MPEG-4	MPEG-4 Video Encoder	Multimedia Peripherals	The MPEG-4 encoder accelerates video compression, following the MPEG-4 standard	—
MSHC	Memory Stick Host Controller	Connectivity Peripheral	The MSHC is placed in between the AIPS and the customer memory stick to support data transfer from the MCIMX31 to the customer memory stick.	4.3.16/82
PADIO	Pads I/O	Buffers and Drivers	The PADIO serves as the interface between the internal modules and the device's external connections.	4.3.1/20
PCMCIA	PCM	Connectivity Peripheral	The PCMCIA Host Adapter provides the control logic for PCMCIA socket interfaces.	4.3.17/84
PWM	Pulse-Width Modulator	Timer Peripheral	The PWM has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones.	4.3.18/86
RNGA	Random Number Generator Accelerator	Security	The RNGA module is a digital integrated circuit capable of generating 32-bit random numbers. It is designed to comply with FIPS-140 standards for randomness and non-determinism.	—
RTC	Real Time Clock	Timer Peripheral	The RTC module provides a current stamp of seconds, minutes, hours, and days. Alarm and timer functions are also available for programming. The RTC supports dates from the year 1980 to 2050.	—
RTIC	Run-Time Integrity Checkers	Security	The RTIC ensures the integrity of the peripheral memory contents and assists with boot authentication.	—

Table 11. Fusebox Supply Current Parameters

Ref. Num	Description	Symbol	Minimum	Typical	Maximum	Units
1	eFuse Program Current. ¹ Current to program one eFuse bit: efuse_pgm = 3.0 V	I_{program}	—	35	60	mA
2	eFuse Read Current ² Current to read an 8-bit eFuse word vdd_fusebox = 1.875 V	I_{read}	—	5	8	mA

¹ The current I_{program} is during program time (t_{program}).

² The current I_{read} is present for approximately 50 ns of the read access to the 8-bit word, and only applies to Silicon Rev. 1.2 and previous.

4.1.1 Supply Current Specifications

Table 12 shows the core current consumption for -40°C to 85°C for Silicon Revision 2.0.1 for the MCIMX31.

Table 12. Current Consumption for -40°C to 85°C^{1, 2} for Silicon Revision 2.0.1

Mode	Conditions	QVCC (Peripheral)		QVCC1 (ARM)		QVCC4 (L2)		FVCC + MVCC + SVCC + UVCC (PLL)		Unit
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Deep Sleep	<ul style="list-style-type: none"> QVCC = 0.95 V ARM and L2 caches are power gated (QVCC1 = QVCC4 = 0 V) All PLLs are off, VCC = 1.4 V ARM is in well bias FPM is off 32 kHz input is on CKIH input is off CAMP is off TCK input is off All modules are off No external resistive loads RNGA oscillator is off 	0.16	5.50	—	—	—	—	0.02	0.10	mA
State Retention	<ul style="list-style-type: none"> QVCC and QVCC1 = 0.95 V L2 caches are power gated (QVCC4 = 0 V) All PLLs are off, VCC = 1.4 V ARM is in well bias FPM is off 32 kHz input is on CKIH input is off CAMP is off TCK input is off All modules are off No external resistive loads RNGA oscillator is off 	0.16	5.50	0.07	2.20	—	—	0.02	0.10	mA
Wait	<ul style="list-style-type: none"> QVCC, QVCC1, and QVCC4 = 1.22 V ARM is in wait for interrupt mode MAX is active L2 cache is stopped but powered MCU PLL is on (532 MHz), VCC = 1.4 V USB PLL and SPPLL are off, VCC = 1.4 V FPM is on CKIH input is on CAMP is on 32 kHz input is on All clocks are gated off All modules are off (by programming CGR[2:0] registers) RNGA oscillator is off No external resistive loads 	6.00	15.00	2.20	25.00	0.03	0.29	3.60	4.40	mA

¹ Typical column: TA = 25°C

² Maximum column: TA = 85°C

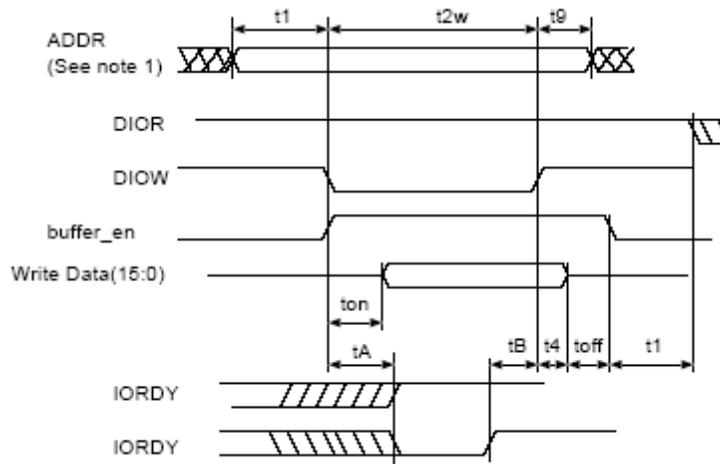


Figure 11. Multiword DMA (MDMA) Timing

Table 25. PIO Write Timing Parameters

ATA Parameter	Parameter from Figure 11	Value	Controlling Variable
t_1	t_1	$t_1 \text{ (min)} = \text{time_1} * T - (\text{tskew1} + \text{tskew2} + \text{tskew5})$	time_1
t_2	t_{2w}	$t_2 \text{ (min)} = \text{time_2w} * T - (\text{tskew1} + \text{tskew2} + \text{tskew5})$	time_2w
t_9	t_9	$t_9 \text{ (min)} = \text{time_9} * T - (\text{tskew1} + \text{tskew2} + \text{tskew6})$	time_9
t_3	—	$t_3 \text{ (min)} = (\text{time_2w} - \text{time_on}) * T - (\text{tskew1} + \text{tskew2} + \text{tskew5})$	If not met, increase time_2w
t_4	t_4	$t_4 \text{ (min)} = \text{time_4} * T - \text{tskew1}$	time_4
t_A	t_A	$t_A = (1.5 + \text{time_ax}) * T - (\text{tco} + \text{tsui} + \text{tcable2} + \text{tcable2} + 2 * \text{tbuf})$	time_ax
t_0	—	$t_0 \text{ (min)} = (\text{time_1} + \text{time_2} + \text{time_9}) * T$	time_1, time_2r, time_9
—	—	Avoid bus contention when switching buffer on by making t_{on} long enough.	—
—	—	Avoid bus contention when switching buffer off by making t_{off} long enough.	—

Figure 12 shows timing for MDMA read, Figure 13 shows timing for MDMA write, and Table 26 lists the timing parameters for MDMA read and write.

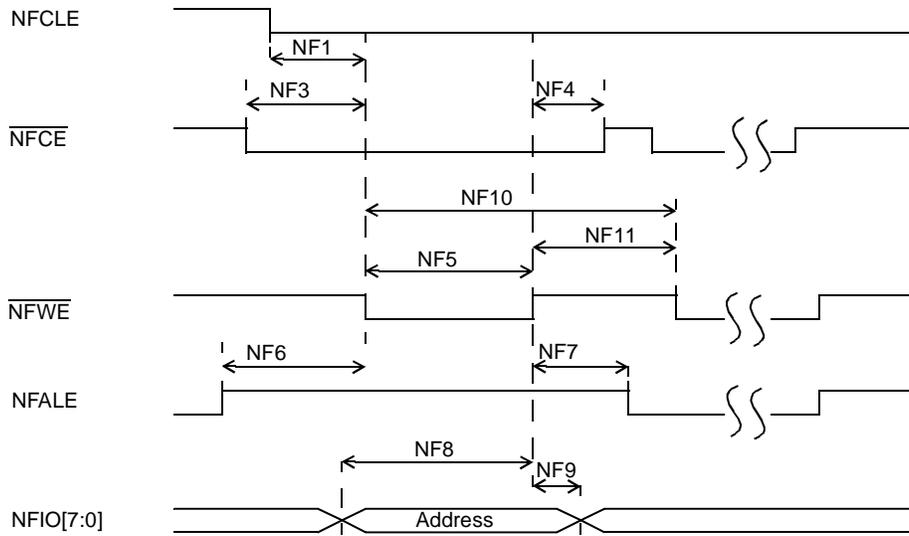


Figure 23. Address Latch Cycle Timing Diagram

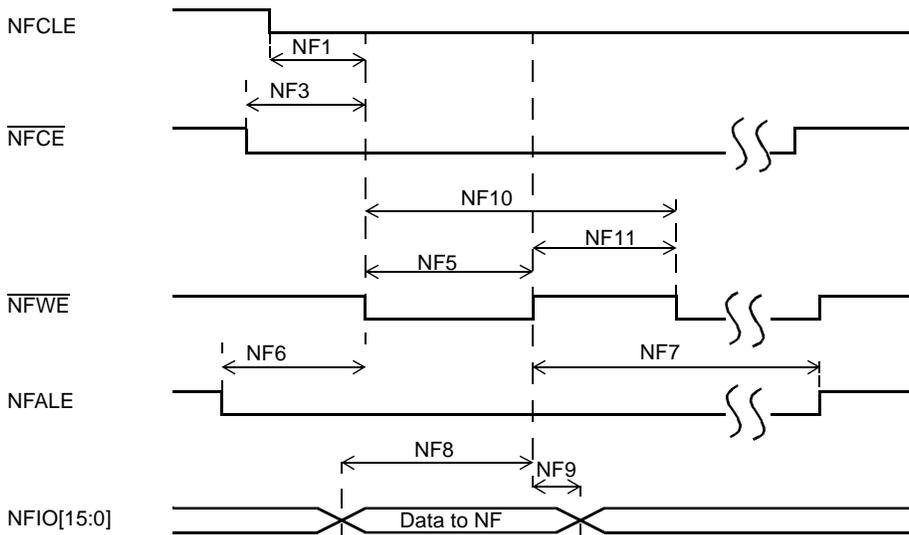


Figure 24. Write Data Latch Cycle Timing Diagram

Electrical Characteristics

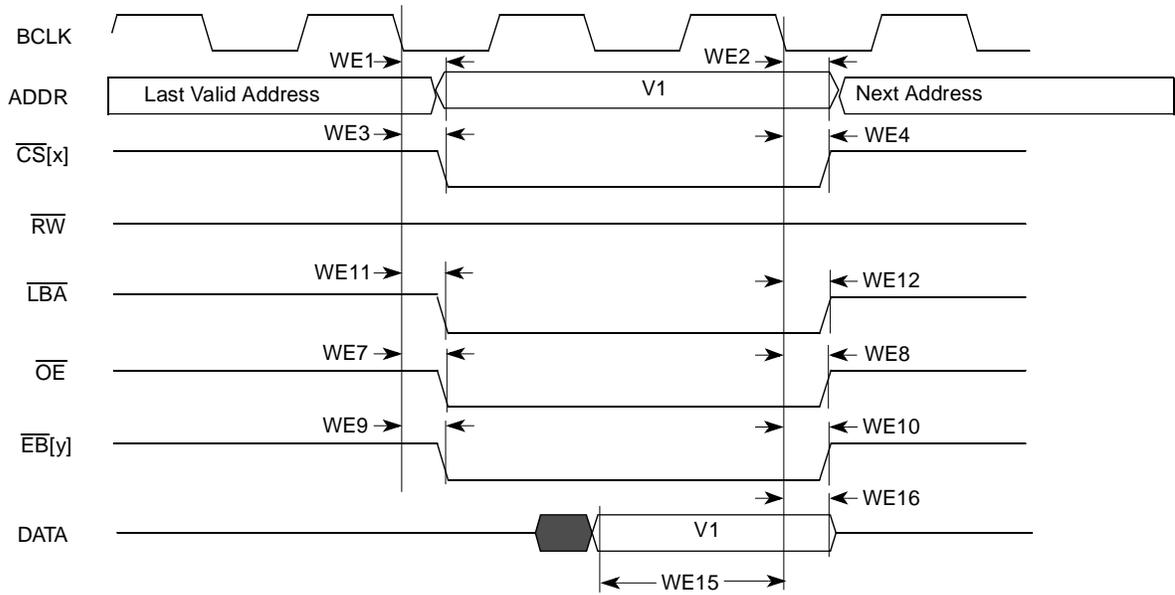


Figure 27. Asynchronous Memory Timing Diagram for Read Access—WSC=1

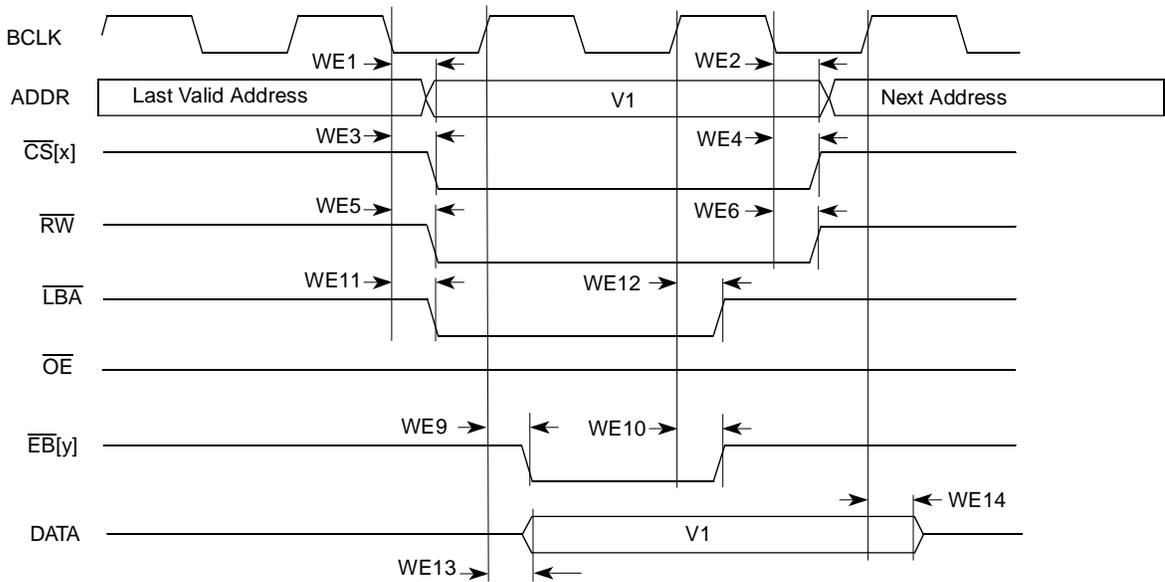


Figure 28. Asynchronous Memory Timing Diagram for Write Access—WSC=1, EBWA=1, EBWN=1, LBN=1

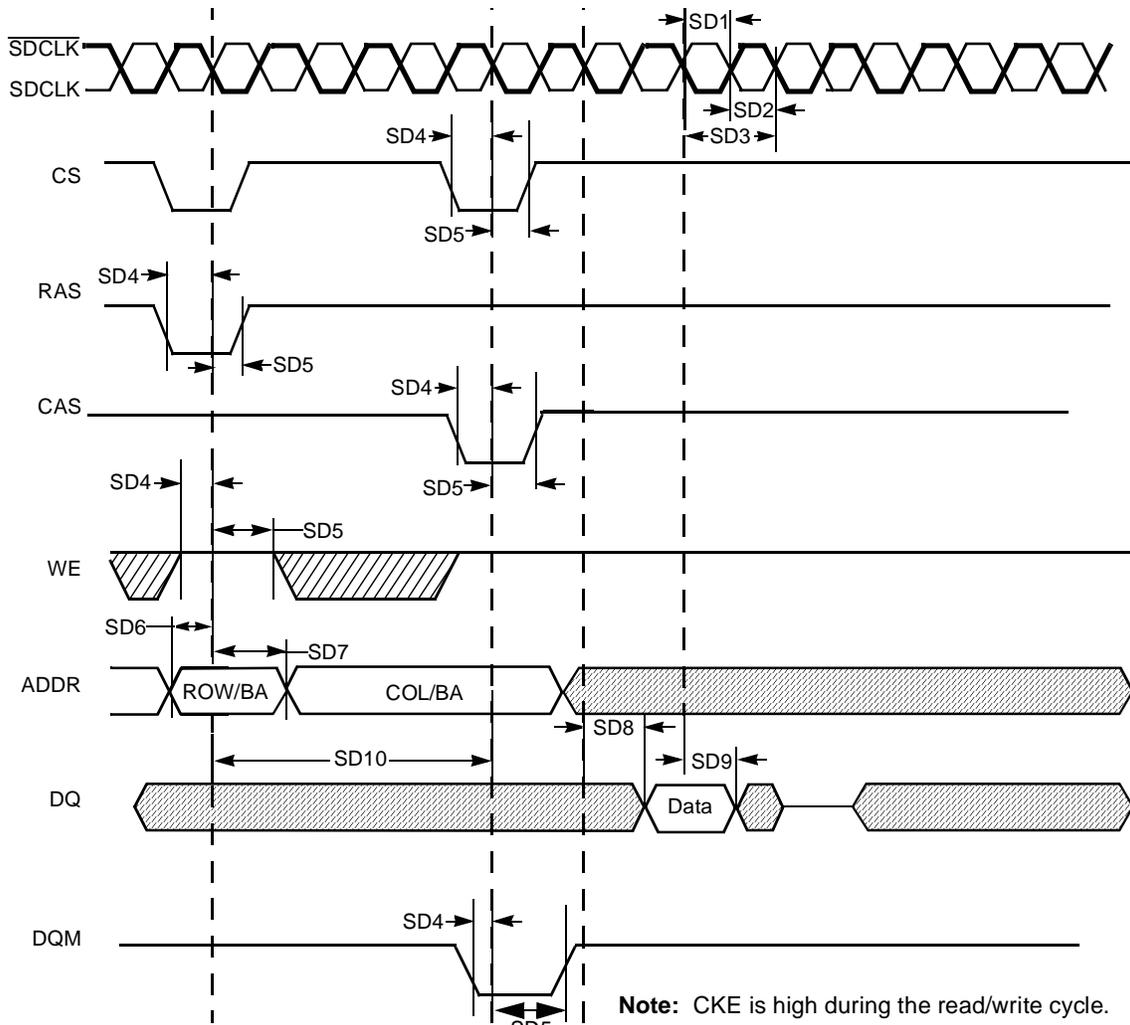


Figure 33. SDRAM Read Cycle Timing Diagram

Table 33. DDR/SDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	SDRAM clock low-level width	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD4	CS, RAS, CAS, WE, DQM, CKE setup time	tCMS	2.0	—	ns
SD5	CS, RAS, CAS, WE, DQM, CKE hold time	tCMH	1.8	—	ns
SD6	Address setup time	tAS	2.0	—	ns
SD7	Address hold time	tAH	1.8	—	ns
SD8	SDRAM access time	tAC	—	6.47	ns

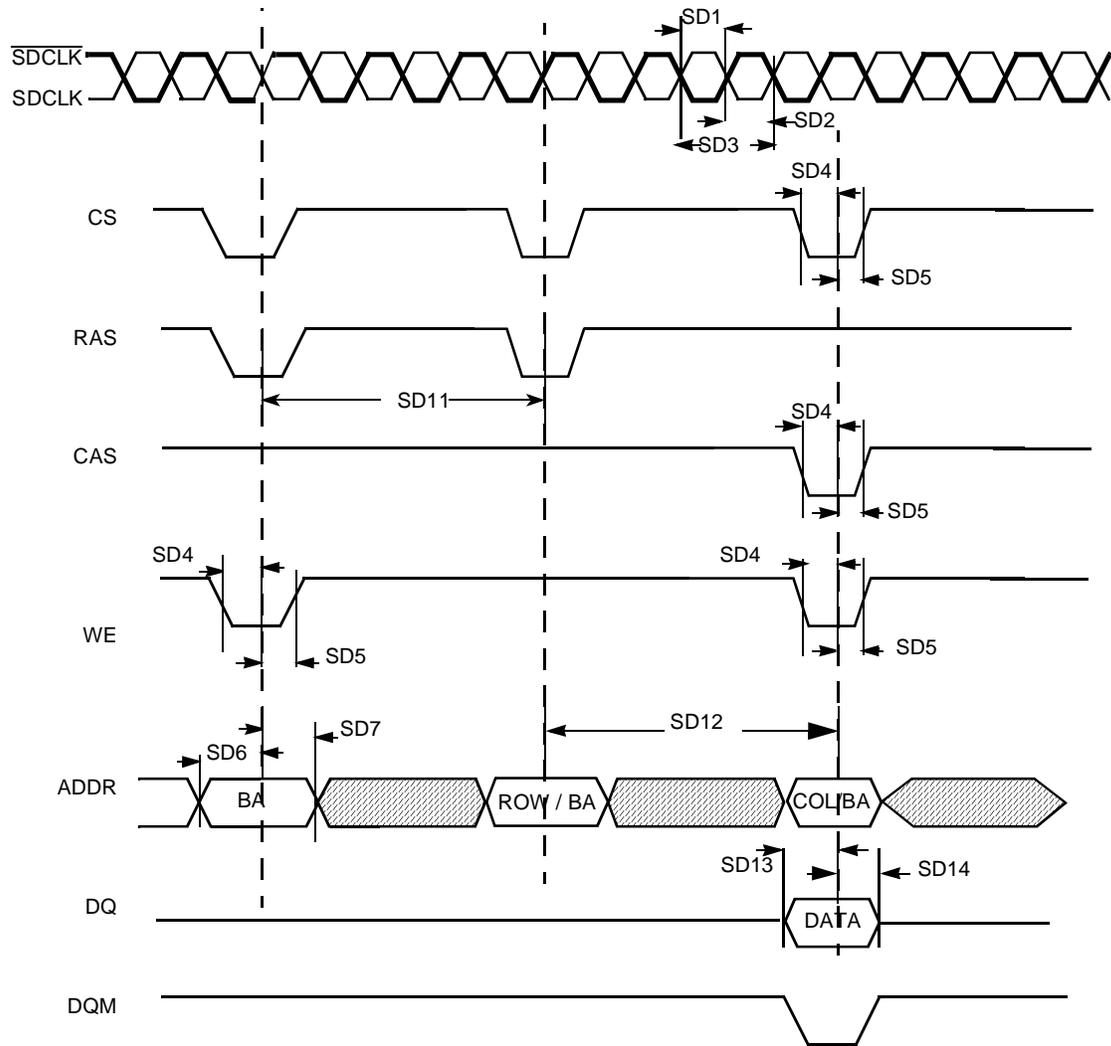


Figure 34. SDR SDRAM Write Cycle Timing Diagram

Table 34. SDR SDRAM Write Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	SDRAM clock low-level width	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD4	CS, RAS, CAS, WE, DQM, CKE setup time	tCMS	2.0	—	ns
SD5	CS, RAS, CAS, WE, DQM, CKE hold time	tCMH	1.8	—	ns
SD6	Address setup time	tAS	2.0	—	ns
SD7	Address hold time	tAH	1.8	—	ns
SD11	Precharge cycle period ¹	tRP	1	4	clock
SD12	Active to read/write command delay ¹	tRCD	1	8	clock

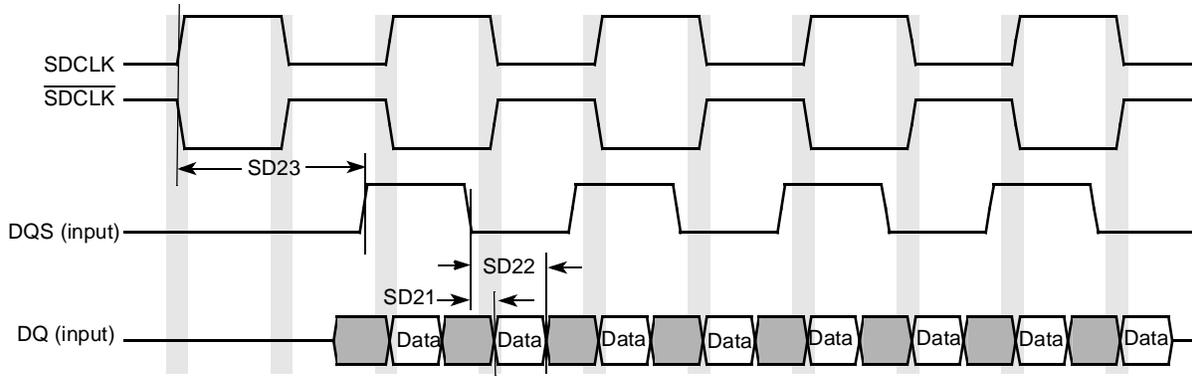


Figure 38. Mobile DDR SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram

Table 38. Mobile DDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
SD21	DQS – DQ Skew (defines the Data valid window in read cycles related to DQS).	tDQSQ	—	0.85	ns
SD22	DQS DQ HOLD time from DQS	tQH	2.3	—	ns
SD23	DQS output access time from SDCLK posedge	tDQSK	—	6.7	ns

NOTE

SDRAM CLK and DQS related parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 38 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

4.3.10 ETM Electrical Specifications

ETM is an ARM protocol. The timing specifications in this section are given as a guide for a TPA that supports TRACECLK frequencies up to 133 MHz.

Figure 39 depicts the TRACECLK timings of ETM, and Table 39 lists the timing parameters.

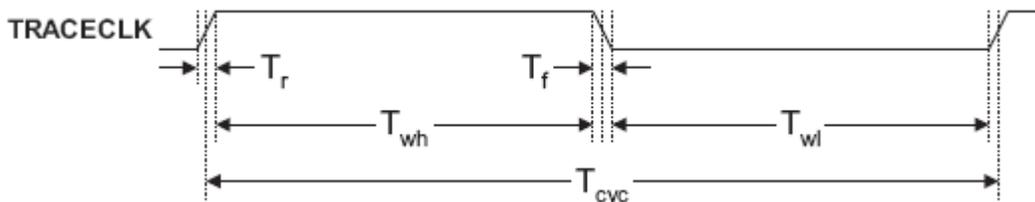


Figure 39. ETM TRACECLK Timing Diagram

4.3.13 I²C Electrical Specifications

This section describes the electrical information of the I²C Module.

4.3.13.1 I²C Module Timing

Figure 41 depicts the timing of I²C module. Table 42 lists the I²C module timing parameters where the I/O supply is 2.7 V. 1

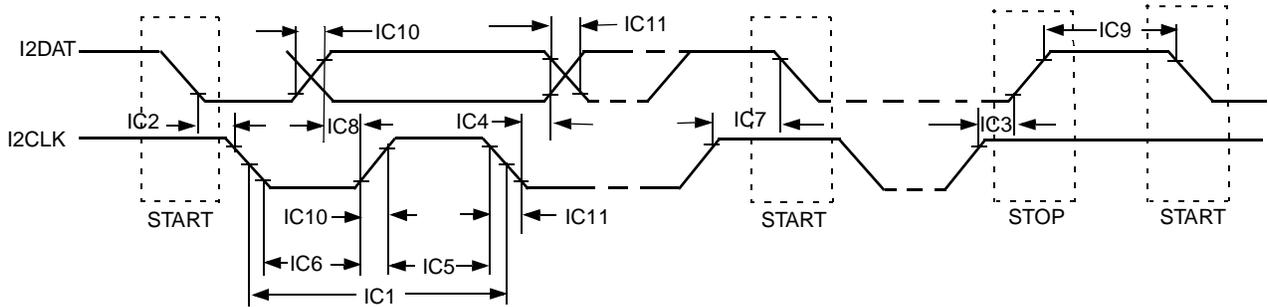


Figure 41. I²C Bus Timing Diagram

Table 42. I²C Module Timing Parameters—I²C Pin I/O Supply=2.7 V

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2CLK cycle time	10	—	2.5	—	μs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	μs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	μs
IC4	Data hold time	0 ¹	3.45 ²	0 ¹	0.9 ²	μs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	μs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	μs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	μs
IC8	Data set-up time	250	—	100 ³	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	μs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	20+0.1C _b ⁴	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	20+0.1C _b ⁴	300	ns
IC12	Capacitive load for each bus line (C _b)	—	400	—	400	pF

¹ A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

² The maximum hold time has to be met only if the device does not stretch the LOW period (ID IC6) of the I2CLK signal.

³ A Fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement of set-up time (ID IC7) of 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (ID No IC10) + data_setup_time (ID No IC8) = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the I2CLK line is released.

⁴ C_b = total capacitance of one bus line in pF.

4.3.14 IPU—Sensor Interfaces

4.3.14.1 Supported Camera Sensors

Table 43 lists the known supported camera sensors at the time of publication.

Table 43. Supported Camera Sensors¹

Vendor	Model
Conexant	CX11646, CX20490 ² , CX20450 ²
Agilent	HDCCP-2010, ADCS-1021 ² , ADCS-1021 ²
Toshiba	TC90A70
ICMedia	ICM202A, ICM102 ²
iMagic	IM8801
Transchip	TC5600, TC5600J, TC5640, TC5700, TC6000
Fujitsu	MB86S02A
Micron	MI-SOC-0133
Matsushita	MN39980
STMicro	W6411, W6500, W6501 ² , W6600 ² , W6552 ² , STV0974 ²
OmniVision	OV7620, OV6630
Sharp	LZ0P3714 (CCD)
Motorola	MC30300 (Python) ² , SCM20014 ² , SCM20114 ² , SCM22114 ² , SCM20027 ²
National Semiconductor	LM9618 ²

¹ Freescale Semiconductor does not recommend one supplier over another and in no way suggests that these are the only camera suppliers.

² These sensors not validated at time of publication.

4.3.14.2 Functional Description

There are three timing modes supported by the IPU.

4.3.14.2.1 Pseudo BT.656 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the SENS_B_VSYNC and SENS_B_HSYNC signals. The timing syntax is defined by the BT.656 standard.

This operation mode follows the recommendations of ITU BT.656 specifications. The only control signal used is SENS_B_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering SENS_B_VSYNC and SENS_B_HSYNC signals for internal use.

NOTE

HSP_CLK is the High-Speed Port Clock, which is the input to the Image Processing Unit (IPU). Its frequency is controlled by the Clock Control Module (CCM) settings. The HSP_CLK frequency must be greater than or equal to the AHB clock frequency.

The SCREEN_WIDTH, SCREEN_HEIGHT, H_SYNC_WIDTH, V_SYNC_WIDTH, BGXP, BGYP and V_SYNC_WIDTH_L parameters are programmed via the SDC_HOR_CONF, SDC_VER_CONF, SDC_BG_POS Registers. The FW and FH parameters are programmed for the corresponding DMA channel. The DISP3_IF_CLK_PER_WR, HSP_CLK_PERIOD and DISP3_IF_CLK_CNT_D parameters are programmed via the DI_DISP3_TIME_CONF, DI_HSP_CLK_PER and DI_DISP_ACC_CC Registers.

Figure 48 depicts the synchronous display interface timing for access level, and Table 47 lists the timing parameters. The DISP3_IF_CLK_DOWN_WR and DISP3_IF_CLK_UP_WR parameters are set via the DI_DISP3_TIME_CONF Register.

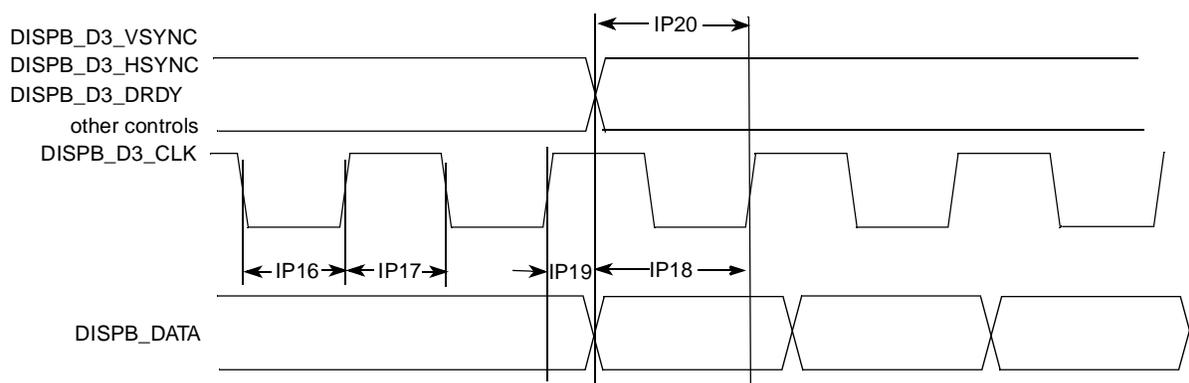


Figure 48. Synchronous Display Interface Timing Diagram—Access Level

Table 47. Synchronous Display Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min	Typ ¹	Max	Units
IP16	Display interface clock low time	Tckl	Tdicd–Tdicu–1.5	Tdicd ² –Tdicu ³	Tdicd–Tdicu+1.5	ns
IP17	Display interface clock high time	Tckh	Tdicp–Tdicd+Tdicu–1.5	Tdicp–Tdicd+Tdicu	Tdicp–Tdicd+Tdicu+1.5	ns
IP18	Data setup time	Tdsu	Tdicd–3.5	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp–Tdicd–3.5	Tdicp–Tdicu	—	ns
IP20	Control signals setup time to display interface clock	Tcsu	Tdicd–3.5	Tdicu	—	ns

¹ The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

Electrical Characteristics

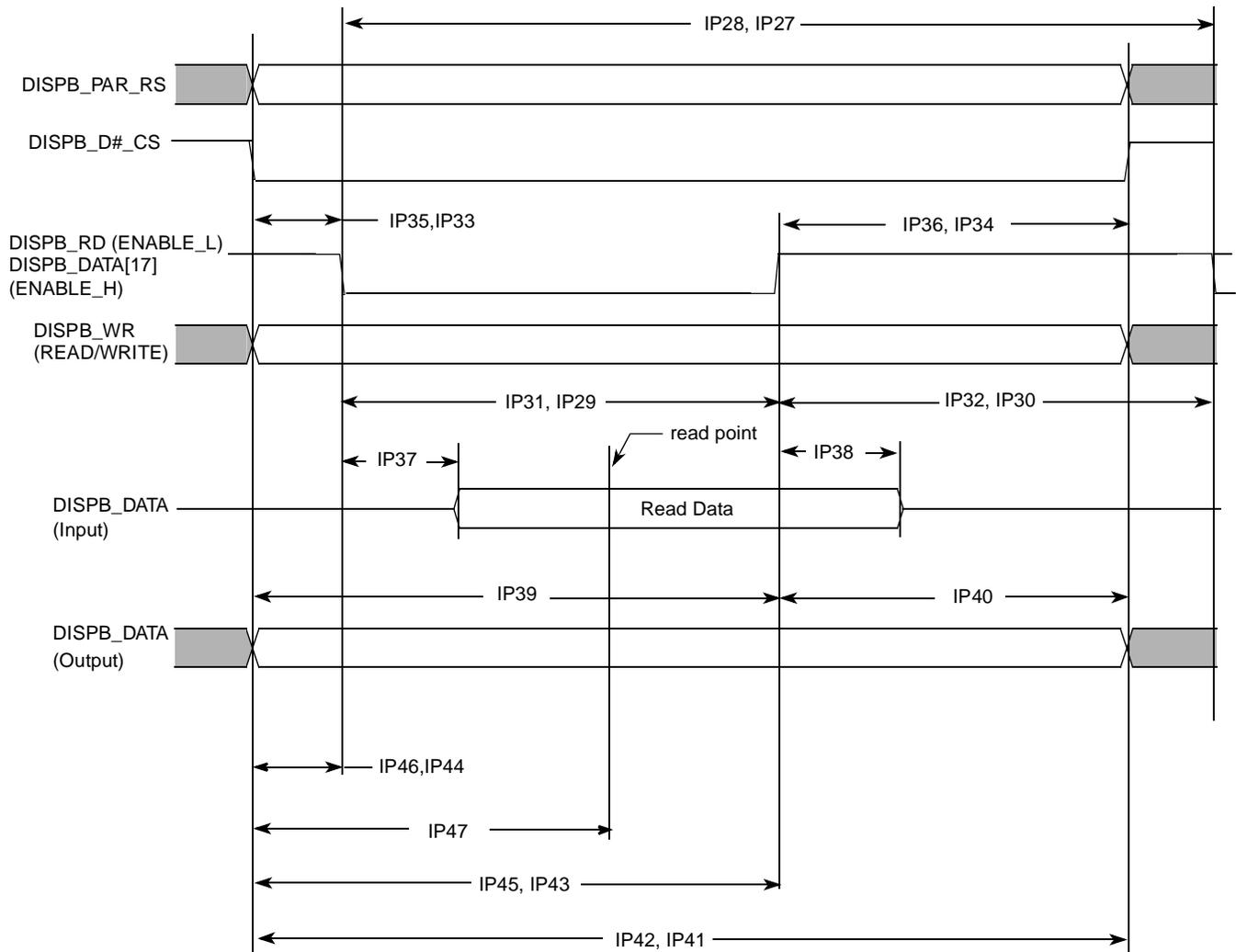


Figure 59. Asynchronous Parallel System 68k Interface (Type 2) Timing Diagram

Table 49. Asynchronous Parallel Interface Timing Parameters—Access Level

ID	Parameter	Symbol	Min.	Typ. ¹	Max.	Units
IP27	Read system cycle time	Tcycr	Tdicpr-1.5	Tdicpr ²	Tdicpr+1.5	ns
IP28	Write system cycle time	Tcycw	Tdicpw-1.5	Tdicpw ³	Tdicpw+1.5	ns
IP29	Read low pulse width	Trl	Tdicdr-Tdicur-1.5	Tdicdr ⁴ -Tdicur ⁵	Tdicdr-Tdicur+1.5	ns
IP30	Read high pulse width	Trh	Tdicpr-Tdicdr+Tdicur-1.5	Tdicpr-Tdicdr+Tdicur	Tdicpr-Tdicdr+Tdicur+1.5	ns
IP31	Write low pulse width	Twl	Tdicdw-Tdicuw-1.5	Tdicdw ⁶ -Tdicuw ⁷	Tdicdw-Tdicuw+1.5	ns
IP32	Write high pulse width	Twh	Tdicpw-Tdicdw+Tdicuw-1.5	Tdicpw-Tdicdw+Tdicuw	Tdicpw-Tdicdw+Tdicuw+1.5	ns
IP33	Controls setup time for read	Tdcsr	Tdicur-1.5	Tdicur	—	ns
IP34	Controls hold time for read	Tdchr	Tdicpr-Tdicdr-1.5	Tdicpr-Tdicdr	—	ns
IP35	Controls setup time for write	Tdcsw	Tdicuw-1.5	Tdicuw	—	ns

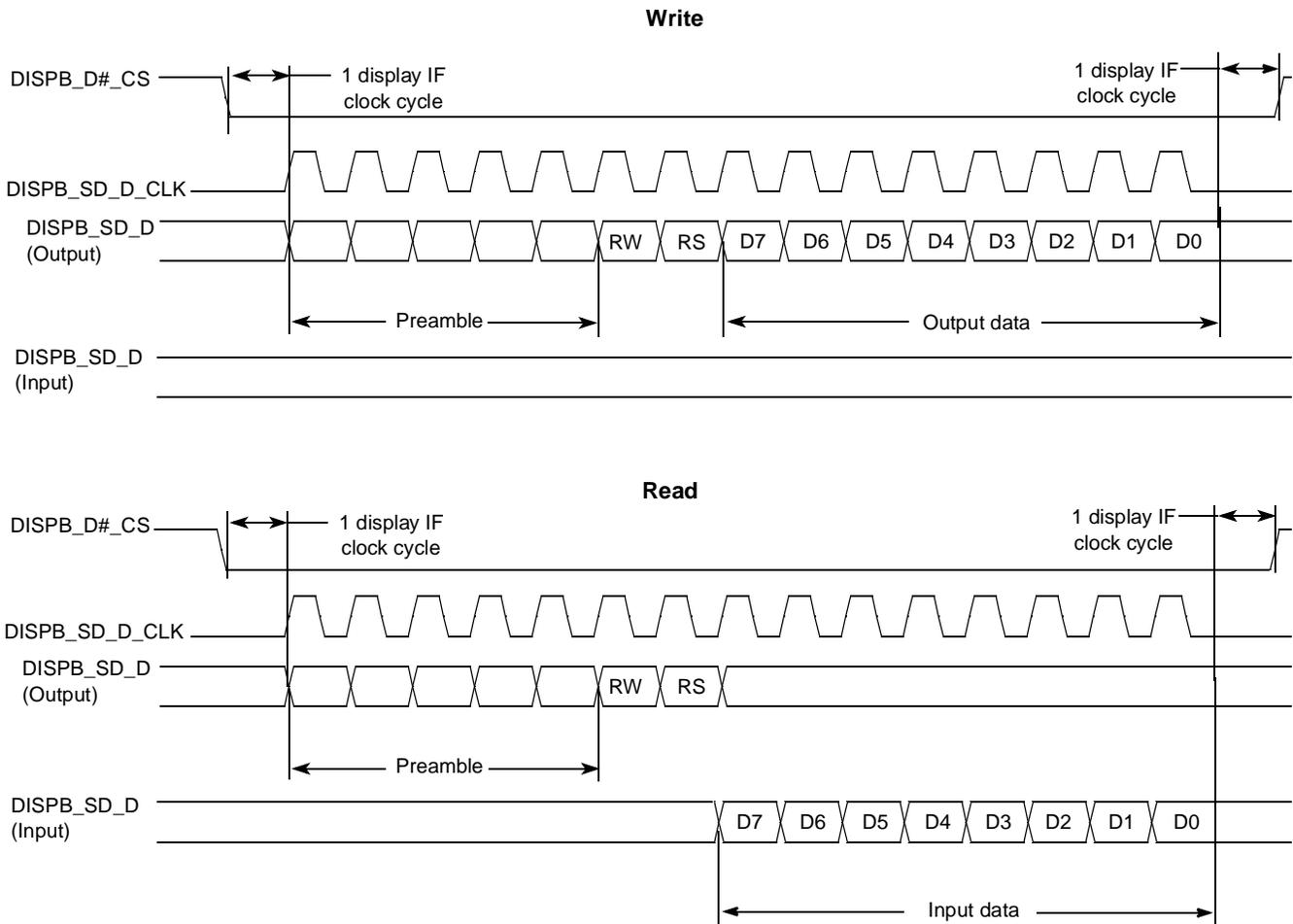


Figure 61. 4-Wire Serial Interface Timing Diagram

Figure 62 depicts timing of the 5-wire serial interface (Type 1). For this interface, a separate RS line is added. When a burst is transmitted within single active chip select interval, the RS can be changed at boundaries of words.

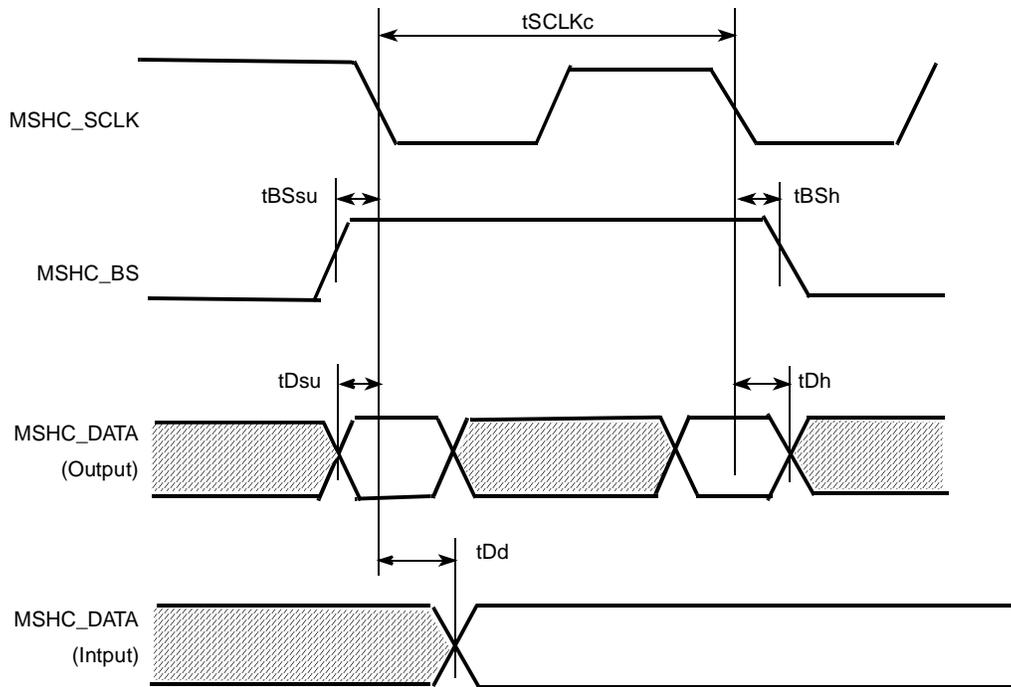


Figure 67. Transfer Operation Timing Diagram (Parallel)

NOTE

The Memory Stick Host Controller is designed to meet the timing requirements per Sony's *Memory Stick Pro Format Specifications* document. Tables in this section details the specifications requirements for parallel and serial modes, and not the MCIMX31 timing.

Table 51. Serial Interface Timing Parameters¹

Signal	Parameter	Symbol	Standards		Unit
			Min.	Max.	
MSHC_SCLK	Cycle	tSCLKc	50	—	ns
	H pulse length	tSCLKwh	15	—	ns
	L pulse length	tSCLKwl	15	—	ns
	Rise time	tSCLKr	—	10	ns
	Fall time	tSCLKf	—	10	ns
MSHC_BS	Setup time	tBSsu	5	—	ns
	Hold time	tBSsh	5	—	ns
MSHC_DATA	Setup time	tDsu	5	—	ns
	Hold time	tDh	5	—	ns
	Output delay time	tDd	—	15	ns

¹ Timing is guaranteed for NVCC from 2.7 through 3.1 V and up to a maximum overdrive NVCC of 3.3 V. See NVCC restrictions described in [Table 8, "Operating Ranges," on page 13.](#)

4.3.18.1 PWM Timing

Figure 70 depicts the timing of the PWM, and Table 54 lists the PWM timing characteristics.

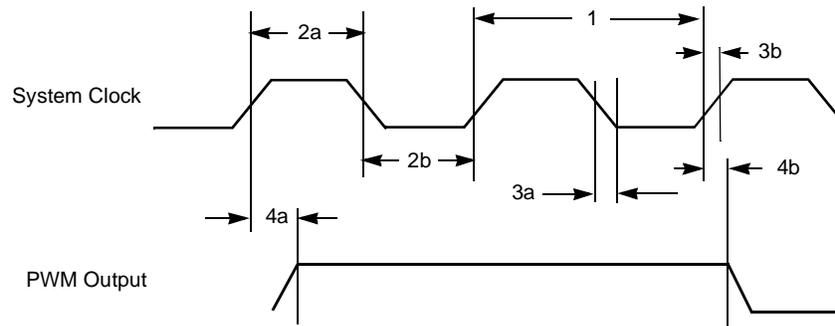


Figure 70. PWM Timing

Table 54. PWM Output Timing Parameters

ID	Parameter	Min	Max	Unit
1	System CLK frequency ¹	0	ipg_clk	MHz
2a	Clock high time	12.29	—	ns
2b	Clock low time	9.91	—	ns
3a	Clock fall time	—	0.5	ns
3b	Clock rise time	—	0.5	ns
4a	Output delay time	—	9.37	ns
4b	Output setup time	8.71	—	ns

¹ CL of PWMO = 30 pF

4.3.19 SDHC Electrical Specifications

This section describes the electrical information of the SDHC.

4.3.19.1 SDHC Timing

Figure 71 depicts the timings of the SDHC, and Table 55 lists the timing parameters.

Table 60. SSI Receiver with Internal Clock Timing Parameters

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6	ns
SS7	(Rx) CK high to FS (bl) high	—	15.0	ns
SS9	(Rx) CK high to FS (bl) low	—	15.0	ns
SS11	(Rx) CK high to FS (wl) high	—	15.0	ns
SS13	(Rx) CK high to FS (wl) low	—	15.0	ns
SS20	SRXD setup time before (Rx) CK low	10.0	—	ns
SS21	SRXD hold time after (Rx) CK low	0	—	ns
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6	—	ns
SS49	Oversampling clock rise time	—	3	ns
SS50	Oversampling clock low period	6	—	ns
SS51	Oversampling clock fall time	—	3	ns

Table 61. SSI Transmitter with External Clock Timing Parameters

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	-10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	-10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

Table 68. 19 x 19 BGA Signal ID by Ball Grid Location (continued)

Signal ID	Ball Location	Signal ID	Ball Location
RTS2	B12	SD5	AC16
RW	V18	SD6	AA15
RXD1	C9	SD7	AB15
RXD2	A12	SD8	AC15
SCK3	P1	SD9	AA14
SCK4	G6	SDBA0	AA6
SCK5	D4	SDBA1	Y7
SDCKE0	Y17	TRSTB	F15
SDCKE1	V16	TXD1	D9
SDCLK	AC20	TXD2	F11
SDCLK	AC19	USB_BYN	C8
SDQS0	AB16	USB_OC	B8
SDQS1	AB12	USB_PWR	A8
SDQS2	AB9	USBH2_CLK	L1
SDQS3	AB6	USBH2_DATA0	M6
SDWE	AB20	USBH2_DATA1	K1
SER_RS	P23	USBH2_DIR	L2
SFS3	P2	USBH2_NXT	L4
SFS4	D3	USBH2_STP	L3
SFS5	G7	USBOTG_CLK	D8
SFS6	P4	USBOTG_DATA0	G8
SIMPD0	B18	USBOTG_DATA1	C7
SJC_MOD	C17	USBOTG_DATA2	A6
SRST0	C18	USBOTG_DATA3	F8
SRX0	A19	USBOTG_DATA4	D7
SRXD3	N3	USBOTG_DATA5	B6
SRXD4	C3	USBOTG_DATA6	A5
SRXD5	C4	USBOTG_DATA7	C6
SRXD6	R1	USBOTG_DIR	A7
STX0	F16	USBOTG_NXT	B7
STXD3	N4	USBOTG_STP	F9
STXD4	B3	VPG0	G21
STXD5	D1	VPG1	G22
STXD6	P3	VSTBY	H18
SVEN0	D17	VSYNC0	L22
TCK	F14	VSYNC3	N20
TDI	A18	WATCHDOG_RST	B21
TDO	B17	WRITE	N22
TMS	C16		