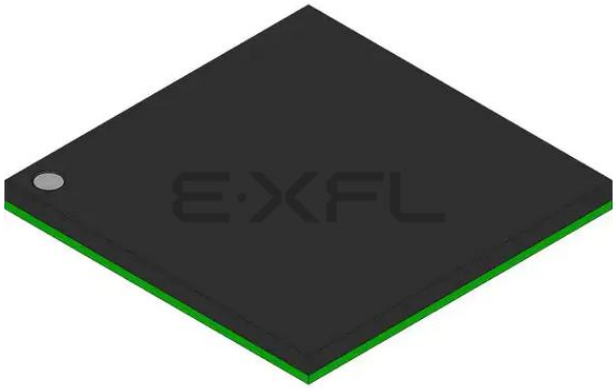

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM1136JF-S |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 532MHz |
| Co-Processors/DSP | Multimedia; GPU, IPU, MPEG-4, VFP |
| RAM Controllers | DDR |
| Graphics Acceleration | Yes |
| Display & Interface Controllers | Keyboard, Keypad, LCD |
| Ethernet | - |
| SATA | - |
| USB | USB 2.0 (3) |
| Voltage - I/O | 1.8V, 2.0V, 2.5V, 2.7V, 3.0V |
| Operating Temperature | -20°C ~ 70°C (TA) |
| Security Features | Random Number Generator, RTIC, Secure Fusebox, Secure JTAG, Secure Memory |
| Package / Case | 457-LFBGA |
| Supplier Device Package | 457-MAPBGA (14x14) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx31ldvkn5d |

**Table 11. Fusebox Supply Current Parameters**

| Ref. Num | Description | Symbol | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| 1 | eFuse Program Current.[1]<br>Current to program one eFuse bit: efuse_pgm = 3.0 V | $I_{program}$ | — | 35 | 60 | mA |
| 2 | eFuse Read Current[2]<br>Current to read an 8-bit eFuse word<br>vdd_fusebox = 1.875 V | $I_{read}$ | — | 5 | 8 | mA |

1 The current $I_{program}$ is during program time ($t_{program}$).

2 The current $I_{read}$ is present for approximately 50 ns of the read access to the 8-bit word, and only applies to Silicon Rev. 1.2 and previous.

## 4.1.1 Supply Current Specifications

Table 12 shows the core current consumption for –40°C to 85°C for Silicon Revision 2.0.1 for the MCIMX31.

**Table 12. Current Consumption for –40°C to 85°C[1, 2] for Silicon Revision 2.0.1**

| Mode | Conditions | QVCC (Peripheral) | | QVCC1 (ARM) | | QVCC4 (L2) | | FVCC + MVCC + SVCC + UVCC (PLL) | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Typ | Max | Typ | Max | Typ | Max | Typ | Max | |
| Deep Sleep | • QVCC = 0.95 V<br>• ARM and L2 caches are power gated (QVCC1 = QVCC4 = 0 V)<br>• All PLLs are off, VCC = 1.4 V<br>• ARM is in well bias<br>• FPM is off<br>• 32 kHz input is on<br>• CKIH input is off<br>• CAMP is off<br>• TCK input is off<br>• All modules are off<br>• No external resistive loads<br>• RNGA oscillator is off | 0.16 | 5.50 | — | — | — | — | 0.02 | 0.10 | mA |
| State Retention | • QVCC and QVCC1 = 0.95 V<br>• L2 caches are power gated (QVCC4 = 0 V)<br>• All PLLs are off, VCC = 1.4 V<br>• ARM is in well bias<br>• FPM is off<br>• 32 kHz input is on<br>• CKIH input is off<br>• CAMP is off<br>• TCK input is off<br>• All modules are off<br>• No external resistive loads<br>• RNGA oscillator is off | 0.16 | 5.50 | 0.07 | 2.20 | — | — | 0.02 | 0.10 | mA |
| Wait | • QVCC,QVCC1, and QVCC4 = 1.22 V<br>• ARM is in wait for interrupt mode<br>• MAX is active<br>• L2 cache is stopped but powered<br>• MCU PLL is on (532 MHz), VCC = 1.4 V<br>• USB PLL and SPLL are off, VCC = 1.4 V<br>• FPM is on<br>• CKIH input is on<br>• CAMP is on<br>• 32 kHz input is on<br>• All clocks are gated off<br>• All modules are off (by programming CGR[2:0] registers)<br>• RNGA oscillator is off<br>• No external resistive loads | 6.00 | 15.00 | 2.20 | 25.00 | 0.03 | 0.29 | 3.60 | 4.40 | mA |

1 Typical column: TA = 25°C

2 Maximum column: TA = 85°C

**Table 17. AC Electrical Characteristics of Fast[1] General I/O [2]**

| ID | Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| PA1 | Output Transition Times (Max Drive) | tpr | 25 pF<br>50 pF | 0.68<br>1.34 | 1.33<br>2.6 | 2.07<br>4.06 | ns |
| | Output Transition Times (High Drive) | tpr | 25 pF<br>50 pF | .91<br>1.79 | 1.77<br>3.47 | 2.74<br>5.41 | ns |
| | Output Transition Times (Std Drive) | tpr | 25 pF<br>50 pF | 1.36<br>2.68 | 2.64<br>5.19 | 4.12<br>8.11 | ns |

1 Fast/slow characteristic is selected per GPIO (where available) by “slew rate” control. See reference manual.

2 Use of GPIO in fast mode with the associated NVCC > 1.95 V can result in excessive overshoot and ringing.

**Table 18. AC Electrical Characteristics of DDR I/O**

| ID | Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| PA1 | Output Transition Times (DDR Drive)[1] | tpr | 25 pF<br>50 pF | 0.51<br>0.97 | 0.82<br>1.58 | 1.28<br>2.46 | ns |
| | Output Transition Times (Max Drive) | tpr | 25 pF<br>50 pF | 0.67<br>1.29 | 1.08<br>2.1 | 1.69<br>3.27 | ns |
| | Output Transition Times (High Drive) | tpr | 25 pF<br>50 pF | .99<br>1.93 | 1.61<br>3.13 | 2.51<br>4.89 | ns |
| | Output Transition Times (Std Drive) | tpr | 25 pF<br>50 pF | 1.96<br>3.82 | 3.19<br>6.24 | 4.99<br>9.73 | ns |

1 Use of DDR Drive can result in excessive overshoot and ringing.

## 4.3.3 Clock Amplifier Module (CAMP) Electrical Characteristics

This section outlines the Clock Amplifier Module (CAMP) specific electrical characteristics. Table 19 shows clock amplifier electrical characteristics.

**Table 19. Clock Amplifier Electrical Characteristics for CKIH Input**

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Input Frequency | 15 | — | 75 | MHz |
| VIL (for square wave input) | 0 | — | 0.3 | V |
| VIH (for square wave input) | (VDD [1]– 0.25) | — | 3 | V |
| Sinusoidal Input Amplitude | 0.4 [2] | — | VDD | Vp-p |
| Duty Cycle | 45 | 50 | 55 | % |

1 VDD is the supply voltage of CAMP. See reference manual.

2 This value of the sinusoidal input will be measured through characterization.

## 4.3.4 1-Wire Electrical Specifications

Figure 6 depicts the RPP timing, and Table 20 lists the RPP timing parameters.

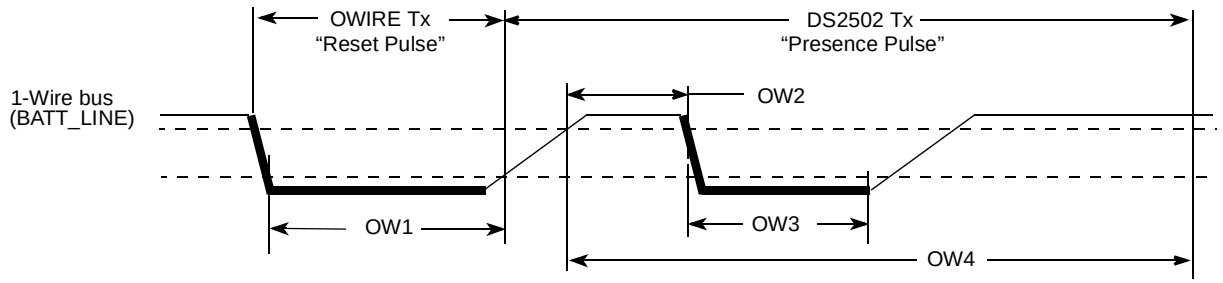


**Figure 6. Reset and Presence Pulses (RPP) Timing Diagram**

**Table 20. RPP Sequence Delay Comparisons Timing Parameters**

| ID | Parameters | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| OW1 | Reset Time Low | $t_{RSTL}$ | 480 | 511 | — | µs |
| OW2 | Presence Detect High | $t_{PDH}$ | 15 | — | 60 | µs |
| OW3 | Presence Detect Low | $t_{PDL}$ | 60 | — | 240 | µs |
| OW4 | Reset Time High | $t_{RSTH}$ | 480 | 512 | — | µs |

Figure 7 depicts Write 0 Sequence timing, and Table 21 lists the timing parameters.

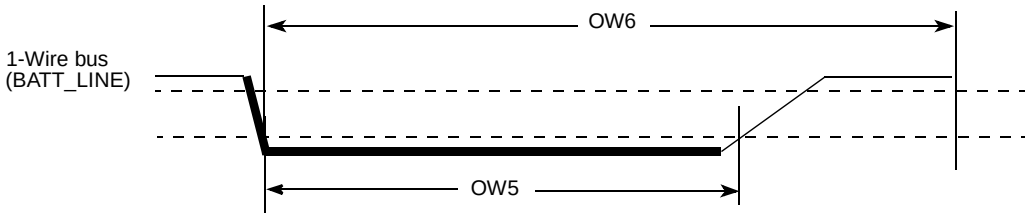


**Figure 7. Write 0 Sequence Timing Diagram**

**Table 21. WR0 Sequence Timing Parameters**

| ID | Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| OW5 | Write 0 Low Time | $t_{WR0\_low}$ | 60 | 100 | 120 | µs |
| OW6 | Transmission Time Slot | $t_{SLOT}$ | OW5 | 117 | 120 | µs |

Figure 8 depicts Write 1 Sequence timing, Figure 9 depicts the Read Sequence timing, and Table 22 lists the timing parameters.

### 4.3.5.2 PIO Mode Timing

Figure 10 shows timing for PIO read, and Table 24 lists the timing parameters for PIO read.

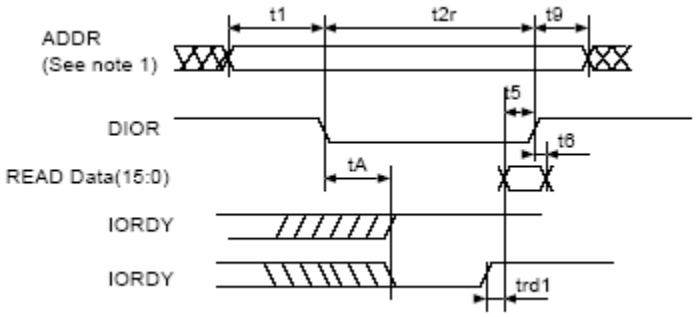


**Figure 10. PIO Read Timing Diagram**

**Table 24. PIO Read Timing Parameters**

| ATA Parameter | Parameter from Figure 10 | Value | Controlling Variable |
|---|---|---|---|
| t1 | t1 | t1 (min) = time_1 * T – (tskew1 + tskew2 + tskew5) | time_1 |
| t2 | t2r | t2 min) = time_2r * T – (tskew1 + tskew2 + tskew5) | time_2r |
| t9 | t9 | t9 (min) = time_9 * T – (tskew1 + tskew2 + tskew6) | time_3 |
| t5 | t5 | t5 (min) = tco + tsu + tbuf + tbuf + tcable1 + tcable2 | If not met, increase time_2 |
| t6 | t6 | 0 | — |
| tA | tA | tA (min) = (1.5 + time_ax) * T – (tco + tsui + tcable2 + tcable2 + 2*tbuf) | time_ax |
| trd | trd1 | trd1 (max) = (–trd) + (tskew3 + tskew4)<br>trd1 (min) = (time_pio_rdx – 0.5)*T – (tsu + thi)<br>(time_pio_rdx – 0.5) * T > tsu + thi + tskew3 + tskew4 | time_pio_rdx |
| t0 | — | t0 (min) = (time_1 + time_2 + time_9) * T | time_1, time_2r, time_9 |

Figure 11 shows timing for PIO write, and Table 25 lists the timing parameters for PIO write.

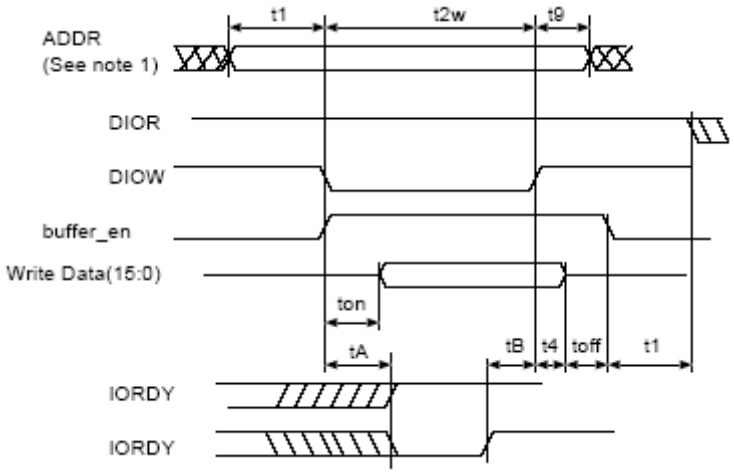


**Figure 11. Multiword DMA (MDMA) Timing**

**Table 25. PIO Write Timing Parameters**

| ATA Parameter | Parameter from Figure 11 | Value | Controlling Variable |
|---|---|---|---|
| t1 | t1 | t1 (min) = time_1 * T – (tskew1 + tskew2 + tskew5) | time_1 |
| t2 | t2w | t2 (min) = time_2w * T – (tskew1 + tskew2 + tskew5) | time_2w |
| t9 | t9 | t9 (min) = time_9 * T – (tskew1 + tskew2 + tskew6) | time_9 |
| t3 | — | t3 (min) = (time_2w – time_on)* T – (tskew1 + tskew2 +tskew5) | If not met, increase time_2w |
| t4 | t4 | t4 (min) = time_4 * T – tskew1 | time_4 |
| tA | tA | tA = (1.5 + time_ax) * T – (tco + tsui + tcable2 + tcable2 + 2*tbuf) | time_ax |
| t0 | — | t0(min) = (time_1 + time_2 + time_9) * T | time_1, time_2r, time_9 |
| — | — | Avoid bus contention when switching buffer on by making ton long enough. | — |
| — | — | Avoid bus contention when switching buffer off by making toff long enough. | — |

Figure 12 shows timing for MDMA read, Figure 13 shows timing for MDMA write, and Table 26 lists the timing parameters for MDMA read and write.

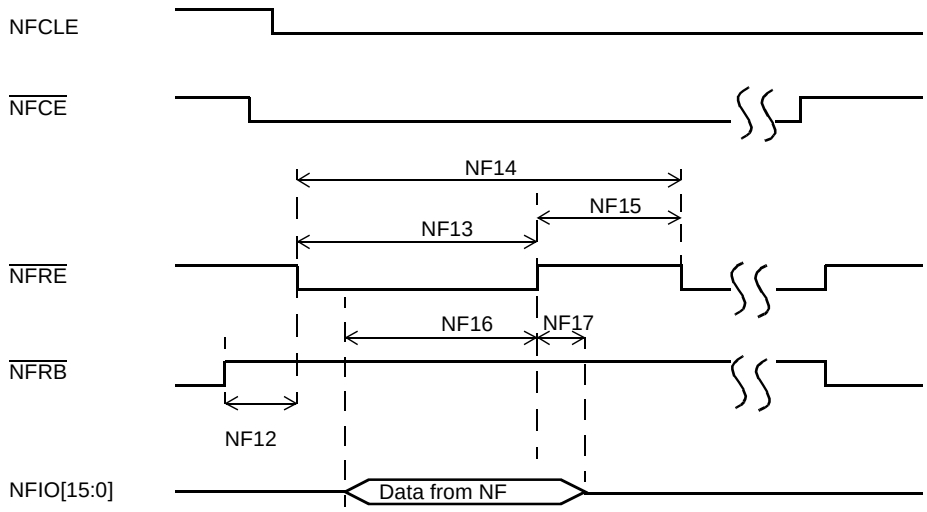


**Figure 25. Read Data Latch Cycle Timing Diagram**

**Table 31. NFC Timing Parameters[1]**

| ID | Parameter | Symbol | Timing T = NFC Clock Cycle[2] | | Example Timing for NFC Clock ≈ 33 MHz T = 30 ns | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| NF1 | NFCLE Setup Time | tCLS | T–1.0 ns | — | 29 | — | ns |
| NF2 | NFCLE Hold Time | tCLH | T–2.0 ns | — | 28 | — | ns |
| NF3 | $\overline{\text{NFCE}}$ Setup Time | tCS | T–1.0 ns | — | 29 | — | ns |
| NF4 | $\overline{\text{NFCE}}$ Hold Time | tCH | T–2.0 ns | — | 28 | — | ns |
| NF5 | $\overline{\text{NF\_WP}}$ Pulse Width | tWP | T–1.5 ns | | 28.5 | | ns |
| NF6 | NFALE Setup Time | tALS | T | — | 30 | — | ns |
| NF7 | NFALE Hold Time | tALH | T–3.0 ns | — | 27 | — | ns |
| NF8 | Data Setup Time | tDS | T | — | 30 | — | ns |
| NF9 | Data Hold Time | tDH | T–5.0 ns | — | 25 | — | ns |
| NF10 | Write Cycle Time | tWC | 2T | | 60 | | ns |
| NF11 | $\overline{\text{NFWE}}$ Hold Time | tWH | T–2.5 ns | | 27.5 | | ns |
| NF12 | Ready to $\overline{\text{NFRE}}$ Low | tRR | 6T | — | 180 | — | ns |
| NF13 | $\overline{\text{NFRE}}$ Pulse Width | tRP | 1.5T | — | 45 | — | ns |
| NF14 | READ Cycle Time | tRC | 2T | — | 60 | — | ns |
| NF15 | $\overline{\text{NFRE}}$ High Hold Time | tREH | 0.5T–2.5 ns | | 12.5 | — | ns |
| NF16 | Data Setup on READ | tDSR | N/A | | 10 | — | ns |
| NF17 | Data Hold on READ | tDHR | N/A | | 0 | — | ns |

1 The flash clock maximum frequency is 50 MHz.

2 Subject to DPLL jitter specification on Table 30, "DPLL Specifications," on page 35.

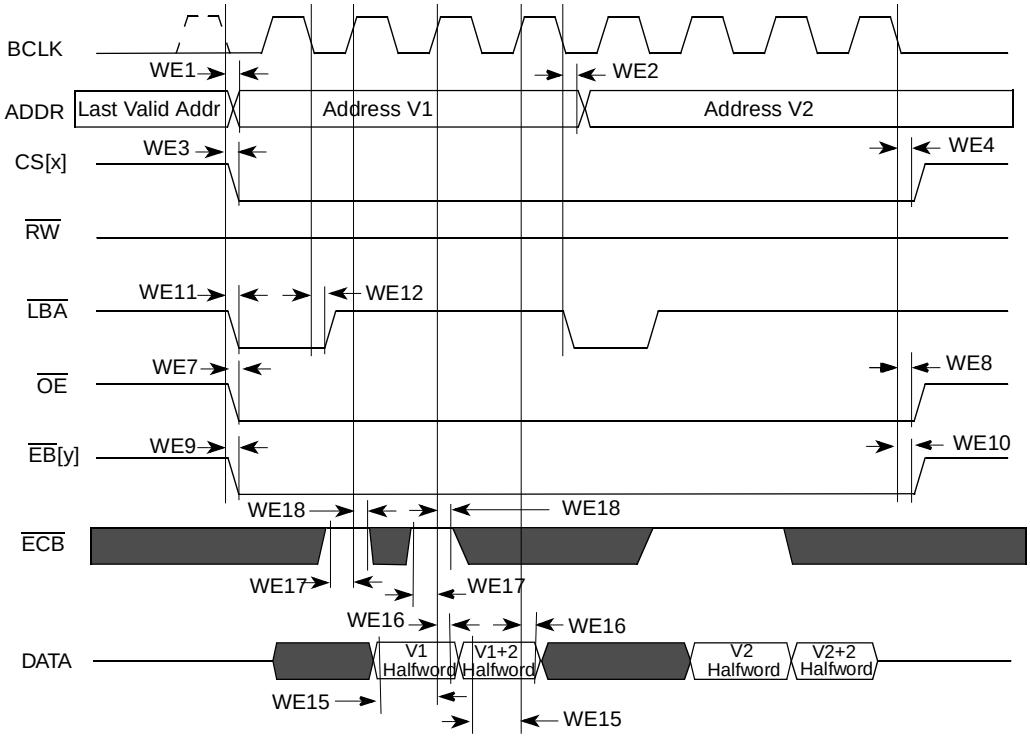


**Figure 29. Synchronous Memory Timing Diagram for Two Non-Sequential Read Accesses—WSC=2, SYNC=1, DOL=0**

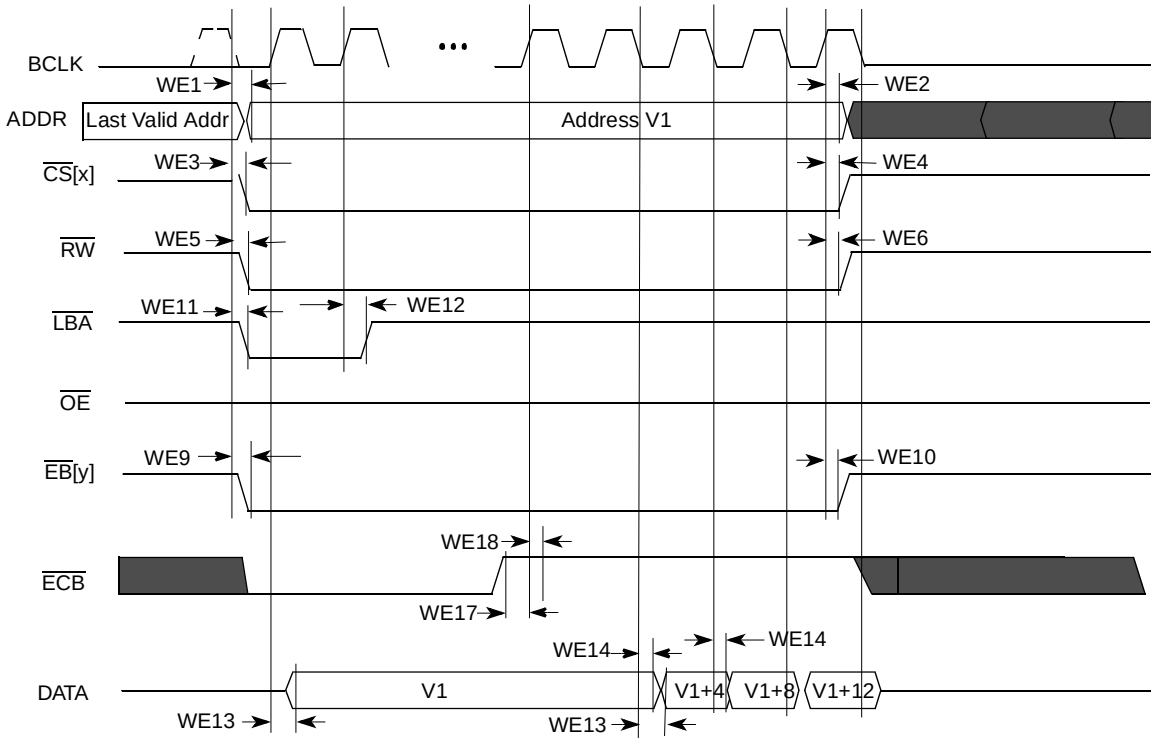


**Figure 30. Synchronous Memory TIming Diagram for Burst Write Access—BCS=1, WSC=4, SYNC=1, DOL=0, PSR=1**

**Table 39. ETM TRACECLK Timing Parameters**

| ID | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_{cyc}$ | Clock period | Frequency dependent | — | ns |
| $T_{wl}$ | Low pulse width | 2 | — | ns |
| $T_{wh}$ | High pulse width | 2 | — | ns |
| $T_r$ | Clock and data rise time | — | 3 | ns |
| $T_f$ | Clock and data fall time | — | 3 | ns |

Figure 40 depicts the setup and hold requirements of the trace data pins with respect to TRACECLK, and Table 40 lists the timing parameters.

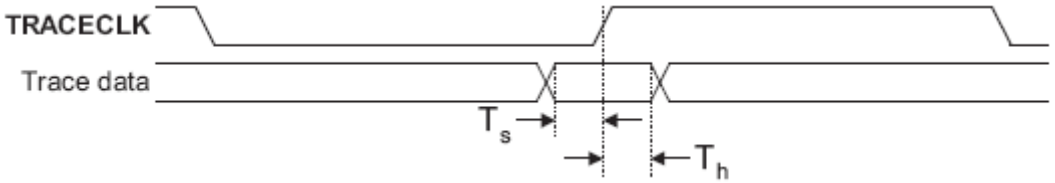


**Figure 40. Trace Data Timing Diagram**

**Table 40. ETM Trace Data Timing Parameters**

| ID | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_s$ | Data setup | 2 | — | ns |
| $T_h$ | Data hold | 1 | — | ns |

### 4.3.10.1 Half-Rate Clocking Mode

When half-rate clocking is used, the trace data signals are sampled by the TPA on both the rising and falling edges of TRACECLK, where TRACECLK is half the frequency of the clock shown in Figure 40.

## 4.3.11 FIR Electrical Specifications

FIR implements asynchronous infrared protocols (FIR, MIR) that are defined by IrDA® (Infrared Data Association). Refer to http://www.IrDA.org for details on FIR and MIR protocols.

## 4.3.12 Fusebox Electrical Specifications

**Table 41. Fusebox Timing Characteristics**

| Ref. Num | Description | Symbol | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| 1 | Program time for eFuse[1] | $t_{program}$ | 125 | — | — | µs |

1 The program length is defined by the value defined in the epm_pgm_length[2:0] bits of the IIM module. The value to program is based on a 32 kHz clock source (4 * 1/32 kHz = 125 µs).

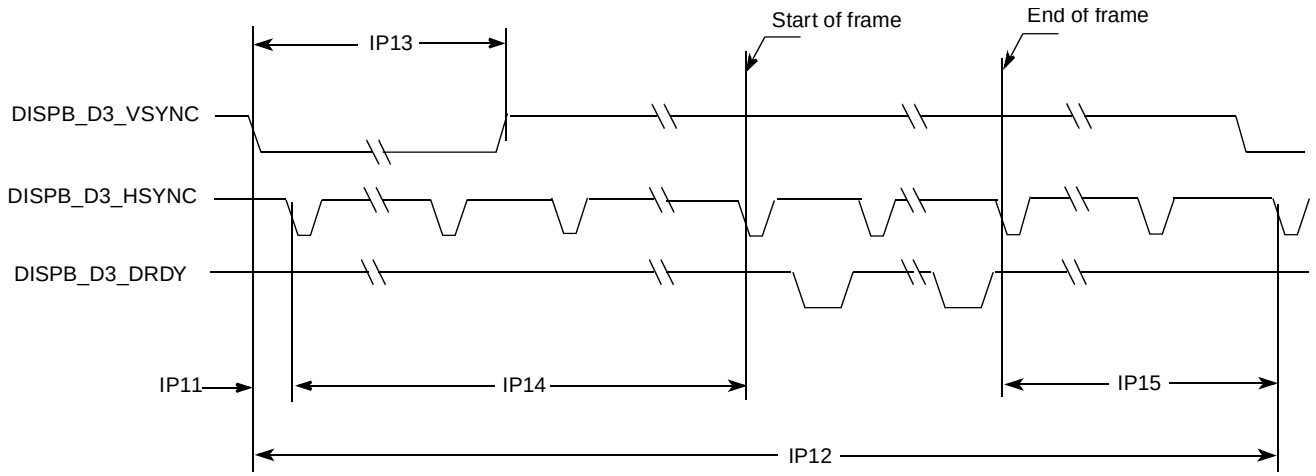


**Figure 47. TFT Panels Timing Diagram—Vertical Sync Pulse**

Table 46 shows timing parameters of signals presented in Figure 46 and Figure 47.

**Table 46. Synchronous Display Interface Timing Parameters—Pixel Level**

| ID | Parameter | Symbol | Value | Units |
|---|---|---|---|---|
| IP5 | Display interface clock period | Tdicp | Tdicp[1] | ns |
| IP6 | Display pixel clock period | Tdpcp | (DISP3_IF_CLK_CNT_D+1) * Tdicp | ns |
| IP7 | Screen width | Tsw | (SCREEN_WIDTH+1) * Tdpcp | ns |
| IP8 | HSYNC width | Thsw | (H_SYNC_WIDTH+1) * Tdpcp | ns |
| IP9 | Horizontal blank interval 1 | Thbi1 | BGXP * Tdpcp | ns |
| IP10 | Horizontal blank interval 2 | Thbi2 | (SCREEN_WIDTH – BGXP – FW) * Tdpcp | ns |
| IP11 | HSYNC delay | Thsd | H_SYNC_DELAY * Tdpcp | ns |
| IP12 | Screen height | Tsh | (SCREEN_HEIGHT+1) * Tsw | ns |
| IP13 | VSYNC width | Tvsw | if V_SYNC_WIDTH_L = 0 than<br>(V_SYNC_WIDTH+1) * Tdpcp<br>else<br>(V_SYNC_WIDTH+1) * Tsw | ns |
| IP14 | Vertical blank interval 1 | Tvbi1 | BGYP * Tsw | ns |
| IP15 | Vertical blank interval 2 | Tvbi2 | (SCREEN_HEIGHT – BGYP – FH) * Tsw | ns |

1 Display interface clock period immediate value.

$$Tdicp = \begin{cases} T_{HSP\_CLK} \cdot \frac{DISP3\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD}, & \text{for integer } \frac{DISP3\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD} \\ T_{HSP\_CLK} \cdot \left( floor\left[ \frac{DISP3\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD} \right] + 0.5 \pm 0.5 \right), & \text{for fractional } \frac{DISP3\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD} \end{cases}$$

Display interface clock period average value.

$$\overline{T}dicp = T_{HSP\_CLK} \cdot \frac{DISP3\_IF\_CLK\_PER\_WR}{HSP\_CLK\_PERIOD}$$

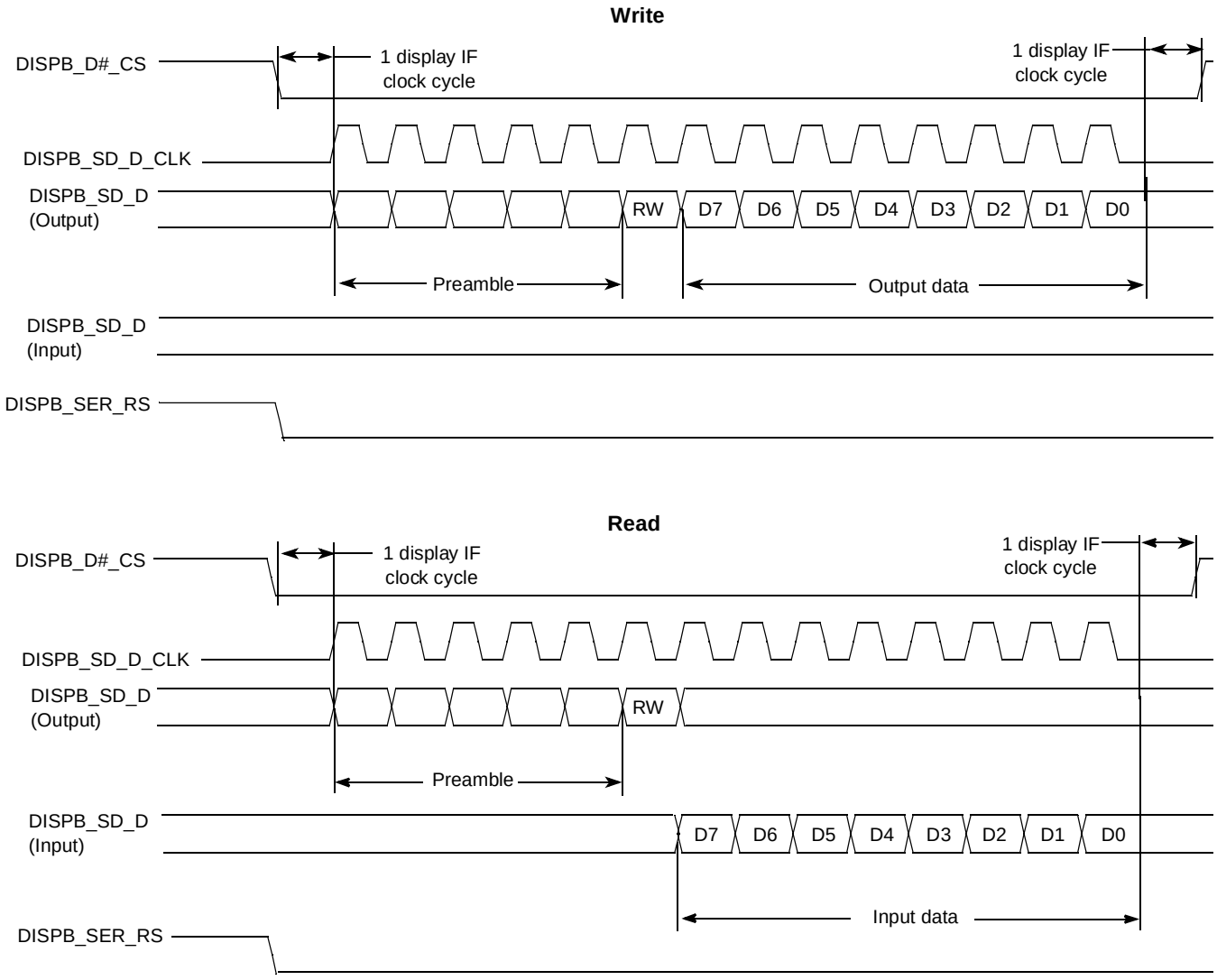


**Figure 62. 5-Wire Serial Interface (Type 1) Timing Diagram**

The DISP#_IF_CLK_PER_WR, DISP#_IF_CLK_PER_RD, HSP_CLK_PERIOD, DISP#_IF_CLK_DOWN_WR, DISP#_IF_CLK_UP_WR, DISP#_IF_CLK_DOWN_RD, DISP#_IF_CLK_UP_RD and DISP#_READ_EN parameters are programmed via the DI_DISP#_TIME_CONF_1, DI_DISP#_TIME_CONF_2 and DI_HSP_CLK_PER Registers.

## 4.3.16 Memory Stick Host Controller (MSHC)

Figure 65, Figure 66, and Figure 67 depict the MSHC timings, and Table 51 and Table 52 list the timing parameters.

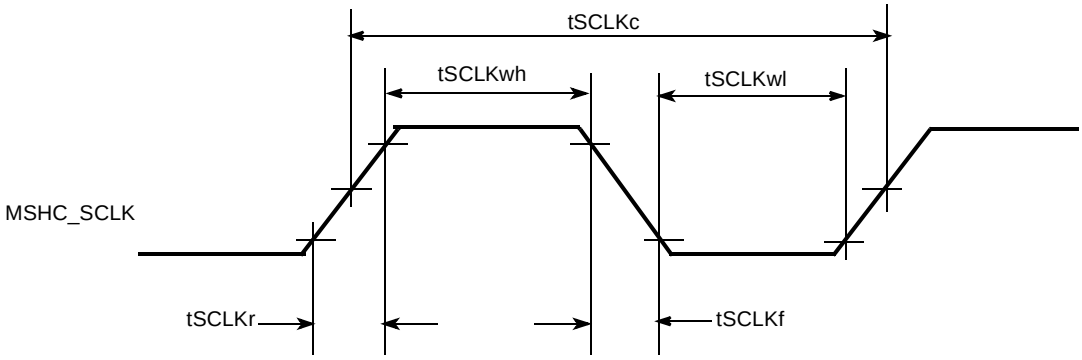


**Figure 65. MSHC_CLK Timing Diagram**

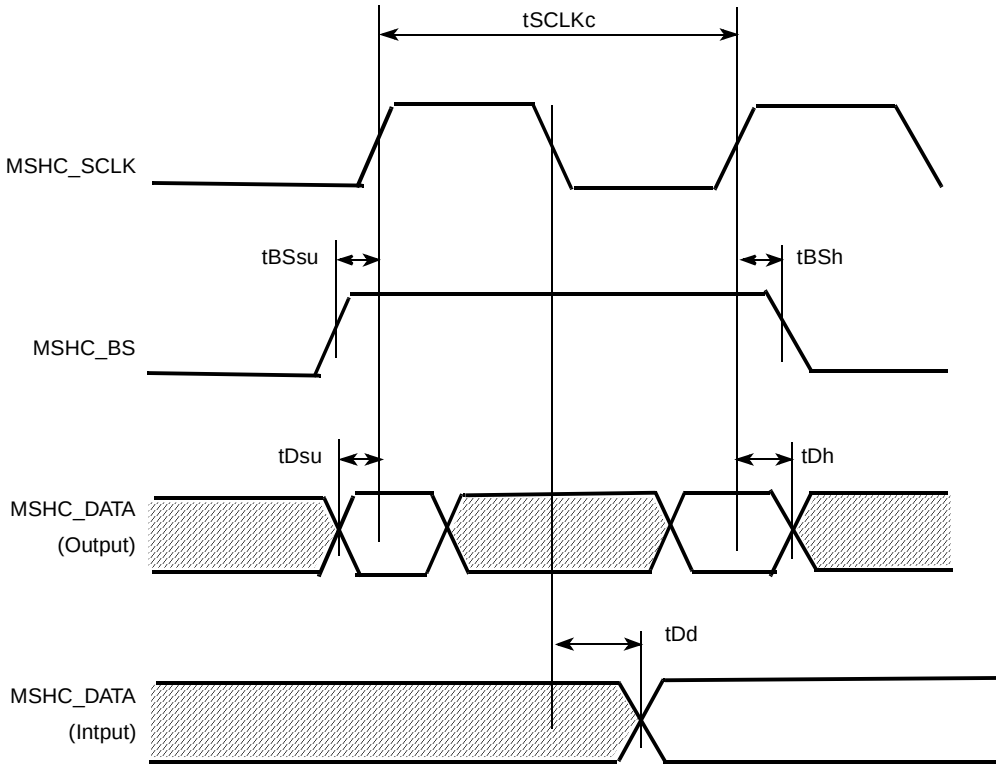


**Figure 66. Transfer Operation Timing Diagram (Serial)**

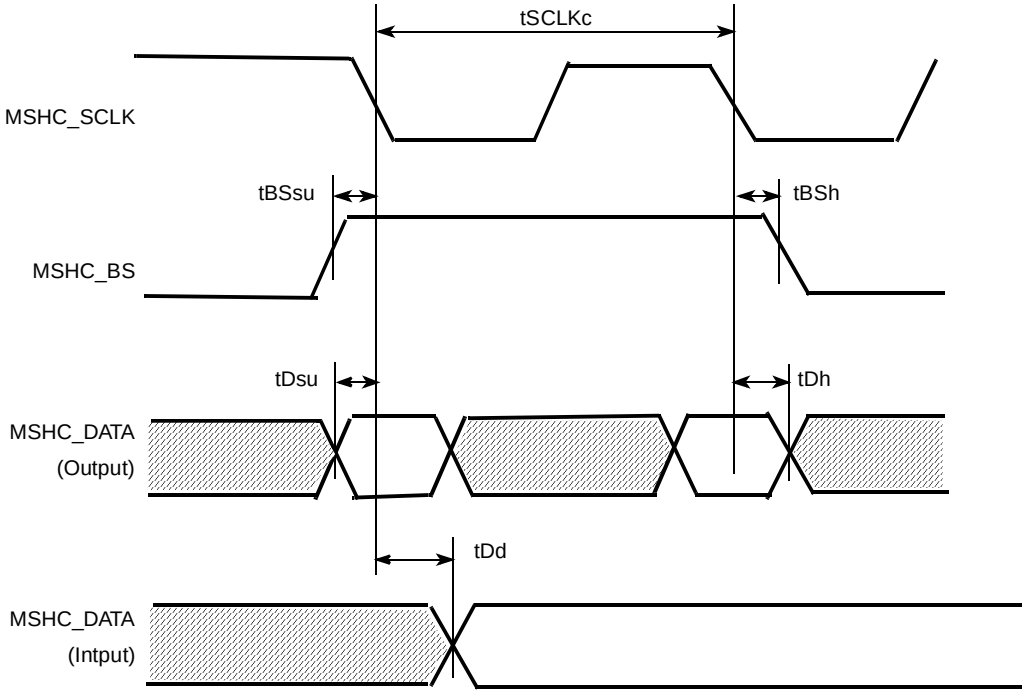


**Figure 67. Transfer Operation Timing Diagram (Parallel)**

## NOTE

The Memory Stick Host Controller is designed to meet the timing requirements per Sony's *Memory Stick Pro Format Specifications* document. Tables in this section details the specifications requirements for parallel and serial modes, and not the MCIMX31 timing.

**Table 51. Serial Interface Timing Parameters[1]**

| Signal | Parameter | Symbol | Standards | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| MSHC_SCLK | Cycle | tSCLKc | 50 | — | ns |
| | H pulse length | tSCLKwh | 15 | — | ns |
| | L pulse length | tSCLKwl | 15 | — | ns |
| | Rise time | tSCLKr | — | 10 | ns |
| | Fall time | tSCLKf | — | 10 | ns |
| MSHC_BS | Setup time | tBSsu | 5 | — | ns |
| | Hold time | tBSh | 5 | — | ns |
| MSHC_DATA | Setup time | tDsu | 5 | — | ns |
| | Hold time | tDh | 5 | — | ns |
| | Output delay time | tDd | — | 15 | ns |

1 Timing is guaranteed for NVCC from 2.7 through 3.1 V and up to a maximum overdrive NVCC of 3.3 V. See NVCC restrictions described in Table 8, "Operating Ranges," on page 13.

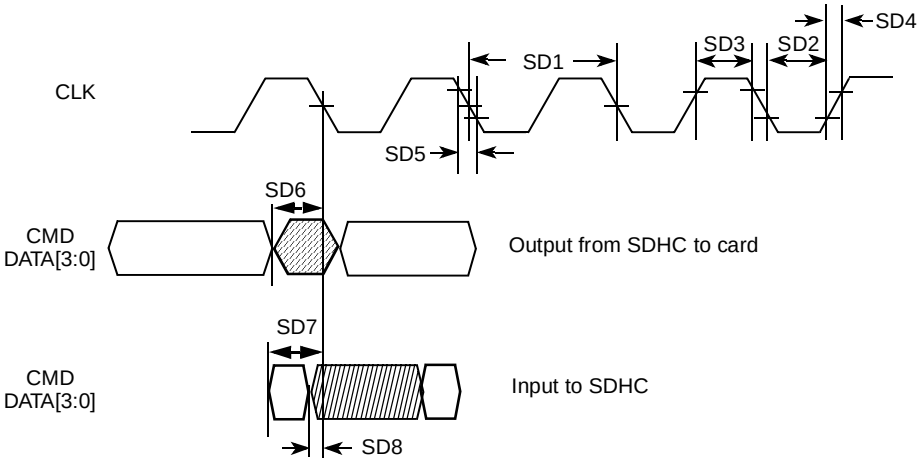


**Figure 71. SDHC Timing Diagram**

**Table 55. SDHC Interface Timing Parameters**

| ID | Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Card Input Clock | | | | | |
| SD1 | Clock Frequency (Low Speed) | $f_{PP}$[1] | 0 | 400 | kHz |
| | Clock Frequency (SD/SDIO Full Speed) | $f_{PP}$[2] | 0 | 25 | MHz |
| | Clock Frequency (MMC Full Speed) | $f_{PP}$[3] | 0 | 20 | MHz |
| | Clock Frequency (Identification Mode) | $f_{OD}$[4] | 100 | 400 | kHz |
| SD2 | Clock Low Time | $t_{WL}$ | 10 | — | ns |
| SD3 | Clock High Time | $t_{WH}$ | 10 | — | ns |
| SD4 | Clock Rise Time | $t_{TLH}$ | — | 10 | ns |
| SD5 | Clock Fall Time | $t_{THL}$ | — | 10 | ns |
| SDHC Output/Card Inputs CMD, DAT (Reference to CLK) | | | | | |
| SD6 | SDHC output delay | $t_{ODL}$ | –6.5 | 3 | ns |
| SDHC Input/Card Outputs CMD, DAT (Reference to CLK) | | | | | |
| SD7 | SDHC input setup | $t_{IS}$ | — | 18.5 | ns |
| SD8 | SDHC input hold | $t_{IH}$ | — | –11.5 | ns |

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 V–3.3 V.

2 In normal data transfer mode for SD/SDIO card, clock frequency can be any value between 0 MHz–25 MHz.

3 In normal data transfer mode for MMC card, clock frequency can be any value between 0 MHz–20 MHz.

4 In card identification mode, card clock must be 100 kHz–400 kHz, voltage ranges from 2.7 V–3.3 V.

## 4.3.20 SIM Electrical Specifications

Each SIM card interface consist of a total of 12 pins (for 2 separate ports of 6 pins each. Mostly one port with 5 pins is used).

### 4.3.20.3 Power Down Sequence

Power down sequence for SIM interface is as follows:

1. SIMPD port detects the removal of the SIM Card
2. RST goes Low
3. CLK goes Low
4. TX goes Low
5. VEN goes Low

Each of this steps is done in one CKIL period (usually 32 kHz). Power down can be started because of a SIM Card removal detection or launched by the processor. Figure 75 and Table 57 show the usual timing requirements for this sequence, with Fckil = CKIL frequency value.

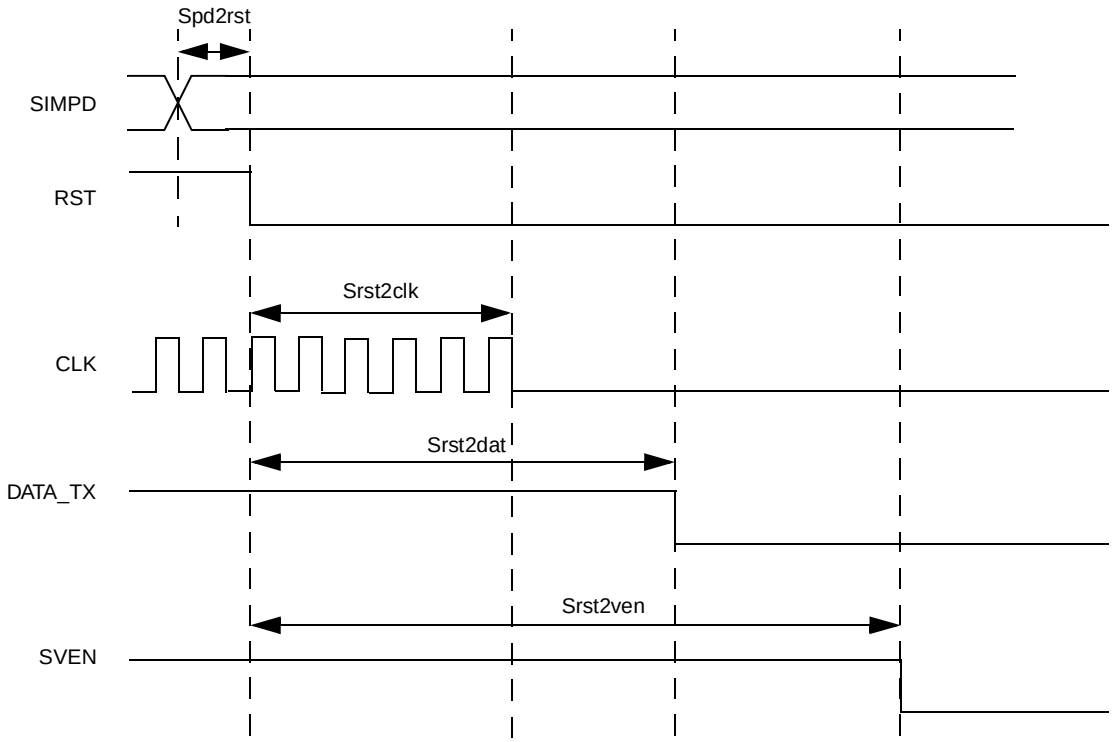


**Figure 75. SmartCard Interface Power Down AC Timing**

**Table 57. Timing Requirements for Power Down Sequence**

| Num | Description | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| 1 | SIM reset to SIM clock stop | $S_{rst2clk}$ | 0.9*1/FCKIL | 0.8 | µs |
| 2 | SIM reset to SIM TX data low | $S_{rst2dat}$ | 1.8*1/FCKIL | 1.2 | µs |
| 3 | SIM reset to SIM Voltage Enable Low | $S_{rst2ven}$ | 2.7*1/FCKIL | 1.8 | µs |
| 4 | SIM Presence Detect to SIM reset Low | $S_{pd2rst}$ | 0.9*1/FCKIL | 25 | ns |

**Table 65. 14 x 14 BGA Signal ID by Ball Grid Location (continued)**

| Signal ID | Ball Location |
|---|---|
| CSPI3_SCLK | E1 |
| CSPI3_SPI_RDY | G6 |
| CTS1 | B11 |
| CTS2 | G13 |
| D0 | AB2 |
| D1 | Y3 |
| D10 | Y1 |
| D11 | U7 |
| D12 | W2 |
| D13 | V3 |
| D14 | W1 |
| D15 | U6 |
| D2 | AB1 |
| D3 | W6 |
| D3_CLS | R20 |
| D3_REV | T26 |
| D3_SPL | U25 |
| D4 | AA2 |
| D5 | V7 |
| D6 | AA1 |
| D7 | W3 |
| D8 | Y2 |
| D9 | V6 |
| DCD_DCE1 | B12 |
| DCD_DTE1 | B13 |
| $\overline{DE}$ | C18 |
| DQM0 | AE19 |
| DQM1 | AD19 |
| DQM2 | AA20 |
| DQM3 | AE18 |
| DRDY0 | N26 |
| DSR_DCE1 | A11 |
| DSR_DTE1 | A12 |
| DTR_DCE1 | C11 |
| DTR_DCE2 | F12 |
| DTR_DTE1 | C12 |
| DVFS0 | E25 |
| DVFS1 | G24 |
| EB0 | W21 |
| EB1 | Y24 |
| ECB | AD23 |
| FPSHIFT | N21 |
| GPIO1_0 | F18 |
| GPIO1_1 | B23 |
| GPIO1_2 | C20 |
| LD7 | W25 |

| Signal ID | Ball Location |
|---|---|
| GPIO1_3 | F25 |
| GPIO1_4 | F19 |
| GPIO1_5 (PWR RDY) | B24 |
| GPIO1_6 | A23 |
| GPIO3_0 | K21 |
| GPIO3_1 | H26 |
| HSYNC | N25 |
| I2C_CLK | J24 |
| I2C_DAT | H25 |
| IOIS16 | J3 |
| KEY_COL0 | C15 |
| KEY_COL1 | B17 |
| KEY_COL2 | G15 |
| KEY_COL3 | A17 |
| KEY_COL4 | C16 |
| KEY_COL5 | B18 |
| KEY_COL6 | F15 |
| KEY_COL7 | A18 |
| KEY_ROW0 | F13 |
| KEY_ROW1 | B15 |
| KEY_ROW2 | C14 |
| KEY_ROW3 | A15 |
| KEY_ROW4 | G14 |
| KEY_ROW5 | B16 |
| KEY_ROW6 | F14 |
| KEY_ROW7 | A16 |
| L2PG | See VPG1 |
| LBA | AE22 |
| LCS0 | P26 |
| LCS1 | P21 |
| LD0 | T24 |
| LD1 | U26 |
| LD10 | V24 |
| LD11 | Y25 |
| LD12 | Y26 |
| LD13 | V21 |
| LD14 | AA25 |
| LD15 | W24 |
| LD16 | AA26 |
| LD17 | V20 |
| LD2 | T21 |
| LD3 | V25 |
| LD4 | T20 |
| LD5 | V26 |
| LD6 | U24 |
| SCK6 | T2 |

## 5.2.2 MAPBGA Signal Assignment–19 × 19 mm 0.8 mm

See Table 70 for the 19 × 19 mm, 0.8 mm pitch signal assignments/ball map.

## 5.2.3 Connection Tables–19 x 19 mm 0.8 mm

Table 66 shows the device connection list for power and ground, alpha-sorted followed by Table 67, which shows the no-connects. Table 68 shows the device connection list for signals.

### 5.2.3.1 Ground and Power ID Locations—19 x 19 mm 0.8 mm

**Table 66. 19 x 19 BGA Ground/Power ID by Ball Grid Location**

| GND/PWR ID | Ball Location |
|---|---|
| FGND | U16 |
| FUSE_VDD | T15 |
| FVCC | T16 |
| GND | A1, A2, A3, A21, A22, A23, B1, B2, B22, B23, C1, C2, C22, C23, D22, D23, J12, J13, K10, K11, K12, K13, K14, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N10, N11, N12, N13, N14, P10, P11, P12, P13, P14, R12, Y1, Y23, AA1, AA2, AA22, AA23, AB1, AB2, AB21, AB22, AB23, AC1, AC2, AC21, AC22, AC23 |
| IOQVDD | T8 |
| MGND | U14 |
| MVCC | U15 |
| NVCC1 | G15, G16, H16, J17 |
| NVCC2 | N16, P16, R15, R16, T14 |
| NVCC3 | K7, K8, L7, L8 |
| NVCC4 | H14, J15, K15 |
| NVCC5 | G9, G10, H8, H9 |
| NVCC6 | G11, G12, G13, H12 |
| NVCC7 | H15, J16, K16, L16, M16 |
| NVCC8 | H10, H11, J11 |
| NVCC9 | G14 |
| NVCC10 | P8, R7, R8, R9, T9 |
| NVCC21 | T11, T12, T13, U11 |
| NVCC22 | T10, U7, U8, U9, U10, V6, V7, V8, V9, V10 |
| QVCC | H13, J14, L15, M15, N9, N15, P9, P15, R10, R11, R13, R14 |
| QVCC1 | J8, J9, J10, K9 |
| QVCC4 | L9, M7, M8, N8 |
| SGND | U13 |
| SVCC | U12 |
| UVCC | P18 |
| UGND | P17 |

**Table 68. 19 x 19 BGA Signal ID by Ball Grid Location (continued)**

| Signal ID | Ball Location |
|---|---|
| DVFS1 | E23 |
| EB0 | W22 |
| EB1 | W21 |
| ECB | Y21 |
| FPSHIFT | M23 |
| GPIO1_0 | C19 |
| GPIO1_1 | G17 |
| GPIO1_2 | B20 |
| LD7 | T20 |
| LD8 | R17 |
| LD9 | U23 |
| M_GRANT | U18 |
| M_REQUEST | T17 |
| MA10 | Y2 |
| MCUPG | See VPG0 |
| NFALE | T2 |
| $\overline{\text{NFCE}}$ | R4 |
| NFCLE | T1 |
| NFRB | R3 |
| $\overline{\text{NFRE}}$ | T4 |
| $\overline{\text{NFWE}}$ | T3 |
| $\overline{\text{NFWP}}$ | P6 |
| OE | T18 |
| PAR_RS | P22 |
| PC_BVD1 | G2 |
| PC_BVD2 | H4 |
| $\overline{\text{PC\_CD1}}$ | J3 |
| $\overline{\text{PC\_CD2}}$ | H1 |
| PC_POE | J6 |
| PC_PWRON | K6 |
| PC_READY | H2 |
| PC_RST | F1 |
| $\overline{\text{PC\_RW}}$ | G3 |
| PC_VS1 | H3 |
| PC_VS2 | G1 |
| $\overline{\text{PC\_WAIT}}$ | J4 |
| $\overline{\text{POR}}$ | F21 |
| POWER_FAIL | F20 |
| PWMO | F2 |
| RAS | AA19 |
| READ | N18 |
| $\overline{\text{RESET\_IN}}$ | F22 |
| RI_DCE1 | D10 |
| RI_DTE1 | B11 |
| RTCK | D15 |
| RTS1 | B9 |

| Signal ID | Ball Location |
|---|---|
| LD15 | V21 |
| LD16 | V20 |
| LD17 | W23 |
| LD2 | R21 |
| LD3 | R20 |
| LD4 | T23 |
| LD5 | T22 |
| LD6 | T21 |
| SCK6 | R2 |
| SCLK0 | B19 |
| SD_D_CLK | M21 |
| SD_D_I | M20 |
| SD_D_IO | M18 |
| SD0 | AC18 |
| SD1 | AA17 |
| SD1_CLK | K2 |
| SD1_CMD | K3 |
| SD1_DATA0 | K4 |
| SD1_DATA1 | J1 |
| SD1_DATA2 | J2 |
| SD1_DATA3 | L6 |
| SD10 | AB14 |
| SD11 | AC14 |
| SD12 | AA13 |
| SD13 | AB13 |
| SD14 | AC13 |
| SD15 | AA12 |
| SD16 | AC12 |
| SD17 | AA11 |
| SD18 | AB11 |
| SD19 | AC11 |
| SD2 | AB17 |
| SD20 | AA10 |
| SD21 | AB10 |
| SD22 | AC10 |
| SD23 | AC9 |
| SD24 | AA9 |
| SD25 | AC8 |
| SD26 | AB8 |
| SD27 | AC7 |
| SD28 | AA8 |
| SD29 | AB7 |
| SD3 | AC17 |
| SD30 | AA7 |
| SD31 | AC6 |
| SD4 | AA16 |

**Table 68. 19 x 19 BGA Signal ID by Ball Grid Location (continued)**

| Signal ID | Ball Location |
|---|---|
| RTS2 | B12 |
| RW | V18 |
| RXD1 | C9 |
| RXD2 | A12 |
| SCK3 | P1 |
| SCK4 | G6 |
| SCK5 | D4 |
| SDCKE0 | Y17 |
| SDCKE1 | V16 |
| SDCLK | AC20 |
| $\overline{\text{SDCLK}}$ | AC19 |
| SDQS0 | AB16 |
| SDQS1 | AB12 |
| SDQS2 | AB9 |
| SDQS3 | AB6 |
| SDWE | AB20 |
| SER_RS | P23 |
| SFS3 | P2 |
| SFS4 | D3 |
| SFS5 | G7 |
| SFS6 | P4 |
| SIMPD0 | B18 |
| SJC_MOD | C17 |
| SRST0 | C18 |
| SRX0 | A19 |
| SRXD3 | N3 |
| SRXD4 | C3 |
| SRXD5 | C4 |
| SRXD6 | R1 |
| STX0 | F16 |
| STXD3 | N4 |
| STXD4 | B3 |
| STXD5 | D1 |
| STXD6 | P3 |
| SVEN0 | D17 |
| TCK | F14 |
| TDI | A18 |
| TDO | B17 |
| TMS | C16 |

| Signal ID | Ball Location |
|---|---|
| SD5 | AC16 |
| SD6 | AA15 |
| SD7 | AB15 |
| SD8 | AC15 |
| SD9 | AA14 |
| SDBA0 | AA6 |
| SDBA1 | Y7 |
| TRSTB | F15 |
| TXD1 | D9 |
| TXD2 | F11 |
| USB_BYP | C8 |
| USB_OC | B8 |
| USB_PWR | A8 |
| USBH2_CLK | L1 |
| USBH2_DATA0 | M6 |
| USBH2_DATA1 | K1 |
| USBH2_DIR | L2 |
| USBH2_NXT | L4 |
| USBH2_STP | L3 |
| USBOTG_CLK | D8 |
| USBOTG_DATA0 | G8 |
| USBOTG_DATA1 | C7 |
| USBOTG_DATA2 | A6 |
| USBOTG_DATA3 | F8 |
| USBOTG_DATA4 | D7 |
| USBOTG_DATA5 | B6 |
| USBOTG_DATA6 | A5 |
| USBOTG_DATA7 | C6 |
| USBOTG_DIR | A7 |
| USBOTG_NXT | B7 |
| USBOTG_STP | F9 |
| VPG0 | G21 |
| VPG1 | G22 |
| VSTBY | H18 |
| VSYNC0 | L22 |
| VSYNC3 | N20 |
| WATCHDOG_RST | B21 |
| WRITE | N22 |
| | |

# 5.3 Ball Maps

**Table 69. Ball Map—14 x 14 0.5 mm Pitch**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | GND | GND | SFS5 | CSPI2_MISO | CSPI2_SS2 | USBOTG_DATA7 | USBOTG_DATA3 | USBOTG_NXT | USB_BYP | RXD1 | DSR_DCE1 | DSR_DTE1 | RXD2 | CE_CONTROL | KEY_ROW3 | KEY_ROW7 | KEY_COL3 | KEY_COL7 | TDO | SJC_MOD | SVEN0 | CAPTURE | GPIO1_6 | WATCHDOG_RST | GND | GND | A |
| B | GND | GND | STXD4 | SRXD5 | CSPI2_SS0 | CSPI2_SPI_RDY | USBOTG_DATA5 | USBOTG_DATA1 | USBOTG_DIR | USB_PWR | CTS1 | DCD_DCE1 | DCD_DTE1 | RTS2 | KEY_ROW1 | KEY_ROW5 | KEY_COL1 | KEY_COL5 | TCK | TRSTB | SRX0 | SCLK0 | GPIO1_1 | GPIO1_5 | GND | GND | B |
| C | GND | GND | SRXD4 | SCK4 | STXD5 | CSPI2_SS1 | CSPI2_SCLK | USBOTG_DATA4 | USBOTG_STP | USB_OC | DTR_DCE1 | DTR_DTE1 | TXD2 | KEY_ROW2 | KEY_COL0 | KEY_COL4 | RTCK | DE | SRST0 | GPIO1_2 | BOOT_MODE1 | BOOT_MODE3 | CLKO | GND | GND | GND | C |
| D | GND | CSPI3_MOSI | SCK5 | | | | | | | | | | | | | | | | | | | | | BOOT_MODE2 | GND | BOOT_MODE4 | D |
| E | CSPI3_SCLK | ATA_DIOR | CSPI2_MOSI | | NVCC5 | | | | | | | | | | | | | | | | | GND | | GND | DVFS0 | POWER_FAIL | E |
| F | ATA_DMACK | ATA_CS1 | SFS4 | | | NVCC5 | BATT_LINE | USBOTG_DATA6 | USBOTG_DATA0 | TXD1 | RI_DCE1 | DTR_DCE2 | KEY_ROW0 | KEY_ROW6 | KEY_COL6 | TDI | STX0 | GPIO1_0 | GPIO1_4 | BOOT_MODE0 | GND | | | CKIH | GPIO1_3 | VSTBY | F |
| G | PWMO | PC_RW | CSPI3_MISO | | | CSPI3_SPI_RDY | NVCC5 | | USBOTG_DATA2 | USBOTG_CLK | RTS1 | RI_DTE1 | CTS2 | KEY_ROW4 | KEY_COL2 | TMS | SIMPD0 | COMPARE | NVCC1 | | NVCC1 | | | DVFS1 | VPG0 | CLKSS | G |
| H | PC_RST | PC_BVD1 | ATA_RESET | | | ATA_DIOW | | | | | | | | | | | | | | | CKIL | | | POR | I2C_DAT | GPIO3_1 | H |
| J | PC_VS1 | PC_READY | IOIS16 | | | ATA_CS0 | PC_POE | | | QVCC1 | QVCC1 | NVCC8 | NVCC8 | QVCC | NVCC6 | NVCC6 | NVCC9 | | | VPG1 | RESET_IN | | | I2C_CLK | CSI_VSYNC | CSI_PIXCLK | J |
| K | PC_CD2 | SD1_DATA3 | PC_PWRON | | | PC_BVD2 | PC_VS2 | | QVCC1 | | | | | | NVCC6 | | | NVCC1 | | CSI_HSYNC | GPIO3_0 | | | CSI_MCLK | CSI_D5 | CSI_D7 | K |
| L | SD1_DATA1 | SD1_CMD | SD1_DATA2 | | | PC_WAIT | PC_CD1 | | NVCC3 | | QVCC1 | GND | QVCC | QVCC | QVCC | QVCC | | NVCC4 | NVCC4 | CSI_D8 | CSI_D4 | | | CSI_D6 | CSI_D9 | CSI_D11 | L |
| M | USBH2_DATA0 | USBH2_STP | USBH2_DATA1 | | | SD1_DATA0 | SD1_CLK | | NVCC3 | | GND | GND | GND | GND | GND | GND | | QVCC | | CSI_D14 | CSI_D12 | | | CSI_D10 | CSI_D13 | CSI_D15 | M |
| N | USBH2_CLK | CSPI1_SCLK | CSPI1_SPI_RDY | | | USBH2_NXT | USBH2_DIR | | QVCC4 | | NVCC3 | GND | GND | GND | GND | GND | | NVCC7 | | SD_D_I | FPSHIFT | | | VSYNC0 | HSYNC | DRDY0 | N |
| P | CSPI1_SS1 | CSPI1_MOSI | CSPI1_SS0 | | | CSPI1_SS2 | CSPI1_MISO | | NVCC10 | | NVCC10 | GND | GND | GND | GND | GND | | NVCC7 | | READ | LCS1 | | | SD_D_CLK | SD_D_IO | LCS0 | P |
| R | STXD3 | SCK3 | SRXD3 | | | SFS3 | SRXD6 | | QVCC4 | | NVCC10 | GND | GND | GND | GND | GND | | NVCC7 | | D3_CLS | PAR_RS | | | CONTRAST | WRITE | VSYNC3 | R |
| T | STXD6 | SCK6 | SFS6 | | | NFCE | NFWE | | QVCC4 | | NVCC10 | GND | GND | SGND | MGND | UGND | | NVCC7 | | LD4 | LD2 | | | LD0 | SER_RS | D3_REV | T |
| U | NFRB | NFWP | NFCLE | | | D15 | D11 | | QVCC4 | | | | | | | | | QVCC | | TTM_PAD | LD8 | | | LD6 | D3_SPL | LD1 | U |
| V | NFALE | NFRE | D13 | | | D9 | D5 | | | QVCC | QVCC | QVCC | QVCC | SVCC | MVCC | UVCC | GND | | | LD17 | LD13 | | | LD10 | LD3 | LD5 | V |
| W | D14 | D12 | D7 | | | D3 | NVCC22 | | | | | | | | | | | | | | EB0 | | | LD15 | LD7 | LD9 | W |
| Y | D10 | D8 | D1 | | | IOQVDD | NVCC22 | NVCC22 | NVCC22 | NVCC22 | NVCC22 | NVCC22 | NVCC22 | NVCC21 | NVCC21 | NVCC21 | NVCC2 | NVCC2 | NVCC2 | NVCC2 | M_GRANT | | | EB1 | LD11 | LD12 | Y |
| AA | D6 | D4 | A4 | | | NVCC22 | SD31 | SD28 | SD27 | SD23 | SD21 | SD18 | SD16 | SD13 | SD9 | SD7 | SD5 | SD3 | SD2 | DQM2 | SDCLK | | | FVCC | LD14 | LD16 | AA |
| AB | D2 | D0 | A6 | | A2 | | | | | | | | | | | | | | | | | RW | | FGND | OE | BCLK | AB |
| AC | MA10 | GND | A11 | | | | | | | | | | | | | | | | | | | | | FUSE_VDD | M_REQUEST | GND | AC |
| AD | GND | GND | A12 | A13 | A8 | A0 | SDBA0 | SDQS3 | SD29 | SD25 | SDQS2 | SD17 | SD15 | SD12 | SD8 | SDQS0 | SD4 | SD0 | DQM1 | CAS | SDCKE0 | CS3 | ECB | GND | GND | GND | AD |
| AE | GND | GND | A7 | A3 | SDBA1 | SD30 | SD26 | SD24 | SD22 | SD20 | SD19 | SDQS1 | SD14 | SD11 | SD10 | SD6 | SD1 | DQM3 | DQM0 | SDCLK | CS2 | LBA | CS0 | GND | GND | GND | AE |
| AF | GND | GND | A9 | A5 | A1 | A25 | A24 | A23 | A22 | A21 | A20 | A19 | A18 | A17 | A16 | A15 | A14 | A10 | RAS | SDWE | SDCKE1 | CS5 | CS1 | CS4 | GND | GND | AF |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | |