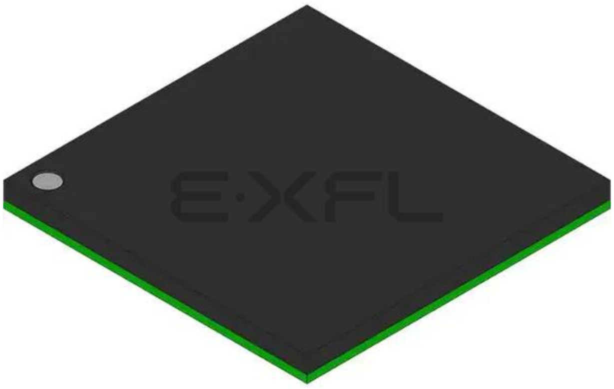

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM1136JF-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	532MHz
Co-Processors/DSP	Multimedia; GPU, IPU, MPEG-4, VFP
RAM Controllers	DDR
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, Keypad, LCD
Ethernet	-
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.0V, 2.5V, 2.7V, 3.0V
Operating Temperature	-20°C ~ 70°C (TA)
Security Features	Random Number Generator, RTIC, Secure Fusebox, Secure JTAG, Secure Memory
Package / Case	457-LFBGA
Supplier Device Package	457-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx31ldvkn5dr2

such as an MPEG-4 Hardware Encoder (VGA, 30 fps), an Autonomous Image Processing Unit, a Vector Floating Point (VFP11) co-processor, and a RISC-based SDMA controller.

The MCIMX31 supports connections to various types of external memories, such as DDR, NAND Flash, NOR Flash, SDRAM, and SRAM. The MCIMX31 can be connected to a variety of external devices using technology, such as high-speed USB2.0 OTG, ATA, MMC/SDIO, and compact flash.

1.1 Features

The MCIMX31 is designed for the high-tier, mid-tier smartphone markets, and portable media players. They provide low-power solutions for high-performance demanding multimedia and graphics applications.

The MCIMX31 is built around the ARM11 MCU core and implemented in the 90 nm technology.

The systems include the following features:

- Multimedia and floating-point hardware acceleration supporting:
  - MPEG-4 real-time encode of up to VGA at 30 fps
  - MPEG-4 real-time video post-processing of up to VGA at 30 fps
  - Video conference call of up to QCIF-30 fps (decoder in software), 128 kbps
  - Video streaming (playback) of up to VGA-30 fps, 384 kbps
  - 3D graphics and other applications acceleration with the ARM® tightly-coupled Vector Floating Point co-processor
  - On-the-fly video processing that reduces system memory load (for example, the power-efficient viewfinder application with no involvement of either the memory system or the ARM CPU)
- Advanced power management
  - Dynamic voltage and frequency scaling
  - Multiple clock and power domains
  - Independent gating of power domains
- Multiple communication and expansion ports including a fast parallel interface to an external graphic accelerator (supporting major graphic accelerator vendors)
- Security

1.3 Block Diagram

Figure 1 shows the MCIMX31 simplified interface block diagram.

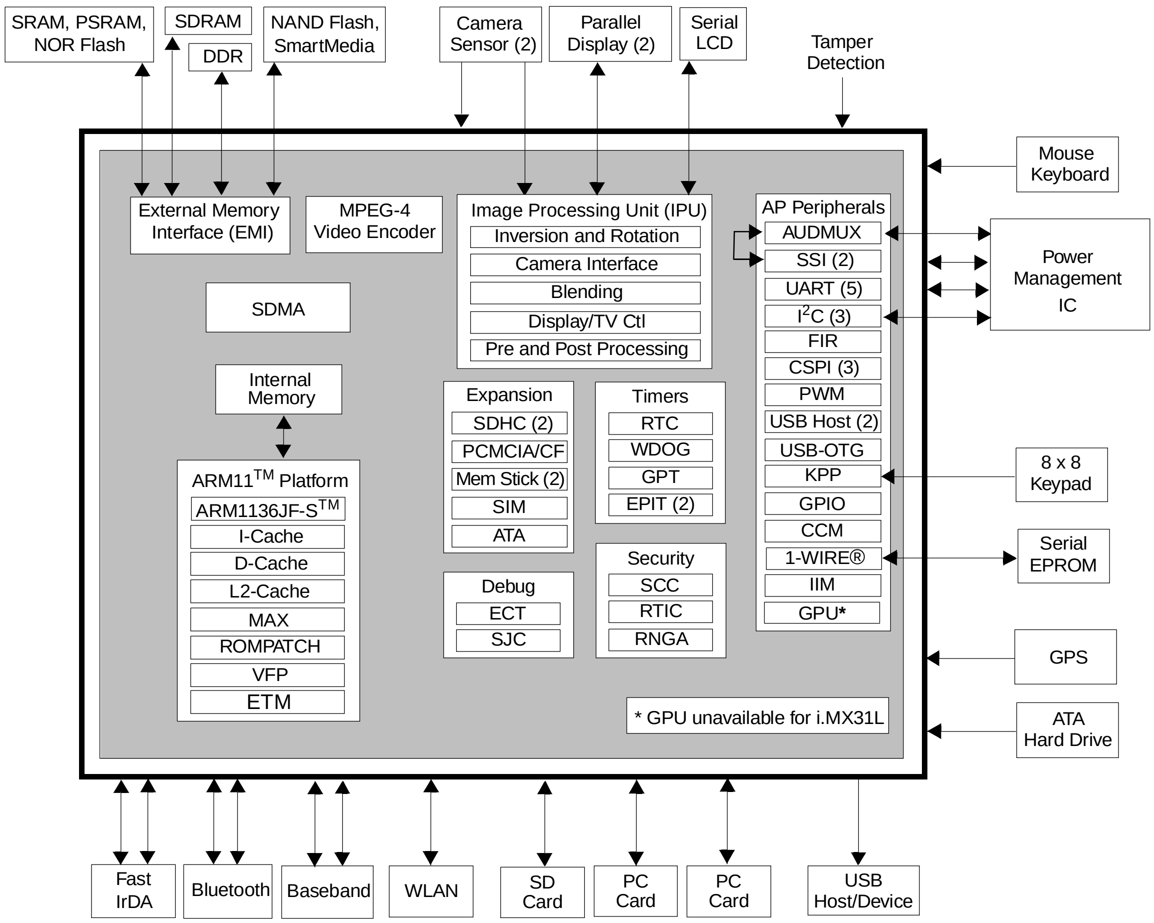

Figure 1. MCIMX31 Simplified Interface Block Diagram

2 Functional Description and Application Information

2.1 ARM11 Microprocessor Core

The CPU of the MCIMX31 is the ARM1136JF-S core based on the ARM v6 architecture. It supports the ARM Thumb® instruction sets, features Jazelle® technology (which enables direct execution of Java byte codes), and a range of SIMD DSP instructions that operate on 16-bit or 8-bit data values in 32-bit registers.

The ARM1136JF-S processor core features:

- Integer unit with integral EmbeddedICE™ logic
- Eight-stage pipeline
- Branch prediction with return stack
- Low-interrupt latency

Table 8 provides the operating ranges.

NOTE

The term NVCC in this section refers to the associated supply rail of an input or output. The association is shown in the Signal Multiplexing chapter of the reference manual.

CAUTION

NVCC6 and NVCC9 must be at the same voltage potential. These supplies are connected together on-chip to optimize ESD damage immunity.

Table 8. Operating Ranges

Symbol	Parameter	Min	Max	Units
QVCC, QVCC1, QVCC4	Core Operating Voltage[1,2,3] $0 \leq f_{ARM} \leq 400$ MHz, non-overdrive $0 \leq f_{ARM} \leq 532$ MHz, non-overdrive $0 \leq f_{ARM} \leq 532$ MHz, overdrive[4]	 1.22 1.38 1.52	 1.47 1.52 1.65	V
	State Retention Voltage[5]	0.95	—	
NVCC1, NVCC3–10	I/O Supply Voltage, except DDR[6]non-overdrive overdrive[7]	1.75 >3.1	3.1 3.3	V
NVCC2, NVCC21, NVCC22	I/O Supply Voltage, DDR only	1.75	1.95	V
FVCC, MVCC, SVCC, UVCC	PLL (Phase-Locked Loop) and FPM (Frequency Pre-multiplier) Supply Voltage[8] non-overdrive overdrive[4]	 1.3 >1.47	 1.47 1.6	V
IOQVDD	On-device Level Shifter Supply Voltage	1.6	1.9	V
FUSE_VDD	Fusebox read Supply Voltage[9, 10]	1.65	1.95	V
	Fusebox write (program) Supply Voltage[11]	3.0	3.3	V
T_A	Operating Ambient Temperature Range[12]	–20	70	^oC

1 Measured at package balls, including peripherals, ARM, and L2 cache supplies (QVCC, QVCC1, QVCC4, respectively).

2 The core voltage must be higher than 1.38V to avoid corrupted data during transfers from the USB HS. Please refer to Errata file ENGcm02610 ID.

3 If the Core voltage is supplied by the MC13738, it will be 1.6 ± 0.05 V during the power-up sequence and this is allowed. After power-up the voltage should be reduced to avoid operation in overdrive mode.

4 Supply voltage is considered “overdrive” for voltages above 1.52 V. Operation time in overdrive—whether switching or not—must be limited to a cumulative duration of 1.25 years (10,950 hours) or less to sustain the maximum operating voltage without significant device degradation—for example, 25% (average 6 hours out of 24 yours per day) duty cycle for 5-year rated equipment. To tolerate the maximum operating overdrive voltage for 10 years, the device must have a duty cycle of 12.5% or less in overdrive (for example 3 out of 24 hours per day). Below 1.52 V, duty cycle restrictions may apply for equipment rated above 5 years.

5 The SR voltage is applied to QVCC, QVCC1, and QVCC4 after the device is placed in SR mode. The Real-Time Clock (RTC) is operational in State Retention (SR) mode**.**

6 Overshoot and undershoot conditions (transitions above NVCC and below GND) on I/O must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

7 Supply voltage is considered "overdrive" for voltages above 3.1 V. Operation time in overdrive—whether switching or not—must be limited to a cumulative duration of 1 year (8,760 hours) or less to sustain the maximum operating voltage without significant device degradation—for example, 20% (average 4.8 hours out of 24 hours per day) duty cycle for 5-year rated equipment. Operation at 3.3 V that exceeds a cumulative 3,504 hours may cause non-operation whenever supply voltage is reduced to 1.8 V; degradation may render the device too slow or inoperable. Below 3.1 V, duty cycle restrictions may apply for equipment rated above 5 years.

8 For normal operating conditions, PLLs' and core supplies must maintain the following relation: PLL ≥ Core – 100 mV. In other words, for a 1.6 V core supply, PLL supplies must be set to 1.5 V or higher. This restriction is no longer necessary on mask set M91E. PLL supplies may be set independently of core supply. PLL voltage must not be altered after power up, otherwise the PLL will be unstable and lose lock. To minimize inducing noise on the PLL supply line, source the voltage from a low-noise, dedicated supply. PLL parameters in Table 30, "DPLL Specifications," on page 35, are guaranteed over the entire specified voltage range.

9 Fusebox read supply voltage applies to silicon Revisions 1.2 and previous.

10 In read mode, FUSE_VDD can be floated or grounded for mask set M91E (silicon Revision 2.0.1).

11 Fuses might be inadvertently blown if written to while the voltage is below this minimum.

12 The temperature range given is for the consumer version. Please refer to Table 1 for extended temperature range offerings and the associated part numbers.

Table 9. Specific Operating Ranges for Silicon Revision 2.0.1

Symbol	Parameter	Min	Max	Units
FUSE_VDD	Fusebox read Supply Voltage[1]	—	—	V
	Fusebox write (program) Supply Voltage[2]	3.0	3.3	V

1 In read mode, FUSE_VDD should be floated or grounded.

2 Fuses might be inadvertently blown if written to while the voltage is below the minimum.

Table 10 provides information for interface frequency limits. For more details about clocks characteristics, see Section 4.3.8, "DPLL Electrical Specifications," and Section 4.3.3, "Clock Amplifier Module (CAMP) Electrical Characteristics."

Table 10. Interface Frequency

ID	Parameter	Symbol	Min	Typ	Max	Units
1	JTAG TCK Frequency	f_{JTAG}	DC	5	10	MHz
2	CKIL Frequency[1]	f_{CKIL}	32	32.768	38.4	kHz
3	CKIH Frequency[2]	f_{CKIH}	15	26	75	MHz

1 CKIL must be driven by an external clock source to ensure proper start-up and operation of the device. CKIL is needed to clock the internal reset synchronizer, the watchdog, and the real-time clock.

2 DPTC functionality, specifically the voltage/frequency relation table, is dependent on CKIH frequency. At the time of publication, standard tables used by Freescale OSs provided for a CKIH frequency of 26 MHz only. Any deviation from this frequency requires an update to the OS. For more details, refer to the particular OS user's guide documentation.

Table 11 shows the fusebox supply current parameters.

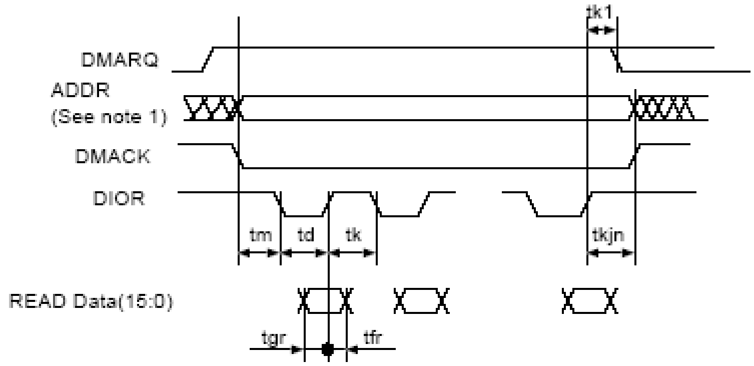

Figure 12. MDMA Read Timing Diagram

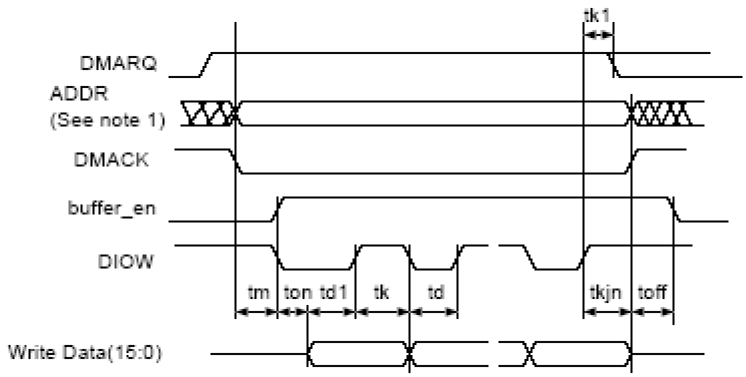

Figure 13. MDMA Write Timing Diagram

Table 26. MDMA Read and Write Timing Parameters

ATA Parameter	Parameter from Figure 12, Figure 13	Value	Controlling Variable
tm, ti	tm	tm (min) = ti (min) = time_m * T – (tskew1 + tskew2 + tskew5)	time_m
td	td, td1	td1.(min) = td (min) = time_d * T – (tskew1 + tskew2 + tskew6)	time_d
tk	tk	tk.(min) = time_k * T – (tskew1 + tskew2 + tskew6)	time_k
t0	—	t0 (min) = (time_d + time_k) * T	time_d, time_k
tg(read)	tgr	tgr (min-read) = tco + tsu + tbuf + tbuf + tcable1 + tcable2 tgr.(min-drive) = td – te(drive)	time_d
tf(read)	tfr	tfr (min-drive) = 0	—
tg(write)	—	tg (min-write) = time_d * T – (tskew1 + tskew2 + tskew5)	time_d
tf(write)	—	tf (min-write) = time_k * T – (tskew1 + tskew2 + tskew6)	time_k
tL	—	tL (max) = (time_d + time_k–2)*T – (tsu + tco + 2*tbuf + 2*tcable2)	time_d, time_k
tn, tj	tkjn	tn= tj= tkjn = (max(time_k,. time_jn) * T – (tskew1 + tskew2 + tskew6)	time_jn
—	ton toff	ton = time_on * T – tskew1 toff = time_off * T – tskew1	—

4.3.6 AUDMUX Electrical Specifications

The AUDMUX provides a programmable interconnect logic for voice, audio and data routing between internal serial interfaces (SSI) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is hence governed by the SSI module. Please refer to their respective electrical specifications.

4.3.7 CSPI Electrical Specifications

This section describes the electrical information of the CSPI.

4.3.7.1 CSPI Timing

Figure 20 and Figure 21 depict the master mode and slave mode timings of CSPI, and Table 29 lists the timing parameters.

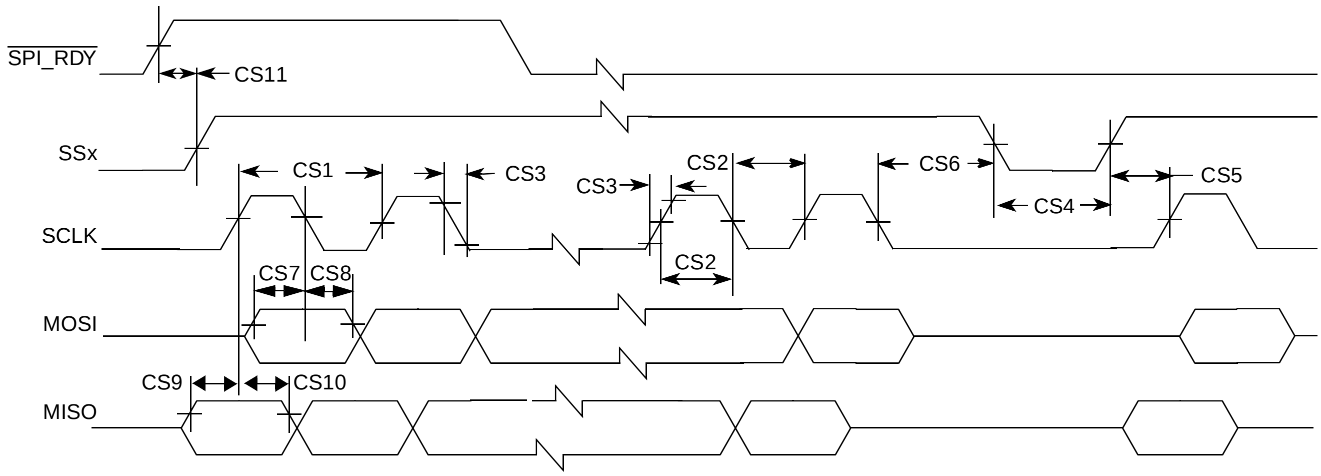

Figure 20. CSPI Master Mode Timing Diagram

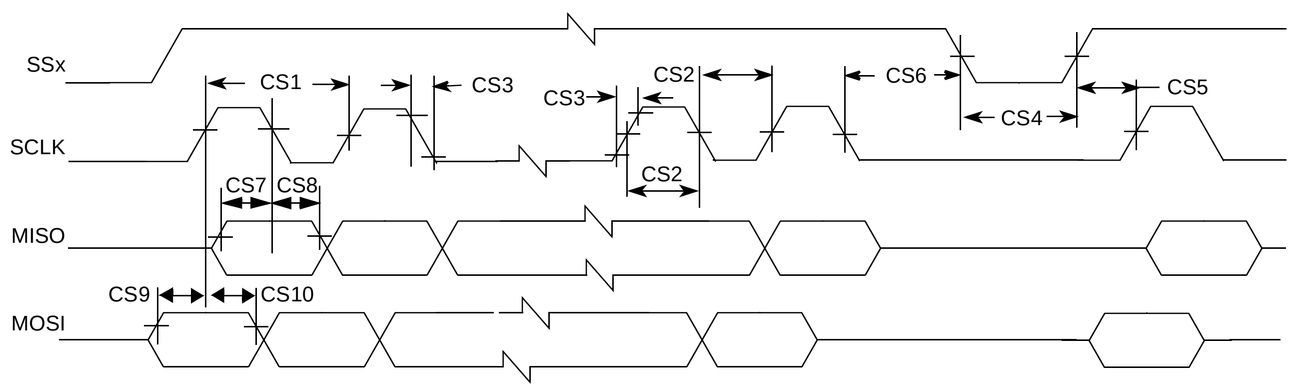

Figure 21. CSPI Slave Mode Timing Diagram

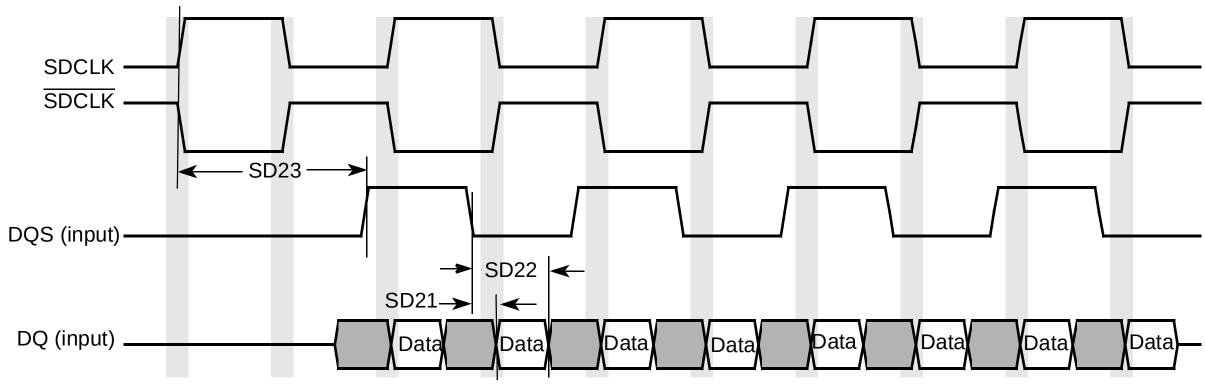

Figure 38. Mobile DDR SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram

Table 38. Mobile DDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
SD21	DQS – DQ Skew (defines the Data valid window in read cycles related to DQS).	tDQSQ	—	0.85	ns
SD22	DQS DQ HOLD time from DQS	tQH	2.3	—	ns
SD23	DQS output access time from SDCLK posedge	tDQSCK	—	6.7	ns

NOTE

SDRAM CLK and DQS related parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 38 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

4.3.10 ETM Electrical Specifications

ETM is an ARM protocol. The timing specifications in this section are given as a guide for a TPA that supports TRACECLK frequencies up to 133 MHz.

Figure 39 depicts the TRACECLK timings of ETM, and Table 39 lists the timing parameters.

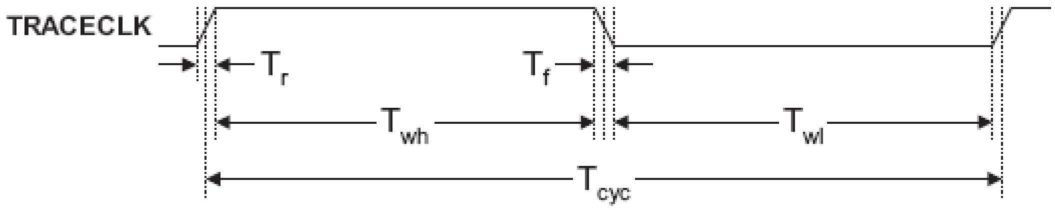

Figure 39. ETM TRACECLK Timing Diagram

Table 39. ETM TRACECLK Timing Parameters

ID	Parameter	Min	Max	Unit
T_{cyc}	Clock period	Frequency dependent	—	ns
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns

Figure 40 depicts the setup and hold requirements of the trace data pins with respect to TRACECLK, and Table 40 lists the timing parameters.

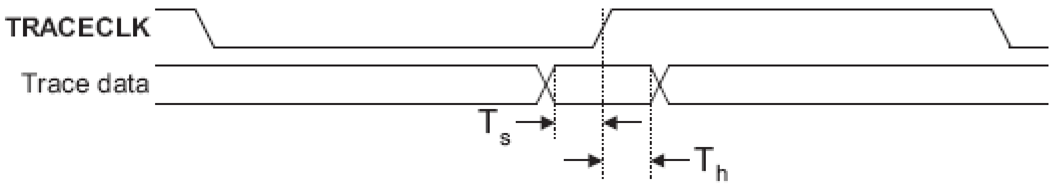

Figure 40. Trace Data Timing Diagram

Table 40. ETM Trace Data Timing Parameters

ID	Parameter	Min	Max	Unit
T_s	Data setup	2	—	ns
T_h	Data hold	1	—	ns

4.3.10.1 Half-Rate Clocking Mode

When half-rate clocking is used, the trace data signals are sampled by the TPA on both the rising and falling edges of TRACECLK, where TRACECLK is half the frequency of the clock shown in Figure 40.

4.3.11 FIR Electrical Specifications

FIR implements asynchronous infrared protocols (FIR, MIR) that are defined by IrDA® (Infrared Data Association). Refer to http://www.IrDA.org for details on FIR and MIR protocols.

4.3.12 Fusebox Electrical Specifications

Table 41. Fusebox Timing Characteristics

Ref. Num	Description	Symbol	Minimum	Typical	Maximum	Units
1	Program time for eFuse[1]	$t_{program}$	125	—	—	µs

[1] The program length is defined by the value defined in the epm_pgm_length[2:0] bits of the IIM module. The value to program is based on a 32 kHz clock source (4 * 1/32 kHz = 125 µs).

4.3.13 I²C Electrical Specifications

This section describes the electrical information of the I²C Module.

4.3.13.1 I²C Module Timing

Figure 41 depicts the timing of I²C module. Table 42 lists the I²C module timing parameters where the I/O supply is 2.7 V. 1

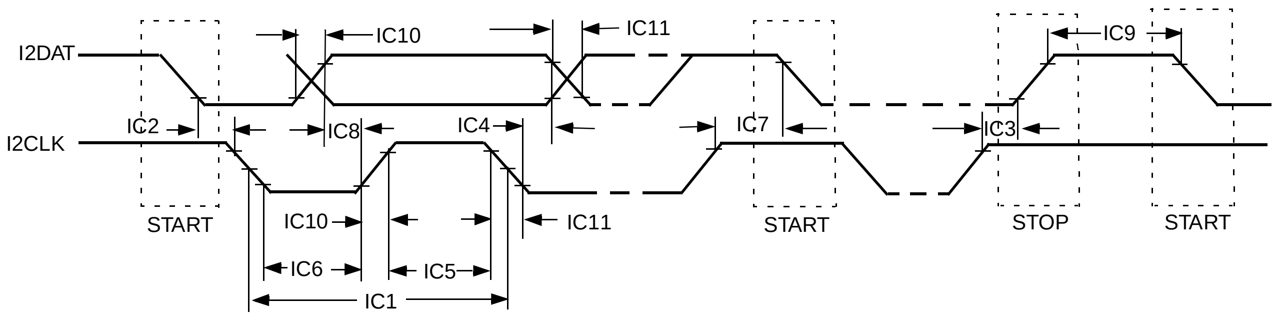

Figure 41. I²C Bus Timing Diagram

Table 42. I²C Module Timing Parameters—I²C Pin I/O Supply=2.7 V

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2CLK cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	$20+0.1C_b$[4]	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	$20+0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

2 The maximum hold time has to be met only if the device does not stretch the LOW period (ID IC6) of the I2CLK signal.

3 A Fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement of set-up time (ID IC7) of 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (ID No IC10) + data_setup_time (ID No IC8) = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the I2CLK line is released.

4 C_b = total capacitance of one bus line in pF.

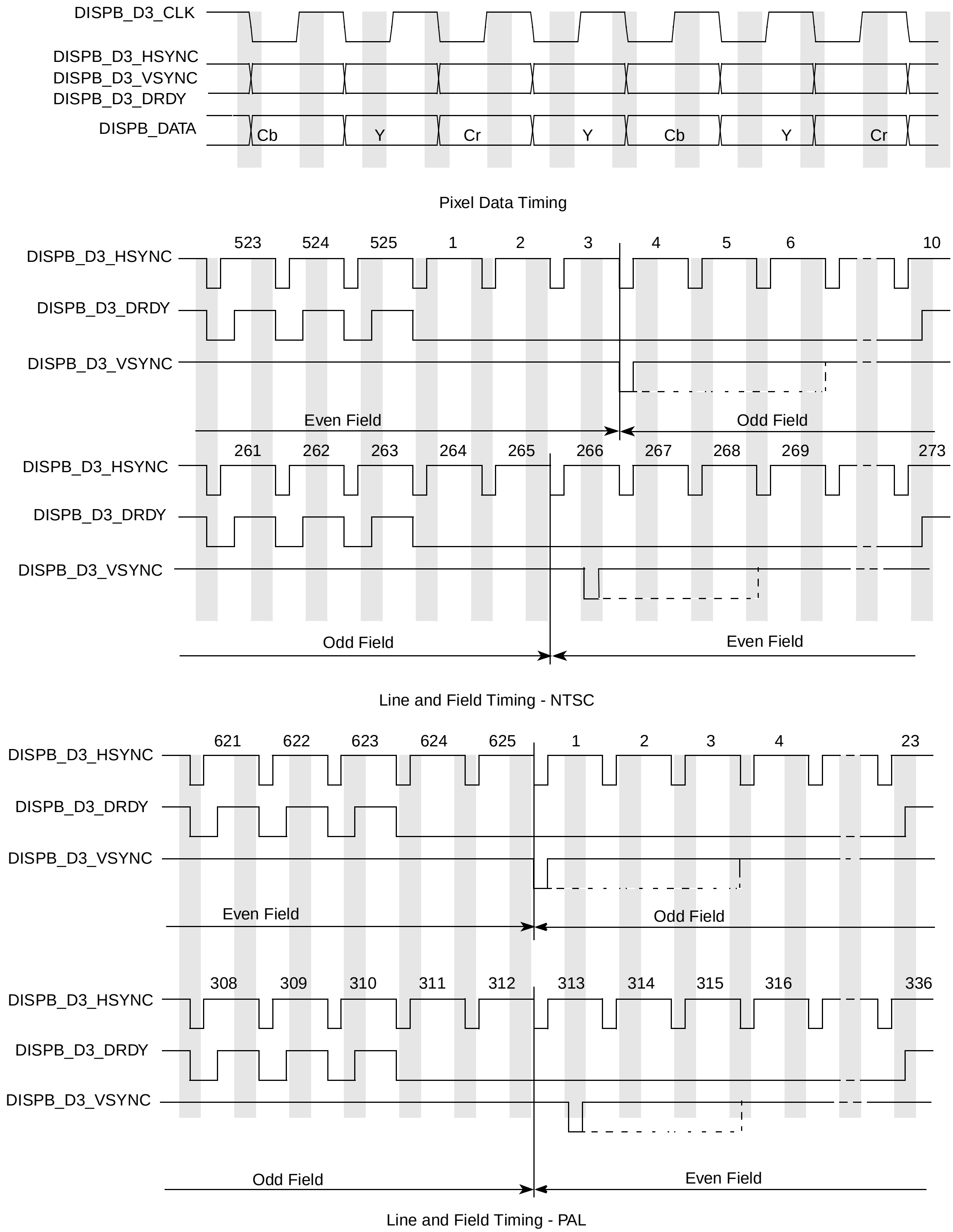

Figure 50. TV Encoder Interface Timing Diagram

4.3.15.4.2 Interface to a TV Encoder, Electrical Characteristics

The timing characteristics of the TV encoder interface are identical to the synchronous display characteristics. See Section 4.3.15.2.2, "Interface to Active Matrix TFT LCD Panels, Electrical Characteristics."

4.3.15.5 Asynchronous Interfaces

4.3.15.5.1 Parallel Interfaces, Functional Description

The IPU supports the following asynchronous parallel interfaces:

- System 80 interface
  - Type 1 (sampling with the chip select signal) with and without byte enable signals.
  - Type 2 (sampling with the read and write signals) with and without byte enable signals.
- System 68k interface
  - Type 1 (sampling with the chip select signal) with or without byte enable signals.
  - Type 2 (sampling with the read and write signals) with or without byte enable signals.

For each of four system interfaces, there are three burst modes:

1. Burst mode without a separate clock. The burst length is defined by the corresponding parameters of the IDMAC (when data is transferred from the system memory) of by the HBURST signal (when the MCU directly accesses the display via the slave AHB bus). For system 80 and system 68k type 1 interfaces, data is sampled by the CS signal and other control signals changes only when transfer direction is changed during the burst. For type 2 interfaces, data is sampled by the WR/RD signals (system 80) or by the ENABLE signal (system 68k) and the CS signal stays active during the whole burst.
2. Burst mode with the separate clock DISPB_BCLK. In this mode, data is sampled with the DISPB_BCLK clock. The CS signal stays active during whole burst transfer. Other controls are changed simultaneously with data when the bus state (read, write or wait) is altered. The CS signals and other controls move to non-active state after burst has been completed.
3. Single access mode. In this mode, slave AHB and DMA burst are broken to single accesses. The data is sampled with CS or other controls according the interface type as described above. All controls (including CS) become non-active for one display interface clock after each access. This mode corresponds to the ATI single access mode.

Both system 80 and system 68k interfaces are supported for all described modes as depicted in Figure 51, Figure 52, Figure 53, and Figure 54. These timing images correspond to active-low DISPB_D#_CS, DISPB_D#_WR and DISPB_D#_RD signals.

Additionally, the IPU allows a programmable pause between two burst. The pause is defined in the HSP_CLK cycles. It allows to avoid timing violation between two sequential bursts or two accesses to different displays. The range of this pause is from 4 to 19 HSP_CLK cycles.

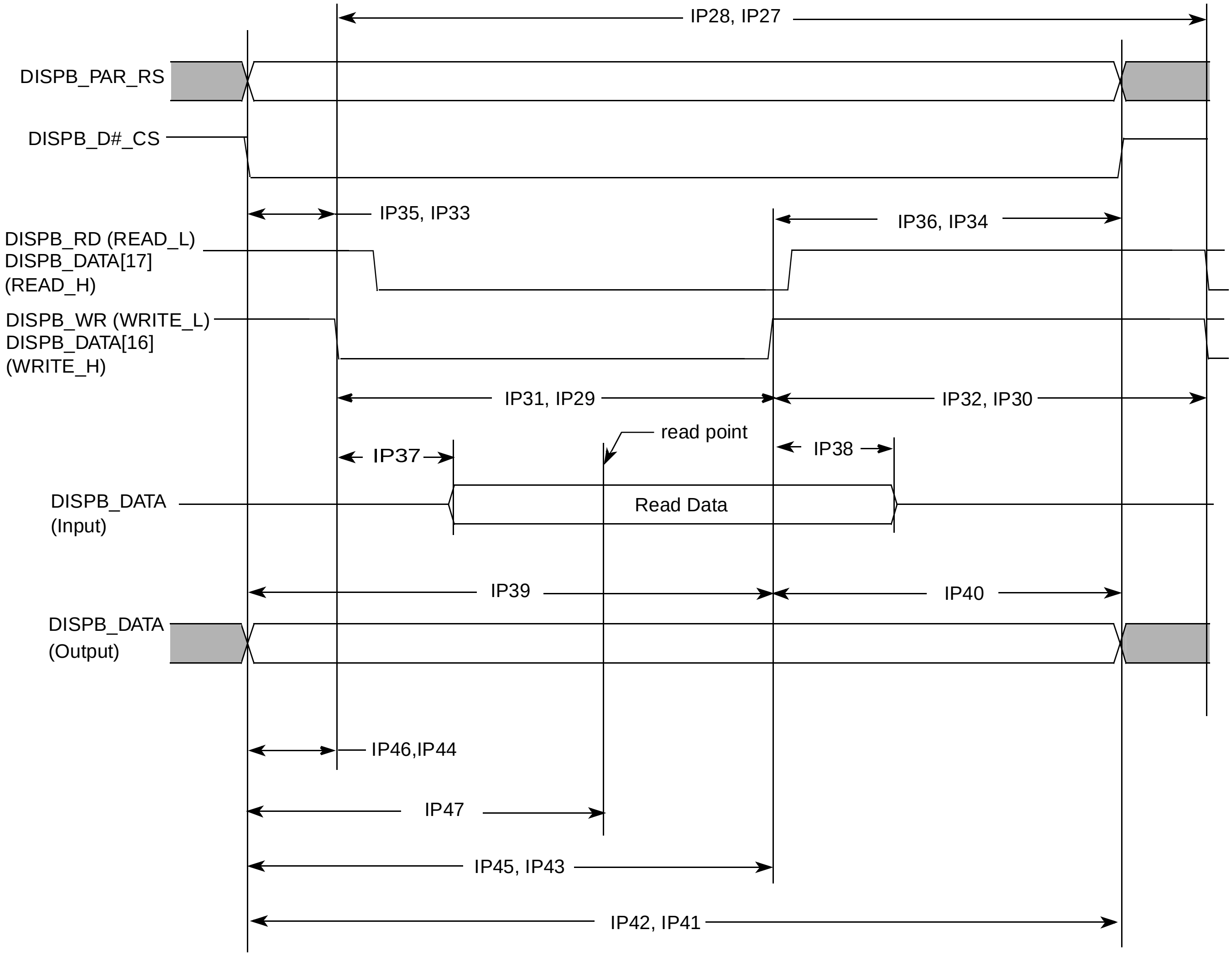

Figure 57. Asynchronous Parallel System 80 Interface (Type 2) Timing Diagram

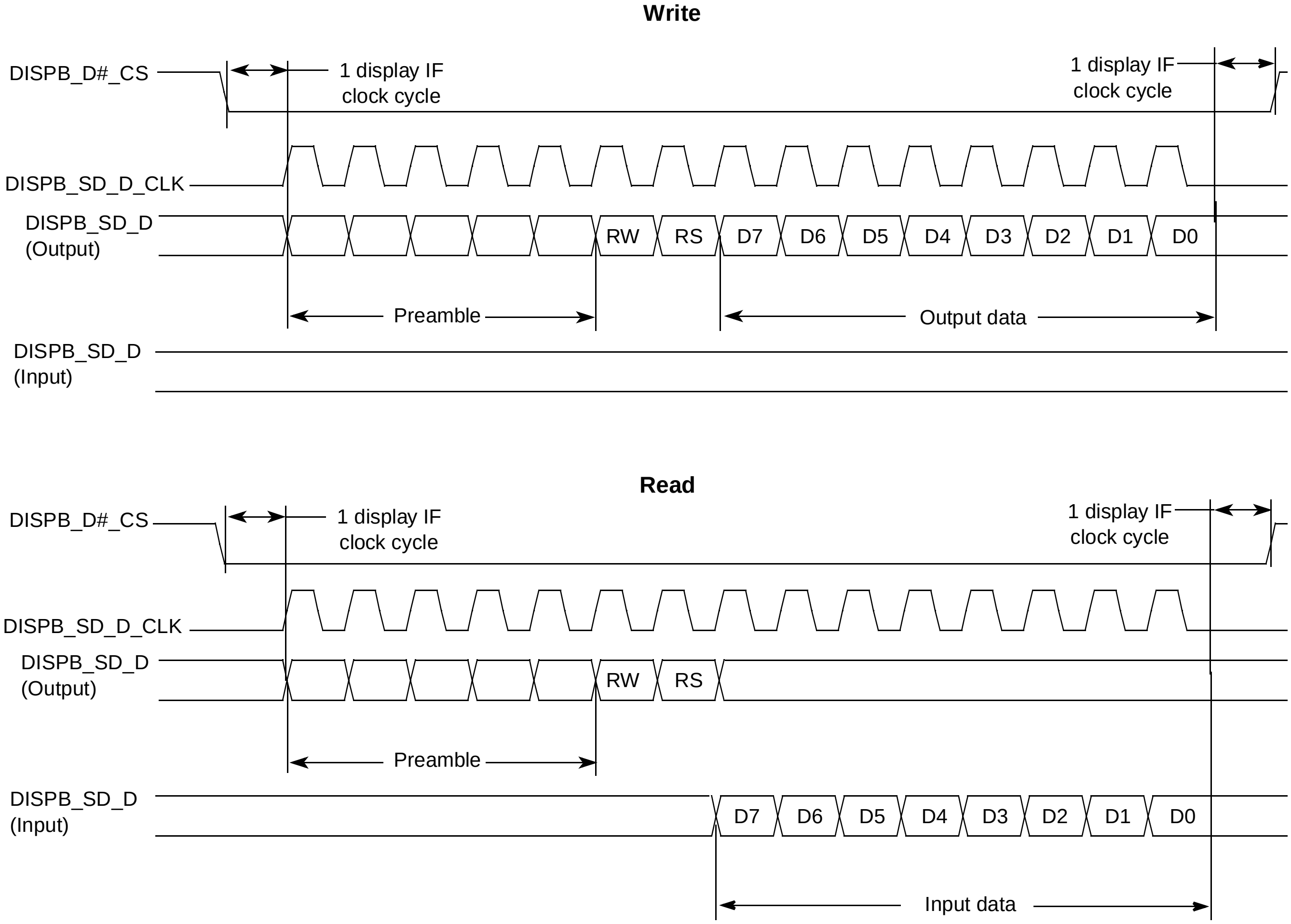

Figure 61. 4-Wire Serial Interface Timing Diagram

Figure 62 depicts timing of the 5-wire serial interface (Type 1). For this interface, a separate RS line is added. When a burst is transmitted within single active chip select interval, the RS can be changed at boundaries of words.

Figure 63 depicts timing of the 5-wire serial interface (Type 2). For this interface, a separate RS line is added. When a burst is transmitted within single active chip select interval, the RS can be changed at boundaries of words.

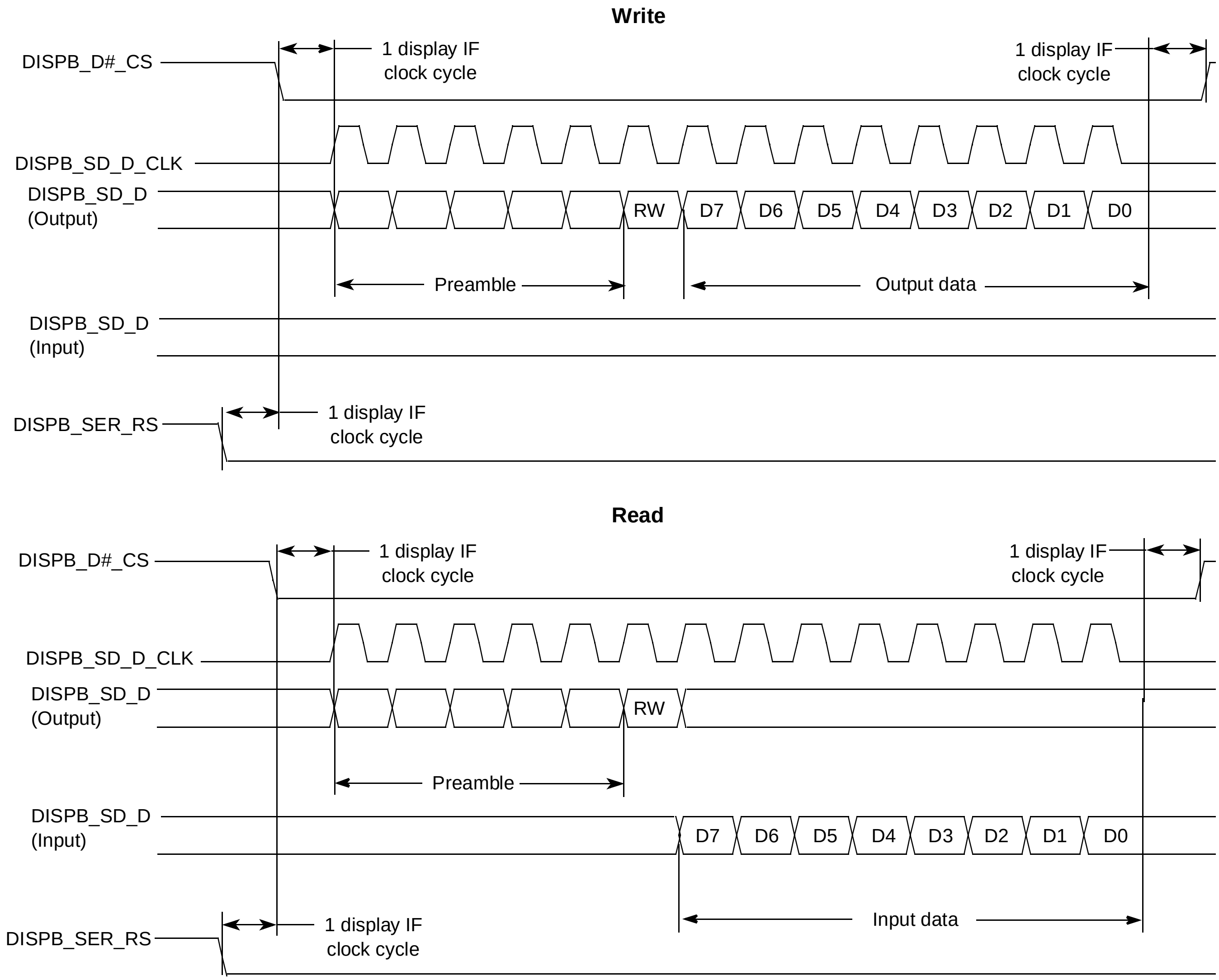

Figure 63. 5-Wire Serial Interface (Type 2) Timing Diagram

4.3.21 SJC Electrical Specifications

This section details the electrical characteristics for the SJC module. Figure 76 depicts the SJC test clock input timing. Figure 77 depicts the SJC boundary scan timing, Figure 78 depicts the SJC test access port, Figure 79 depicts the SJC $\overline{\text{TRST}}$ timing, and Table 58 lists the SJC timing parameters.

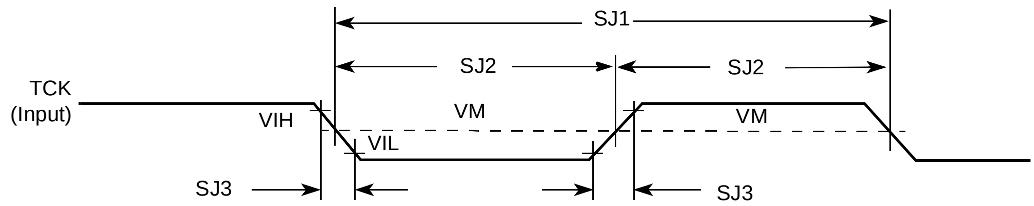

Figure 76. Test Clock Input Timing Diagram

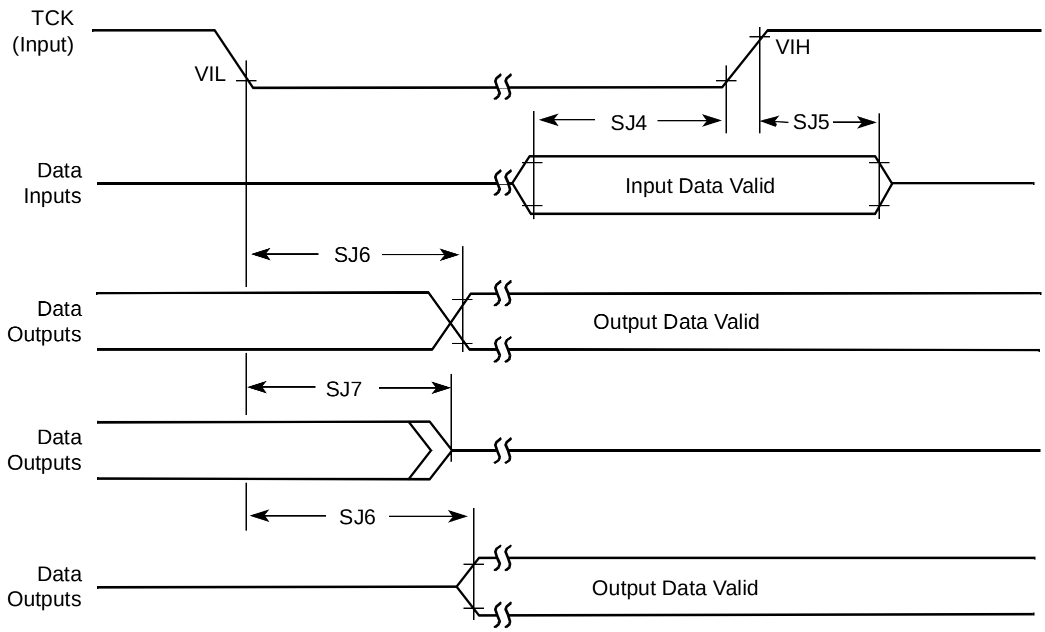

Figure 77. Boundary Scan (JTAG) Timing Diagram

Table 62. SSI Receiver with External Clock Timing Parameters (continued)

ID	Parameter	Min	Max	Unit
SS28	(Rx) CK high to FS (bl) high	–10.0	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10.0	—	ns
SS32	(Rx) CK high to FS (wl) high	–10.0	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10.0	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10.0	—	ns
SS41	SRXD hold time after (Rx) CK low	2.0	—	ns

4.3.23 USB Electrical Specifications

This section describes the electrical information of the USBOTG port. The OTG port supports both serial and parallel interfaces.

The high speed (HS) interface is supported via the ULPI (Ultra Low Pin Count Interface). Figure 84 depicts the USB ULPI timing diagram, and Table 63 lists the timing parameters.

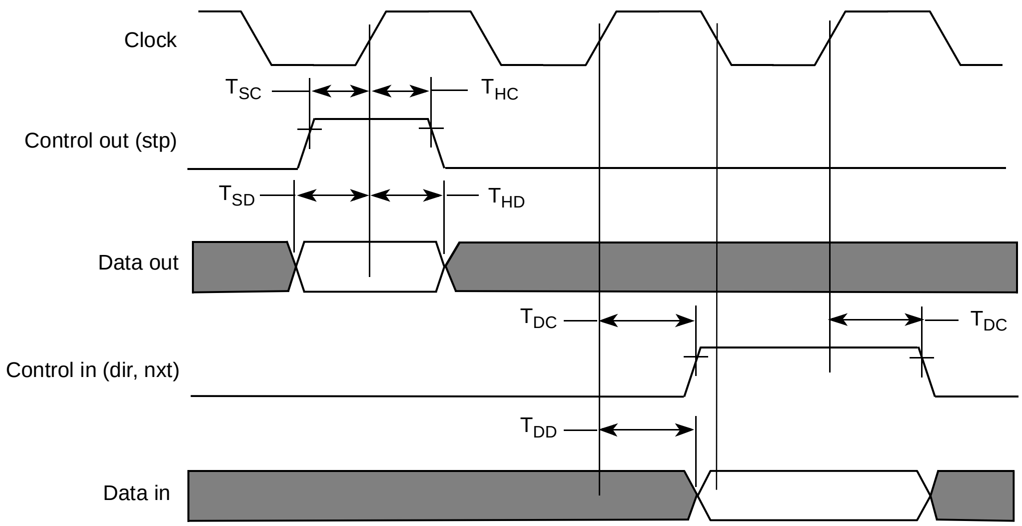

Figure 84. USB ULPI Interface Timing Diagram

Table 63. USB ULPI Interface Timing Specification[1]

Parameter	Symbol	Min	Max	Units
Setup time (control in, 8-bit data in)	T_{SC}, T_{SD}	6	—	ns
Hold time (control in, 8-bit data in)	T_{HC}, T_{HD}	0	—	ns
Output delay (control out, 8-bit data out)	T_{DC}, T_{DD}	—	9	ns

1 Timing parameters are given as viewed by transceiver side.

5.1.2 MAPBGA Signal Assignment–14 × 14 mm 0.5 mm

See Section 7, "Revision History," Figure 69 for the 0.5 mm 14 × 14 MAPBGA signal assignments.

5.1.3 Connection Tables–14 x 14 mm 0.5 mm

Table 64 shows the device connection list for power and ground, alpha-sorted. Table 65 shows the device connection list for signals.

5.1.3.1 Ground and Power ID Locations–14 x 14 mm 0.5 mm

Table 64. 14 x 14 MAPBGA Ground/Power ID by Ball Grid Location

GND/PWR ID	Ball Location
FGND	AB24
FUSE_VDD	AC24
FVCC	AA24
GND	A1, A2, A25, A26, B1, B2, B25, B26, C1, C2, C24, C25, C26, D1, D25, E22, E24, F21, L12, M11, M12, M13, M14, M15, M16, N12, N13, N14, N15, N16, P12, P13, P14, P15, P16, R12, R13, R14, R15, R16, T12, T13, V17, AC2, AC26, AD1, AD2, AD24, AD25, AD26, AE1, AE2, AE24, AE25, AE26, AF1, AF2, AF25, AF26
IOQVDD	Y6
MGND	T15
MVCC	V15
NVCC1	G19, G21, K18
NVCC2	Y17, Y18, Y19, Y20
NVCC3	L9, M9, N11
NVCC4	L18, L19
NVCC5	E5, F6, G7
NVCC6	J15, J16, K15
NVCC7	N18, P18, R18, T18
NVCC8	J12, J13
NVCC9	J17
NVCC10	P9, P11, R11, T11
NVCC21	Y14, Y15, Y16
NVCC22	W7, Y7, Y8, Y9, Y10, Y11, Y12, Y13, AA6
QVCC	J14, L13, L14, L15, L16, M18, U18, V10, V11, V12, V13
QVCC1	J10, J11, K9, L11
QVCC4	N9, R9, T9, U9
SGND	T14
SVCC	V14
UVCC	V16
UGND	T16

5.1.3.2 BGA Signal ID by Ball Grid Location–14 x 14 0.5 mm

Table 65 shows the device connection list for signals only, alpha-sorted by signal identification.

Table 65. 14 x 14 BGA Signal ID by Ball Grid Location

Signal ID	Ball Location	Signal ID	Ball Location
A0	AD6	CKIL	H21
A1	AF5	CLKO	C23
A10	AF18	CLKSS	G26
A11	AC3	COMPARE	G18
A12	AD3	CONTRAST	R24
A13	AD4	CS0	AE23
A14	AF17	CS1	AF23
A15	AF16	CS2	AE21
A16	AF15	CS3	AD22
A17	AF14	CS4	AF24
A18	AF13	CS5	AF22
A19	AF12	CSI_D10	M24
A2	AB5	CSI_D11	L26
A20	AF11	CSI_D12	M21
A21	AF10	CSI_D13	M25
A22	AF9	CSI_D14	M20
A23	AF8	CSI_D15	M26
A24	AF7	CSI_D4	L21
A25	AF6	CSI_D5	K25
A3	AE4	CSI_D6	L24
A4	AA3	CSI_D7	K26
A5	AF4	CSI_D8	L20
A6	AB3	CSI_D9	L25
A7	AE3	CSI_HSYNC	K20
A8	AD5	CSI_MCLK	K24
A9	AF3	CSI_PIXCLK	J26
ATA_CS0	J6	CSI_VSYNC	J25
ATA_CS1	F2	CSPI1_MISO	P7
ATA_DIOR	E2	CSPI1_MOSI	P2
ATA_DIOW	H6	CSPI1_SCLK	N2
ATA_DMACK	F1	CSPI1_SPI_RDY	N3
$\overline{\text{ATA\_RESET}}$	H3	CSPI1_SS0	P3
BATT_LINE	F7	CSPI1_SS1	P1
BCLK	AB26	CSPI1_SS2	P6
BOOT_MODE0	F20	CSPI2_MISO	A4
BOOT_MODE1	C21	CSPI2_MOSI	E3
BOOT_MODE2	D24	CSPI2_SCLK	C7
BOOT_MODE3	C22	CSPI2_SPI_RDY	B6
BOOT_MODE4	D26	CSPI2_SS0	B5
CAPTURE	A22	CSPI2_SS1	C6
CAS	AD20	CSPI2_SS2	A5
CE_CONTROL	A14	CSPI3_MISO	G3
CKIH	F24	CSPI3_MOSI	D2

Table 67. 19 x 19 BGA No Connects[1]

Signal	Ball Location
NC	N7
NC	P7
NC	U21

[1] These contacts are not used and must be floated by the user.

5.2.3.2 BGA Signal ID by Ball Grid Location—19 x 19 0.8 mm

Table 68. 19 x 19 BGA Signal ID by Ball Grid Location

Signal ID	Ball Location	Signal ID	Ball Location
A0	Y6	CKIL	E21
A1	AC5	CLKO	C20
A10	V15	CLKSS	H17
A11	AB3	COMPARE	A20
A12	AA3	CONTRAST	N21
A13	Y3	CS0	U17
A14	Y15	CS1	Y22
A15	Y14	CS2	Y18
A16	V14	CS3	Y19
A17	Y13	CS4	Y20
A18	V13	CS5	AA21
A19	Y12	CSI_D10	K21
A2	AB5	CSI_D11	K22
A20	V12	CSI_D12	K23
A21	Y11	CSI_D13	L20
A22	V11	CSI_D14	L18
A23	Y10	CSI_D15	L21
A24	Y9	CSI_D4	J20
A25	Y8	CSI_D5	J21
A3	AA5	CSI_D6	L17
A4	Y5	CSI_D7	J22
A5	AC4	CSI_D8	J23
A6	AB4	CSI_D9	K20
A7	AA4	CSI_HSYNC	H22
A8	Y4	CSI_MCLK	H20
A9	AC3	CSI_PIXCLK	H23
ATA_CS0	E1	CSI_VSYNC	H21
ATA_CS1	G4	CSPI1_MISO	N2
ATA_DIOR	E3	CSPI1_MOSI	N1
ATA_DIOW	H6	CSPI1_SCLK	M4
ATA_DMACK	E2	CSPI1_SPI_RDY	M1
$\overline{\text{ATA\_RESET}}$	F3	CSPI1_SS0	M2
BATT_LINE	F6	CSPI1_SS1	N6
BCLK	W20	CSPI1_SS2	M3

5.3 Ball Maps

Table 69. Ball Map—14 x 14 0.5 mm Pitch

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	GND	GND	SFS5	CSPI2_MISO	CSPI2_SS2	USBOTG_DATA7	USBOTG_DATA3	USBOTG_NXT	USB_BYP	RXD1	DSR_DCE1	DSR_DTE1	RXD2	CE_CONTROL	KEY_ROW3	KEY_ROW7	KEY_COL3	KEY_COL7	TDO	SJC_MOD	SVEN0	CAPTURE	GPIO1_6	WATCHDOG_RST	GND	GND	A
B	GND	GND	STXD4	SRXD5	CSPI2_SS0	CSPI2_SPI_RDY	USBOTG_DATA5	USBOTG_DATA1	USBOTG_DIR	USB_PWR	CTS1	DCD_DCE1	DCD_DTE1	RTS2	KEY_ROW1	KEY_ROW5	KEY_COL1	KEY_COL5	TCK	TRSTB	SRX0	SCLK0	GPIO1_1	GPIO1_5	GND	GND	B
C	GND	GND	SRXD4	SCK4	STXD5	CSPI2_SS1	CSPI2_SCLK	USBOTG_DATA4	USBOTG_STP	USB_OC	DTR_DCE1	DTR_DTE1	TXD2	KEY_ROW2	KEY_COL0	KEY_COL4	RTCK	DE	SRST0	GPIO1_2	BOOT_MODE1	BOOT_MODE3	CLKO	GND	GND	GND	C
D	GND	CSPI3_MOSI	SCK5																					BOOT_MODE2	GND	BOOT_MODE4	D
E	CSPI3_SCLK	ATA_DIOR	CSPI2_MOSI		NVCC5																	GND		GND	DVFS0	POWER_FAIL	E
F	ATA_DMACK	ATA_CS1	SFS4			NVCC5	BATT_LINE	USBOTG_DATA6	USBOTG_DATA0	TXD1	RI_DCE1	DTR_DCE2	KEY_ROW0	KEY_ROW6	KEY_COL6	TDI	STX0	GPIO1_0	GPIO1_4	BOOT_MODE0	GND			CKIH	GPIO1_3	VSTBY	F
G	PWMO	PC_RW	CSPI3_MISO			CSPI3_SPI_RDY	NVCC5		USBOTG_DATA2	USBOTG_CLK	RTS1	RI_DTE1	CTS2	KEY_ROW4	KEY_COL2	TMS	SIMPD0	COMPARE	NVCC1		NVCC1			DVFS1	VPG0	CLKSS	G
H	PC_RST	PC_BVD1	ATA_RESET			ATA_DIOW															CKIL			POR	I2C_DAT	GPIO3_1	H
J	PC_VS1	PC_READY	IOIS16			ATA_CS0	PC_POE			QVCC1	QVCC1	NVCC8	NVCC8	QVCC	NVCC6	NVCC6	NVCC9			VPG1	RESET_IN			I2C_CLK	CSI_VSYNC	CSI_PIXCLK	J
K	PC_CD2	SD1_DATA3	PC_PWRON			PC_BVD2	PC_VS2		QVCC1						NVCC6			NVCC1		CSI_HSYNC	GPIO3_0			CSI_MCLK	CSI_D5	CSI_D7	K
L	SD1_DATA1	SD1_CMD	SD1_DATA2			PC_WAIT	PC_CD1		NVCC3		QVCC1	GND	QVCC	QVCC	QVCC	QVCC		NVCC4	NVCC4	CSI_D8	CSI_D4			CSI_D6	CSI_D9	CSI_D11	L
M	USBH2_DATA0	USBH2_STP	USBH2_DATA1			SD1_DATA0	SD1_CLK		NVCC3		GND	GND	GND	GND	GND	GND		QVCC		CSI_D14	CSI_D12			CSI_D10	CSI_D13	CSI_D15	M
N	USBH2_CLK	CSPI1_SCLK	CSPI1_SPI_RDY			USBH2_NXT	USBH2_DIR		QVCC4		NVCC3	GND	GND	GND	GND	GND		NVCC7		SD_D_I	FPSHIFT			VSYNC0	HSYNC	DRDY0	N
P	CSPI1_SS1	CSPI1_MOSI	CSPI1_SS0			CSPI1_SS2	CSPI1_MISO		NVCC10		NVCC10	GND	GND	GND	GND	GND		NVCC7		READ	LCS1			SD_D_CLK	SD_D_IO	LCS0	P
R	STXD3	SCK3	SRXD3			SFS3	SRXD6		QVCC4		NVCC10	GND	GND	GND	GND	GND		NVCC7		D3_CLS	PAR_RS			CONTRAST	WRITE	VSYNC3	R
T	STXD6	SCK6	SFS6			NFCE	NFWE		QVCC4		NVCC10	GND	GND	SGND	MGND	UGND		NVCC7		LD4	LD2			LD0	SER_RS	D3_REV	T
U	NFRB	NFWP	NFCLE			D15	D11		QVCC4									QVCC		TTM_PAD	LD8			LD6	D3_SPL	LD1	U
V	NFALE	NFRE	D13			D9	D5			QVCC	QVCC	QVCC	QVCC	SVCC	MVCC	UVCC	GND			LD17	LD13			LD10	LD3	LD5	V
W	D14	D12	D7			D3	NVCC22														EB0			LD15	LD7	LD9	W
Y	D10	D8	D1			IOQVDD	NVCC22	NVCC22	NVCC22	NVCC22	NVCC22	NVCC22	NVCC22	NVCC21	NVCC21	NVCC21	NVCC2	NVCC2	NVCC2	NVCC2	M_GRANT			EB1	LD11	LD12	Y
AA	D6	D4	A4			NVCC22	SD31	SD28	SD27	SD23	SD21	SD18	SD16	SD13	SD9	SD7	SD5	SD3	SD2	DQM2	SDCLK			FVCC	LD14	LD16	AA
AB	D2	D0	A6		A2																	RW		FGND	OE	BCLK	AB
AC	MA10	GND	A11																					FUSE_VDD	M_REQUEST	GND	AC
AD	GND	GND	A12	A13	A8	A0	SDBA0	SDQS3	SD29	SD25	SDQS2	SD17	SD15	SD12	SD8	SDQS0	SD4	SD0	DQM1	CAS	SDCKE0	CS3	ECB	GND	GND	GND	AD
AE	GND	GND	A7	A3	SDBA1	SD30	SD26	SD24	SD22	SD20	SD19	SDQS1	SD14	SD11	SD10	SD6	SD1	DQM3	DQM0	SDCLK	CS2	LBA	CS0	GND	GND	GND	AE
AF	GND	GND	A9	A5	A1	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A10	RAS	SDWE	SDCKE1	CS5	CS1	CS4	GND	GND	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	