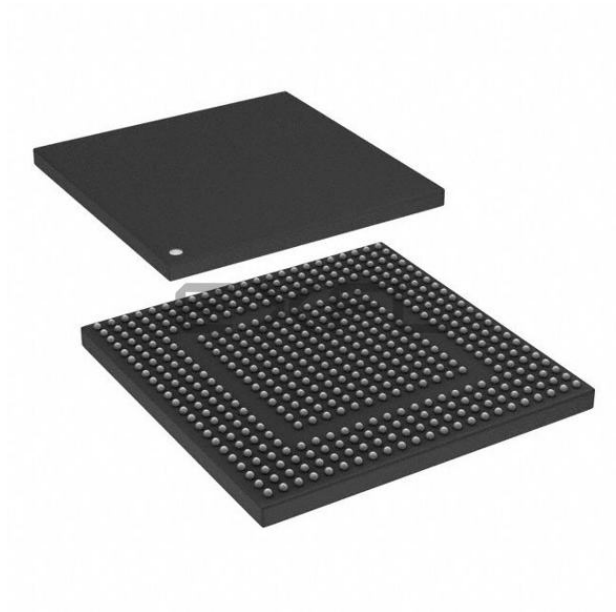

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM1136JF-S |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 532MHz |
| Co-Processors/DSP | Multimedia; GPU, IPU, MPEG-4, VFP |
| RAM Controllers | DDR |
| Graphics Acceleration | Yes |
| Display & Interface Controllers | Keyboard, Keypad, LCD |
| Ethernet | - |
| SATA | - |
| USB | USB 2.0 (3) |
| Voltage - I/O | 1.8V, 2.0V, 2.5V, 2.7V, 3.0V |
| Operating Temperature | -20°C ~ 70°C (TA) |
| Security Features | Random Number Generator, RTIC, Secure Fusebox, Secure JTAG, Secure Memory |
| Package / Case | 473-LFBGA |
| Supplier Device Package | 473-LFBGA (19x19) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx31ldvmn5dr2 |

# 3 Signal Descriptions

Signal descriptions are in the reference manual. Special signal considerations are listed following this paragraph. The BGA ball assignment is in Section 5, "Package Information and Pinout."

Special Signal Considerations:

- **Tamper detect (GPIO1_6)**

  Tamper detect logic is used to issue a security violation. This logic is activated if the tamper detect input is asserted.

  The tamper detect logic is disabled after reset. After enabling the logic, it is impossible to disable it until the next reset. The GPR[16] bit functions as the tamper detect enable bit.

  GPIO1_6 functions similarly to other I/O with GPIO capabilities regardless of the status of the tamper detect enable bit. (For example, the GPIO1_6 can function as an input with GPIO capabilities, such as sampling through PSR or generating interrupts.)

- **Power ready (GPIO1_5)**

  The power ready input, GPIO1_5, should be connected to an external power management IC power ready output signal. If not used, GPIO1_5 must either be (a) externally pulled-up to NVCC1 or (b) a no connect, internally pulled-up by enabling the on-chip pull-up resistor. GPIO1_5 is a dedicated input and cannot be used as a general-purpose input/output.

- **SJC_MOD**

  SJC_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed, but the value should be much smaller than the on-chip 100 kΩ pull-up.

- **CE_CONTROL**
  CE_CONTROL is a reserved input and must be externally tied to GND through a 1 kΩ resistor.

- **TTM_PAD**
  This is for Freescale factory use only. Control bits indicate that the pull-up/down is disabled. However, the TTM_PAD is actually connected to an on-chip pull-down device. Users must either float this signal or tie it to GND.

- **M_REQUEST and M_GRANT**

  These two signals are not utilized internally. The user should make no connection to these signals.

- **Clock Source Select (CLKSS)**

  The CLKSS is the input that selects the default reference clock source providing input to the DPLL. To select CKIH, tie CLKSS to NVCC1. To select CKIL, tie CLKSS to ground. After initialization, the reference clock source can be changed (initial setting is overwritten) by programming the PRCS bits in the CCMR.

Table 8 provides the operating ranges.

**NOTE**

The term NVCC in this section refers to the associated supply rail of an input or output. The association is shown in the Signal Multiplexing chapter of the reference manual.

**CAUTION**

NVCC6 and NVCC9 must be at the same voltage potential. These supplies are connected together on-chip to optimize ESD damage immunity.

**Table 8. Operating Ranges**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| QVCC, QVCC1, QVCC4 | Core Operating Voltage[1,2,3]<br>$0 \le f_{ARM} \le 400$ MHz, non-overdrive<br>$0 \le f_{ARM} \le 532$ MHz, non-overdrive<br>$0 \le f_{ARM} \le 532$ MHz, overdrive[4] | <br>1.22<br>1.38<br>1.52 | <br>1.47<br>1.52<br>1.65 | V |
| | State Retention Voltage[5] | 0.95 | — | |
| NVCC1, NVCC3–10 | I/O Supply Voltage, except DDR[6]non-overdrive<br>overdrive[7] | 1.75<br>>3.1 | 3.1<br>3.3 | V |
| NVCC2, NVCC21, NVCC22 | I/O Supply Voltage, DDR only | 1.75 | 1.95 | V |
| FVCC, MVCC, SVCC, UVCC | PLL (Phase-Locked Loop) and FPM (Frequency Pre-multiplier) Supply Voltage[8]<br>non-overdrive<br>overdrive[4] | <br>1.3<br>>1.47 | <br>1.47<br>1.6 | V |
| IOQVDD | On-device Level Shifter Supply Voltage | 1.6 | 1.9 | V |
| FUSE_VDD | Fusebox read Supply Voltage[9, 10] | 1.65 | 1.95 | V |
| | Fusebox write (program) Supply Voltage[11] | 3.0 | 3.3 | V |
| $T_A$ | Operating Ambient Temperature Range[12] | –20 | 70 | $^0$C |

1 Measured at package balls, including peripherals, ARM, and L2 cache supplies (QVCC, QVCC1, QVCC4, respectively).

2 The core voltage must be higher than 1.38V to avoid corrupted data during transfers from the USB HS. Please refer to Errata file ENGcm02610 ID.

3 If the Core voltage is supplied by the MC13738, it will be 1.6 ± 0.05 V during the power-up sequence and this is allowed. After power-up the voltage should be reduced to avoid operation in overdrive mode.

4 Supply voltage is considered “overdrive” for voltages above 1.52 V. Operation time in overdrive—whether switching or not—must be limited to a cumulative duration of 1.25 years (10,950 hours) or less to sustain the maximum operating voltage without significant device degradation—for example, 25% (average 6 hours out of 24 yours per day) duty cycle for 5-year rated equipment. To tolerate the maximum operating overdrive voltage for 10 years, the device must have a duty cycle of 12.5% or less in overdrive (for example 3 out of 24 hours per day). Below 1.52 V, duty cycle restrictions may apply for equipment rated above 5 years.

5 The SR voltage is applied to QVCC, QVCC1, and QVCC4 after the device is placed in SR mode. The Real-Time Clock (RTC) is operational in State Retention (SR) mode.

6 Overshoot and undershoot conditions (transitions above NVCC and below GND) on I/O must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

Table 13 shows the core current consumption for –20°C to 70°C for Silicon Revision 2.0.1 for the MCIMX31.

**Table 13. Current Consumption for –20°C to 70°C[1, 2] for Silicon Revision 2.0.1**

| Mode | Conditions | QVCC (Peripheral) | | QVCC1 (ARM) | | QVCC4 (L2) | | FVCC, +MVCC, +SVCC, +UVCC (PLL) | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Typ | Max | Typ | Max | Typ | Max | Typ | Max | |
| Deep Sleep | • QVCC = 0.95 V<br>• ARM and L2 caches are power gated (QVCC1 2= QVCC4 = 0 V)<br>• All PLLs are off, VCC = 1.4 V<br>• ARM is in well bias<br>• FPM is off<br>• 32 kHz input is on<br>• CKIH input is off<br>• CAMP is off<br>• TCK input is off<br>• All modules are off<br>• No external resistive loads<br>• RNGA oscillator is off | 0.16 | — | — | — | — | — | 0.02 | — | mA |
| State Retention | • QVCC and QVCC1 = 0.95 V<br>• L2 caches are power gated (QVCC4 = 0 V)<br>• All PLLs are off, VCC = 1.4 V<br>• ARM is in well bias<br>• FPM is off<br>• 32 kHz input is on<br>• CKIH input is off<br>• CAMP is off<br>• TCK input is off<br>• All modules are off<br>• No external resistive loads<br>• RNGA oscillator is off | 0.16 | — | 0.07 | — | — | — | 0.02 | — | mA |
| Wait | • QVCC,QVCC1, and QVCC4 = 1.22 V<br>• ARM is in wait for interrupt mode<br>• MAX is active<br>• L2 cache is stopped but powered<br>• MCU PLL is on (532 MHz), VCC = 1.4 V<br>• USB PLL and SPLL are off, VCC = 1.4 V<br>• FPM is on<br>• CKIH input is on<br>• CAMP is on<br>• 32 kHz input is on<br>• All clocks are gated off<br>• All modules are off (by programming CGR[2:0] registers)<br>• RNGA oscillator is off<br>• No external resistive loads | 6.00 | — | 2.20 | — | 0.03 | — | 3.60 | — | mA |

1 Typical column: TA = 25°C

2 Maximum column: TA = 70°C

### 4.2.2 Powering Down

For silicon revisions beginning with Revision 2.0.1 there is no special requirements for the power down sequence.

## 4.3 Module-Level Electrical Specifications

This section contains the MCIMX31 electrical information including timing specifications, arranged in alphabetical order by module name.

### 4.3.1 I/O Pad (PADIO) Electrical Specifications

This section specifies the AC/DC characterization of functional I/O of the MCIMX31. There are two main types of I/O: regular and DDR. In this document, the “Regular” type is referred to as GPIO.

#### 4.3.1.1 DC Electrical Characteristics

The MCIMX31 I/O parameters appear in Table 14 for GPIO. See Table 8 for temperature and supply voltage ranges.

**NOTE**

The term NVCC in this section refers to the associated supply rail of an input or output. The association is shown in the Signal Multiplexing chapter of the reference manual. NVCC for Table 14 refers to NVCC1 and NVCC3–10; QVCC refers to QVCC, QVCC1, and QVCC4.

**Table 14. GPIO DC Electrical Parameters**

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| High-level output voltage | $V_{OH}$ | $I_{OH}$ = –1 mA | NVCC –0.15 | — | — | V |
| | | $I_{OH}$ = specified Drive | 0.8*NVCC | — | — | V |
| Low-level output voltage | $V_{OL}$ | $I_{OL}$ = 1 mA | — | — | 0.15 | V |
| | | $I_{OL}$ = specified Drive | — | — | 0.2*NVCC | V |
| High-level output current, slow slew rate | $I_{OH\_S}$ | $V_{OH}$=0.8*NVCC<br>Std Drive<br>High Drive<br>Max Drive | <br>–2<br>–4<br>–8 | — | — | mA |
| High-level output current, fast slew rate | $I_{OH\_F}$ | $V_{OH}$=0.8*NVCC<br>Std Drive<br>High Drive<br>Max Drive | <br>–4<br>–6<br>–8 | — | — | mA |
| Low-level output current, slow slew rate | $I_{OL\_S}$ | $V_{OL}$=0.2*NVCC<br>Std Drive<br>High Drive<br>Max Drive | <br>2<br>4<br>8 | — | — | mA |

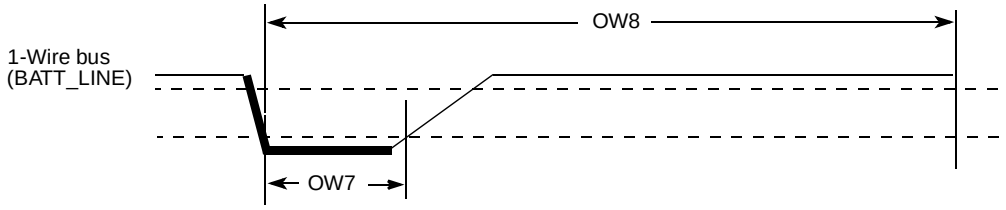



**Figure 8. Write 1 Sequence Timing Diagram**

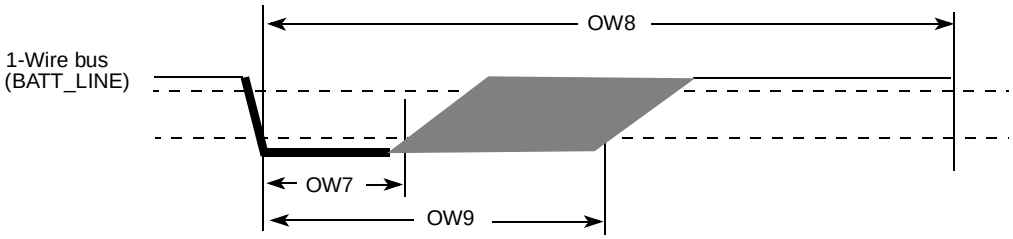



**Figure 9. Read Sequence Timing Diagram**

**Table 22. WR1/RD Timing Parameters**

| ID | Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| OW7 | Write 1 / Read Low Time | $t_{LOW1}$ | 1 | 5 | 15 | µs |
| OW8 | Transmission Time Slot | $t_{SLOT}$ | 60 | 117 | 120 | µs |
| OW9 | Release Time | $t_{RELEASE}$ | 15 | — | 45 | µs |

## 4.3.5 ATA Electrical Specifications (ATA Bus, Bus Buffers)

This section discusses ATA parameters. For a detailed description, refer to the ATA specification.

The user needs to use level shifters for 3.3 Volt or 5.0 Volt compatibility on the ATA interface.

The use of bus buffers introduces delay on the bus and introduces skew between signal lines. These factors make it difficult to operate the bus at the highest speed (UDMA-5) when bus buffers are used. If fast UDMA mode operation is needed, this may not be compatible with bus buffers.

Another area of attention is the slew rate limit imposed by the ATA specification on the ATA bus. According to this limit, any signal driven on the bus should have a slew rate between 0.4 and 1.2 V/ns with a 40 pF load. Not many vendors of bus buffers specify slew rate of the outgoing signals.

When bus buffers are used, the ata_data bus buffer is special. This is a bidirectional bus buffer, so a direction control signal is needed. This direction control signal is ata_buffer_en. When its high, the bus should drive from host to device. When its low, the bus should drive from device to host. Steering of the signal is such that contention on the host and device tri-state busses is always avoided.

### 4.3.5.1 Timing Parameters

In the timing equations, some timing parameters are used. These parameters depend on the implementation of the ATA interface on silicon, the bus buffer used, the cable delay and cable skew. Table 23 shows ATA timing parameters.

**Table 23. ATA Timing Parameters**

| Name | Description | Value/ Contributing Factor[1] |
|---|---|---|
| T | Bus clock period (ipg_clk_ata) | peripheral clock frequency |
| ti_ds | Set-up time ata_data to ata_iordy edge (UDMA-in only)<br>UDMA0<br>UDMA1<br>UDMA2, UDMA3<br>UDMA4<br>UDMA5 | <br>15 ns<br>10 ns<br>7 ns<br>5 ns<br>4 ns |
| ti_dh | Hold time ata_iordy edge to ata_data (UDMA-in only)<br>UDMA0, UDMA1, UDMA2, UDMA3, UDMA4<br>UDMA5 | <br>5.0 ns<br>4.6 ns |
| tco | Propagation delay bus clock L-to-H to ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data, ata_buffer_en | 12.0 ns |
| tsu | Set-up time ata_data to bus clock L-to-H | 8.5 ns |
| tsui | Set-up time ata_iordy to bus clock H-to-L | 8.5 ns |
| thi | Hold time ata_iordy to bus clock H to L | 2.5 ns |
| tskew1 | Max difference in propagation delay bus clock L-to-H to any of following signals ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en | 7 ns |
| tskew2 | Max difference in buffer propagation delay for any of following signals ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en | transceiver |
| tskew3 | Max difference in buffer propagation delay for any of following signals ata_iordy, ata_data (read) | transceiver |
| tbuf | Max buffer propagation delay | transceiver |
| tcable1 | Cable propagation delay for ata_data | cable |
| tcable2 | Cable propagation delay for control signals ata_dior, ata_diow, ata_iordy, ata_dmack | cable |
| tskew4 | Max difference in cable propagation delay between ata_iordy and ata_data (read) | cable |
| tskew5 | Max difference in cable propagation delay between (ata_dior, ata_diow, ata_dmack) and ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_data(write) | cable |
| tskew6 | Max difference in cable propagation delay without accounting for ground bounce | cable |

1 Values provided where applicable.

### 4.3.5.2 PIO Mode Timing

Figure 10 shows timing for PIO read, and Table 24 lists the timing parameters for PIO read.

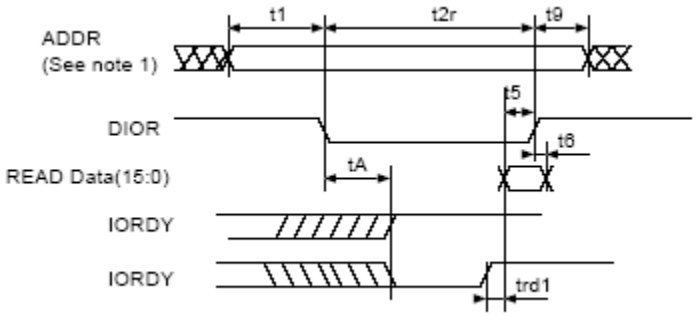



**Figure 10. PIO Read Timing Diagram**

**Table 24. PIO Read Timing Parameters**

| ATA Parameter | Parameter from Figure 10 | Value | Controlling Variable |
|---|---|---|---|
| t1 | t1 | t1 (min) = time_1 * T – (tskew1 + tskew2 + tskew5) | time_1 |
| t2 | t2r | t2 min) = time_2r * T – (tskew1 + tskew2 + tskew5) | time_2r |
| t9 | t9 | t9 (min) = time_9 * T – (tskew1 + tskew2 + tskew6) | time_3 |
| t5 | t5 | t5 (min) = tco + tsu + tbuf + tbuf + tcable1 + tcable2 | If not met, increase time_2 |
| t6 | t6 | 0 | — |
| tA | tA | tA (min) = (1.5 + time_ax) * T – (tco + tsui + tcable2 + tcable2 + 2*tbuf) | time_ax |
| trd | trd1 | trd1 (max) = (–trd) + (tskew3 + tskew4)<br>trd1 (min) = (time_pio_rdx – 0.5)*T – (tsu + thi)<br>(time_pio_rdx – 0.5) * T > tsu + thi + tskew3 + tskew4 | time_pio_rdx |
| t0 | — | t0 (min) = (time_1 + time_2 + time_9) * T | time_1, time_2r, time_9 |

Figure 11 shows timing for PIO write, and Table 25 lists the timing parameters for PIO write.

**Table 29. CSPI Interface Timing Parameters**

| ID | Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|---|
| CS1 | SCLK Cycle Time | $t_{clk}$ | 60 | — | ns |
| CS2 | SCLK High or Low Time | $t_{SW}$ | 30 | — | ns |
| CS3 | SCLK Rise or Fall | $t_{RISE/FALL}$ | — | 7.6 | ns |
| CS4 | SSx pulse width | $t_{CSLH}$ | 25 | — | ns |
| CS5 | SSx Lead Time (CS setup time) | $t_{SCS}$ | 25 | — | ns |
| CS6 | SSx Lag Time (CS hold time) | $t_{HCS}$ | 25 | — | ns |
| CS7 | Data Out Setup Time | $t_{Smosi}$ | 5 | — | ns |
| CS8 | Data Out Hold Time | $t_{Hmosi}$ | 5 | — | ns |
| CS9 | Data In Setup Time | $t_{Smiso}$ | 6 | — | ns |
| CS10 | Data In Hold Time | $t_{Hmiso}$ | 5 | — | ns |
| CS11 | $\overline{\text{SPI\_RDY}}$ Setup Time[1] | $t_{SRDY}$ | — | — | ns |

1 SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

## 4.3.8 DPLL Electrical Specifications

The three PLL's of the MCIMX31 (MCU, USB, and Serial PLL) are all based on same DPLL design. The characteristics provided herein apply to all of them, except where noted explicitly. The PLL characteristics are provided based on measurements done for both sources—external clock source (CKIH), and FPM (Frequency Pre-Multiplier) source.

### 4.3.8.1 Electrical Specifications

Table 30 lists the DPLL specification.

**Table 30. DPLL Specifications**

| Parameter | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|
| CKIH frequency | 15 | 26[1] | 75[2] | MHz | — |
| CKIL frequency<br>(Frequency Pre-multiplier (FPM) enable mode) | — | 32; 32.768, 38.4 | — | kHz | FPM lock time ≈ 480 µs. |
| Predivision factor (PD bits) | 1 | — | 16 | — | — |
| PLL reference frequency range after Predivider | 15 | — | 35 | MHz | 15 ≤ CKIH frequency/PD ≤ 35 MHz<br>15 ≤ FPM output/PD ≤ 35 MHz |
| PLL output frequency range:<br>MPLL and SPLL<br>UPLL | <br>52<br>190 | — | <br>532<br>240 | MHz | — |
| Maximum allowed reference clock phase noise. | — | — | ± 100 | ps | — |
| Frequency lock time<br>(FOL mode or non-integer MF) | — | — | 398 | — | Cycles of divided reference clock. |

**Table 30. DPLL Specifications (continued)**

| Parameter | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|
| Phase lock time | — | — | 100 | µs | In addition to the frequency |
| Maximum allowed PLL supply voltage ripple | — | — | 25 | mV | $F_{modulation}$ < 50 kHz |
| Maximum allowed PLL supply voltage ripple | — | — | 20 | mV | 50 kHz < $F_{modulation}$ < 300 kHz |
| Maximum allowed PLL supply voltage ripple | — | — | 25 | mV | $F_{modulation}$ > 300 kHz |
| PLL output clock phase jitter | — | — | 5.2 | ns | Measured on CLKO pin |
| PLL output clock period jitter | — | — | 420 | ps | Measured on CLKO pin |

1 The user or board designer must take into account that the use of a frequency other than 26 MHz would require adjustment to the DPTC–DVFS table, which is incorporated into operating system code.

2 The PLL reference frequency must be ≤ 35 MHz. Therefore, for frequencies between 35 MHz and 70 MHz, program the predivider to divide by 2 or more. If the CKIH frequency is above 70 MHz, program the predivider to 3 or more. For PD bit description, see the reference manual.

## 4.3.9 EMI Electrical Specifications

This section provides electrical parametrics and timings for EMI module.

### 4.3.9.1 NAND Flash Controller Interface (NFC)

The NFC supports normal timing mode, using two flash clock cycles for one access of $\overline{RE}$ and $\overline{WE}$. AC timings are provided as multiplications of the clock cycle and fixed delay. Figure 22, Figure 23, Figure 24, and Figure 25 depict the relative timing requirements among different signals of the NFC at module level, for normal mode, and Table 31 lists the timing parameters.

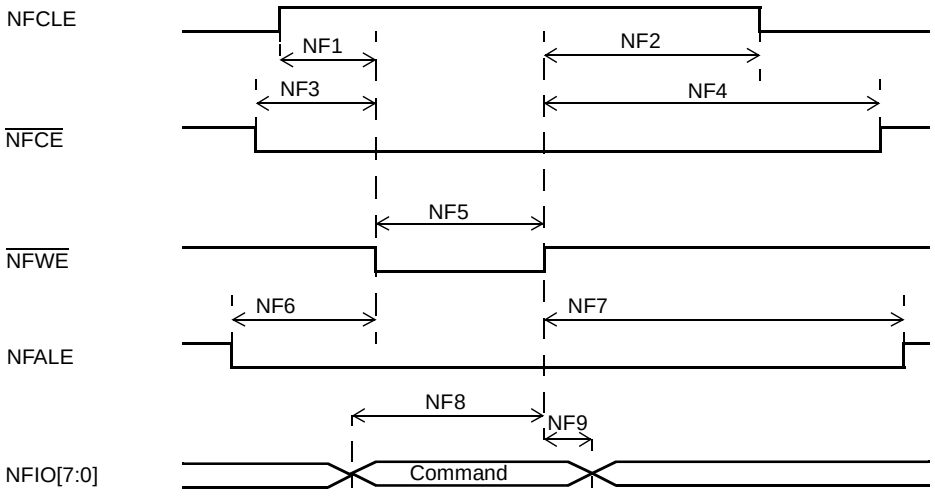



**Figure 22. Command Latch Cycle Timing Diagram**

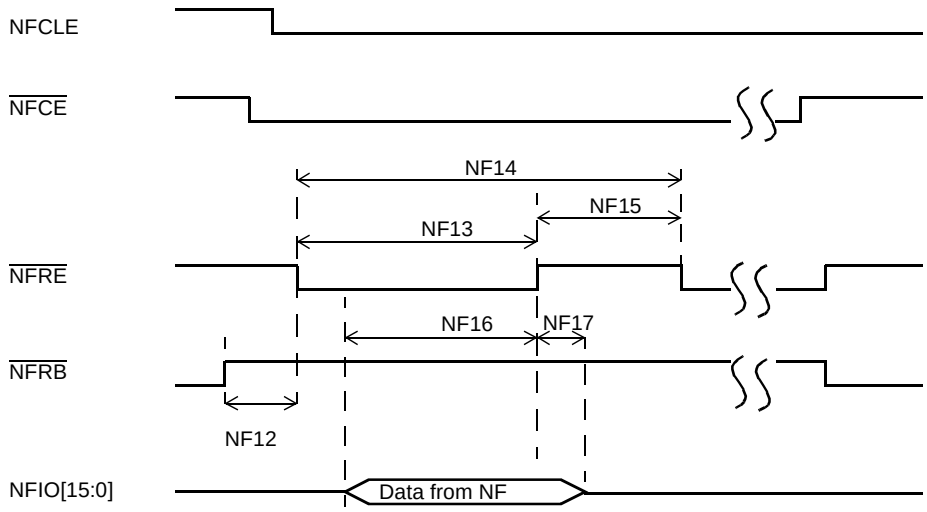



**Figure 25. Read Data Latch Cycle Timing Diagram**

**Table 31. NFC Timing Parameters[1]**

| ID | Parameter | Symbol | Timing T = NFC Clock Cycle[2] | | Example Timing for NFC Clock ≈ 33 MHz T = 30 ns | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| NF1 | NFCLE Setup Time | tCLS | T–1.0 ns | — | 29 | — | ns |
| NF2 | NFCLE Hold Time | tCLH | T–2.0 ns | — | 28 | — | ns |
| NF3 | $\overline{\text{NFCE}}$ Setup Time | tCS | T–1.0 ns | — | 29 | — | ns |
| NF4 | $\overline{\text{NFCE}}$ Hold Time | tCH | T–2.0 ns | — | 28 | — | ns |
| NF5 | $\overline{\text{NF\_WP}}$ Pulse Width | tWP | T–1.5 ns | | 28.5 | | ns |
| NF6 | NFALE Setup Time | tALS | T | — | 30 | — | ns |
| NF7 | NFALE Hold Time | tALH | T–3.0 ns | — | 27 | — | ns |
| NF8 | Data Setup Time | tDS | T | — | 30 | — | ns |
| NF9 | Data Hold Time | tDH | T–5.0 ns | — | 25 | — | ns |
| NF10 | Write Cycle Time | tWC | 2T | | 60 | | ns |
| NF11 | $\overline{\text{NFWE}}$ Hold Time | tWH | T–2.5 ns | | 27.5 | | ns |
| NF12 | Ready to $\overline{\text{NFRE}}$ Low | tRR | 6T | — | 180 | — | ns |
| NF13 | $\overline{\text{NFRE}}$ Pulse Width | tRP | 1.5T | — | 45 | — | ns |
| NF14 | READ Cycle Time | tRC | 2T | — | 60 | — | ns |
| NF15 | $\overline{\text{NFRE}}$ High Hold Time | tREH | 0.5T–2.5 ns | | 12.5 | — | ns |
| NF16 | Data Setup on READ | tDSR | N/A | | 10 | — | ns |
| NF17 | Data Hold on READ | tDHR | N/A | | 0 | — | ns |

1 The flash clock maximum frequency is 50 MHz.

2 Subject to DPLL jitter specification on Table 30, "DPLL Specifications," on page 35.

**NOTE**

High is defined as 80% of signal value and low is defined as 20% of signal value.

Timing for HCLK is 133 MHz and internal NFC clock (flash clock) is approximately 33 MHz (30 ns). All timings are listed according to this NFC clock frequency (multiples of NFC clock phases), except NF16 and NF17, which are not NFC clock related.

#### 4.3.9.2 Wireless External Interface Module (WEIM)

All WEIM output control signals may be asserted and deasserted by internal clock related to BCLK rising edge or falling edge according to corresponding assertion/negation control fields. Address always begins related to BCLK falling edge but may be ended both on rising and falling edge in muxed mode according to control register configuration. Output data begins related to BCLK rising edge except in muxed mode where both rising and falling edge may be used according to control register configuration. Input data, $\overline{\text{ECB}}$ and $\overline{\text{DTACK}}$ all captured according to BCLK rising edge time. Figure 26 depicts the timing of the WEIM module, and Table 32 lists the timing parameters.

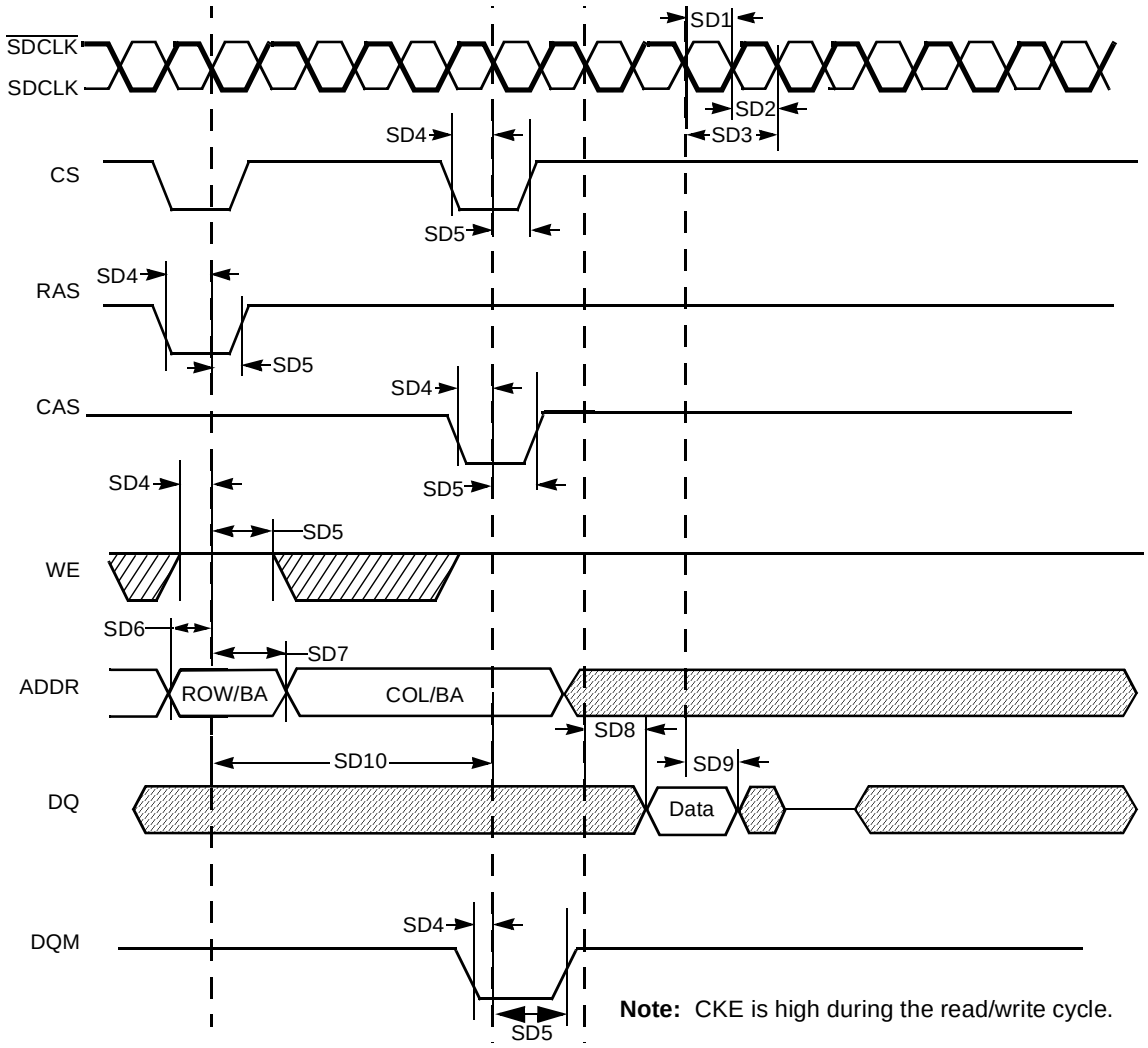



**Figure 33. SDRAM Read Cycle Timing Diagram**

**Table 33. DDR/SDR SDRAM Read Cycle Timing Parameters**

| ID | Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| SD1 | SDRAM clock high-level width | tCH | 3.4 | 4.1 | ns |
| SD2 | $\overline{\text{SDRAM clock low-level width}}$ | tCL | 3.4 | 4.1 | ns |
| SD3 | SDRAM clock cycle time | tCK | 7.5 | — | ns |
| SD4 | CS, RAS, CAS, WE, DQM, CKE setup time | tCMS | 2.0 | — | ns |
| SD5 | CS, RAS, CAS, WE, DQM, CKE hold time | tCMH | 1.8 | — | ns |
| SD6 | Address setup time | tAS | 2.0 | — | ns |
| SD7 | Address hold time | tAH | 1.8 | — | ns |
| SD8 | SDRAM access time | tAC | — | 6.47 | ns |

- DISPB_D3_DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.

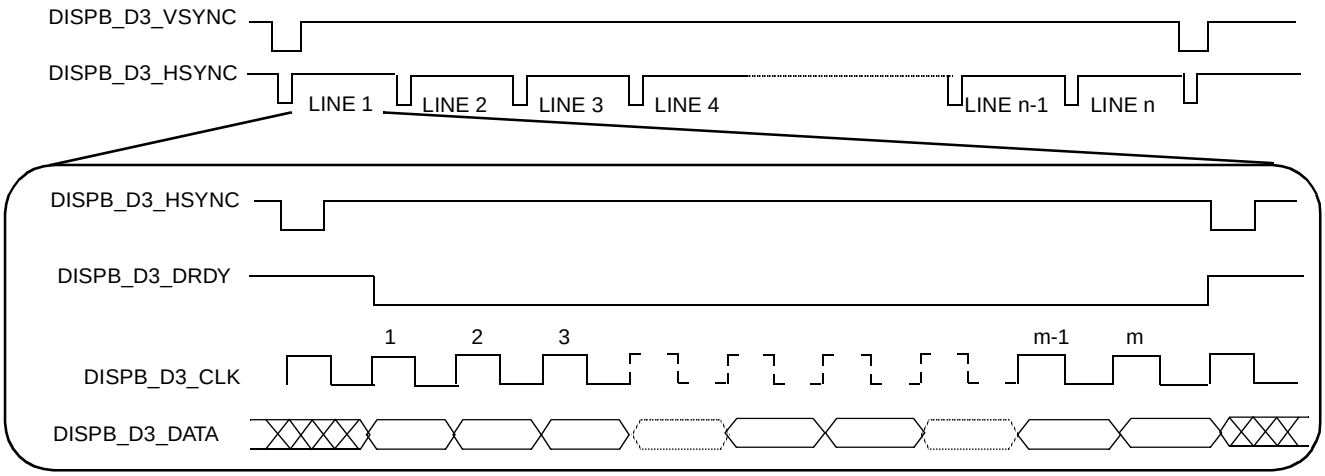



**Figure 45. Interface Timing Diagram for TFT (Active Matrix) Panels**

### 4.3.15.2.2 Interface to Active Matrix TFT LCD Panels, Electrical Characteristics

Figure 46 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All figure parameters shown are programmable. The timing images correspond to inverse polarity of the DISPB_D3_CLK signal and active-low polarity of the DISPB_D3_HSYNC, DISPB_D3_VSYNC and DISPB_D3_DRDY signals.

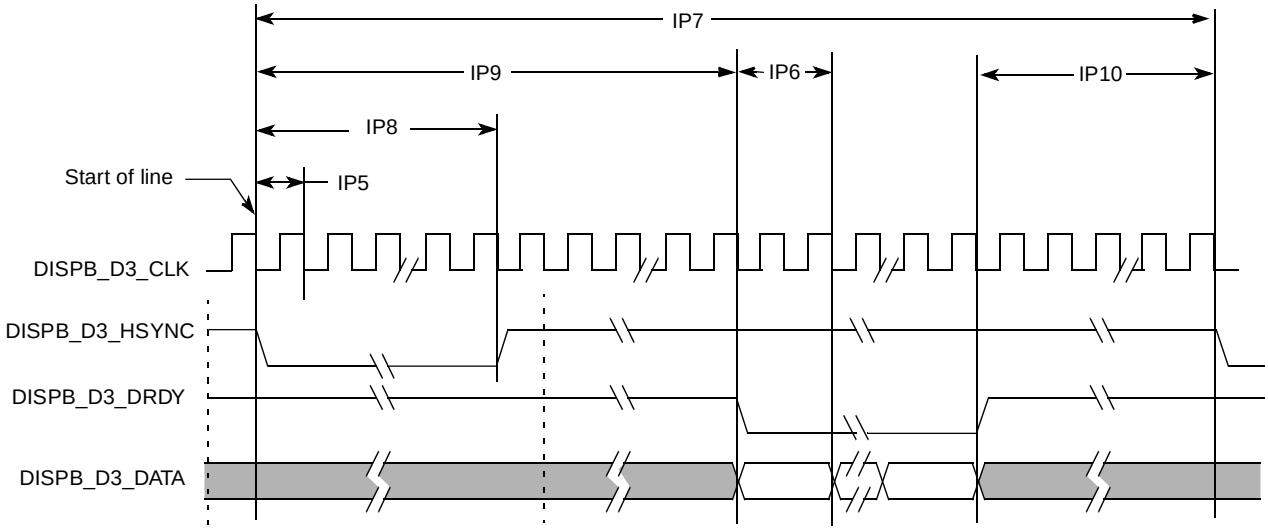



**Figure 46. TFT Panels Timing Diagram—Horizontal Sync Pulse**

Figure 47 depicts the vertical timing (timing of one frame). All figure parameters shown are programmable.

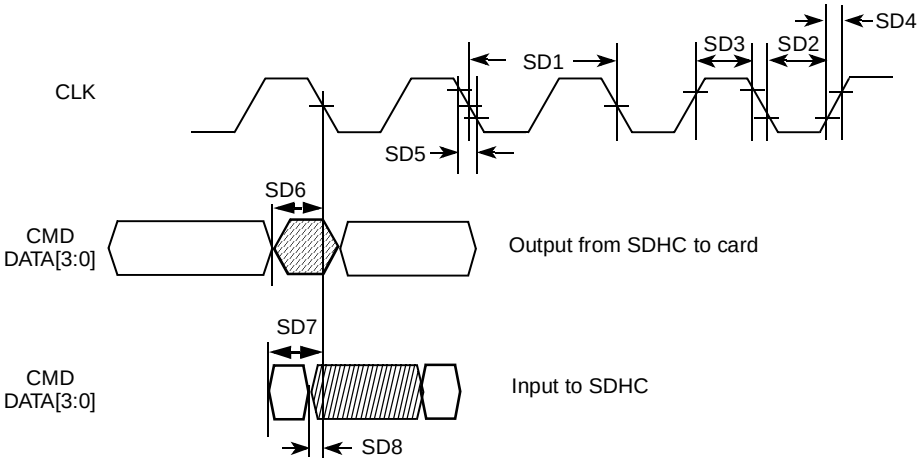



**Figure 71. SDHC Timing Diagram**

**Table 55. SDHC Interface Timing Parameters**

| ID | Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Card Input Clock | | | | | |
| SD1 | Clock Frequency (Low Speed) | $f_{PP}$[1] | 0 | 400 | kHz |
| | Clock Frequency (SD/SDIO Full Speed) | $f_{PP}$[2] | 0 | 25 | MHz |
| | Clock Frequency (MMC Full Speed) | $f_{PP}$[3] | 0 | 20 | MHz |
| | Clock Frequency (Identification Mode) | $f_{OD}$[4] | 100 | 400 | kHz |
| SD2 | Clock Low Time | $t_{WL}$ | 10 | — | ns |
| SD3 | Clock High Time | $t_{WH}$ | 10 | — | ns |
| SD4 | Clock Rise Time | $t_{TLH}$ | — | 10 | ns |
| SD5 | Clock Fall Time | $t_{THL}$ | — | 10 | ns |
| SDHC Output/Card Inputs CMD, DAT (Reference to CLK) | | | | | |
| SD6 | SDHC output delay | $t_{ODL}$ | –6.5 | 3 | ns |
| SDHC Input/Card Outputs CMD, DAT (Reference to CLK) | | | | | |
| SD7 | SDHC input setup | $t_{IS}$ | — | 18.5 | ns |
| SD8 | SDHC input hold | $t_{IH}$ | — | –11.5 | ns |

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 V–3.3 V.

2 In normal data transfer mode for SD/SDIO card, clock frequency can be any value between 0 MHz–25 MHz.

3 In normal data transfer mode for MMC card, clock frequency can be any value between 0 MHz–20 MHz.

4 In card identification mode, card clock must be 100 kHz–400 kHz, voltage ranges from 2.7 V–3.3 V.

## 4.3.20 SIM Electrical Specifications

Each SIM card interface consist of a total of 12 pins (for 2 separate ports of 6 pins each. Mostly one port with 5 pins is used).

The interface is meant to be used with synchronous SIM cards. This means that the SIM module provides a clock for the SIM card to use. The frequency of this clock is normally 372 times the data rate on the TX/RX pins, however SIM module can work with CLK equal to 16 times the data rate on TX/RX pins.

There is no timing relationship between the clock and the data. The clock that the SIM module provides to the aim card will be used by the SIM card to recover the clock from the data much like a standard UART. All six (or 5 in case bi-directional TXRX is used) of the pins for each half of the SIM module are asynchronous to each other.

There are no required timing relationships between the signals in normal mode, but there are some in two specific cases: reset and power down sequences.

### 4.3.20.1 General Timing Requirements

Figure 72 shows the timing of the SIM module, and Figure 56 lists the timing parameters.

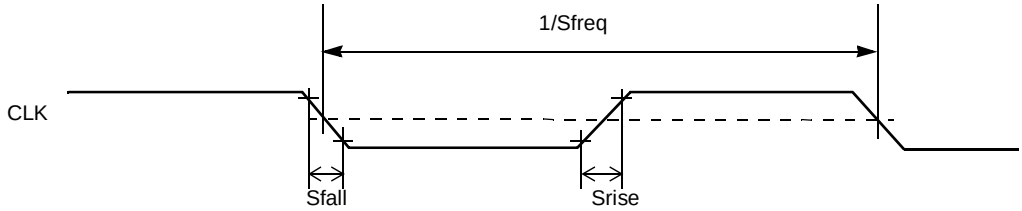



**Figure 72. SIM Clock Timing Diagram**

**Table 56. SIM Timing Specification—High Drive Strength**

| Num | Description | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| 1 | SIM Clock Frequency (CLK)[1] | $S_{freq}$ | 0.01 | 5 (Some new cards may reach 10) | MHz |
| 2 | SIM CLK Rise Time [2] | $S_{rise}$ | — | 20 | ns |
| 3 | SIM CLK Fall Time [3] | $S_{fall}$ | — | 20 | ns |
| 4 | SIM Input Transition Time (RX, SIMPD) | $S_{trans}$ | — | 25 | ns |

1 50% duty cycle clock
2 With C = 50pF
3 With C = 50pF

### 4.3.20.2 Reset Sequence

#### 4.3.20.2.1 Cards with Internal Reset

The sequence of reset for this kind of SIM Cards is as follows (see Figure 73):

- After powerup, the clock signal is enabled on SGCLK (time T0)
- After 200 clock cycles, RX must be high.
- The card must send a response on RX acknowledging the reset between 400 and 40000 clock cycles after T0.

## 4.3.21 SJC Electrical Specifications

This section details the electrical characteristics for the SJC module. Figure 76 depicts the SJC test clock input timing. Figure 77 depicts the SJC boundary scan timing, Figure 78 depicts the SJC test access port, Figure 79 depicts the SJC $\overline{\text{TRST}}$ timing, and Table 58 lists the SJC timing parameters.

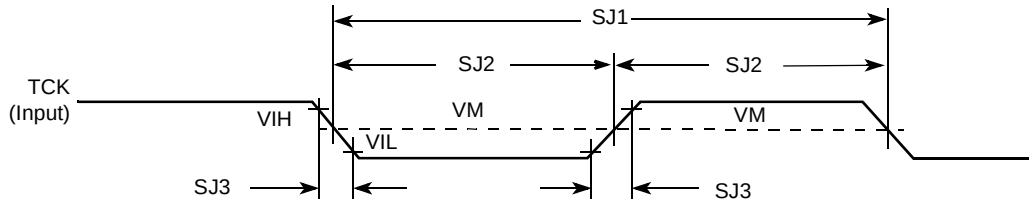



**Figure 76. Test Clock Input Timing Diagram**

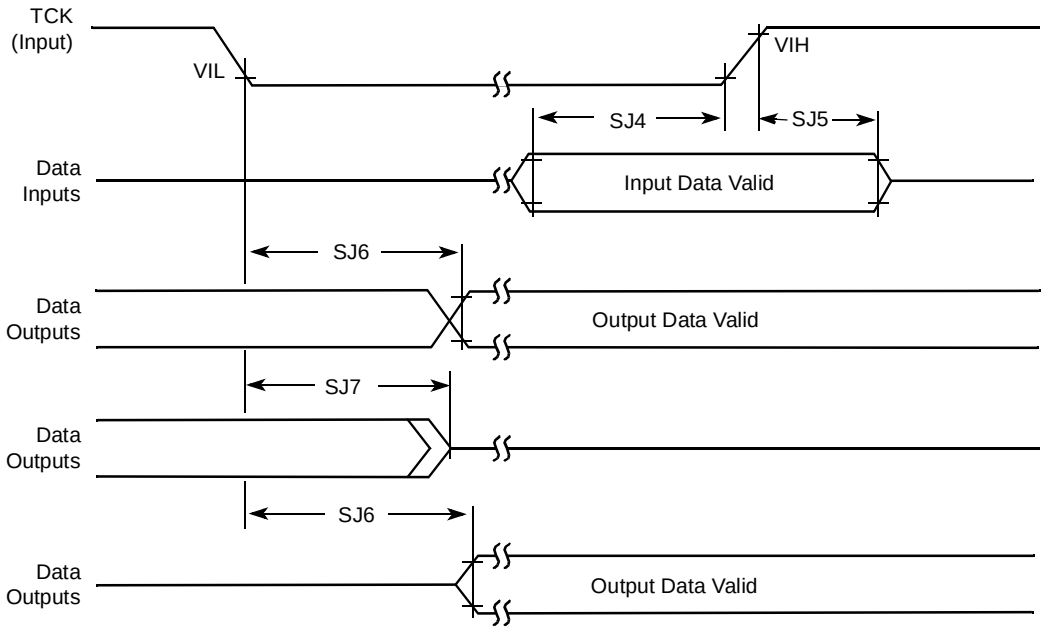



**Figure 77. Boundary Scan (JTAG) Timing Diagram**

### 4.3.22.2 SSI Receiver Timing with Internal Clock

Figure 81 depicts the SSI receiver timing with internal clock, and Table 60 lists the timing parameters.

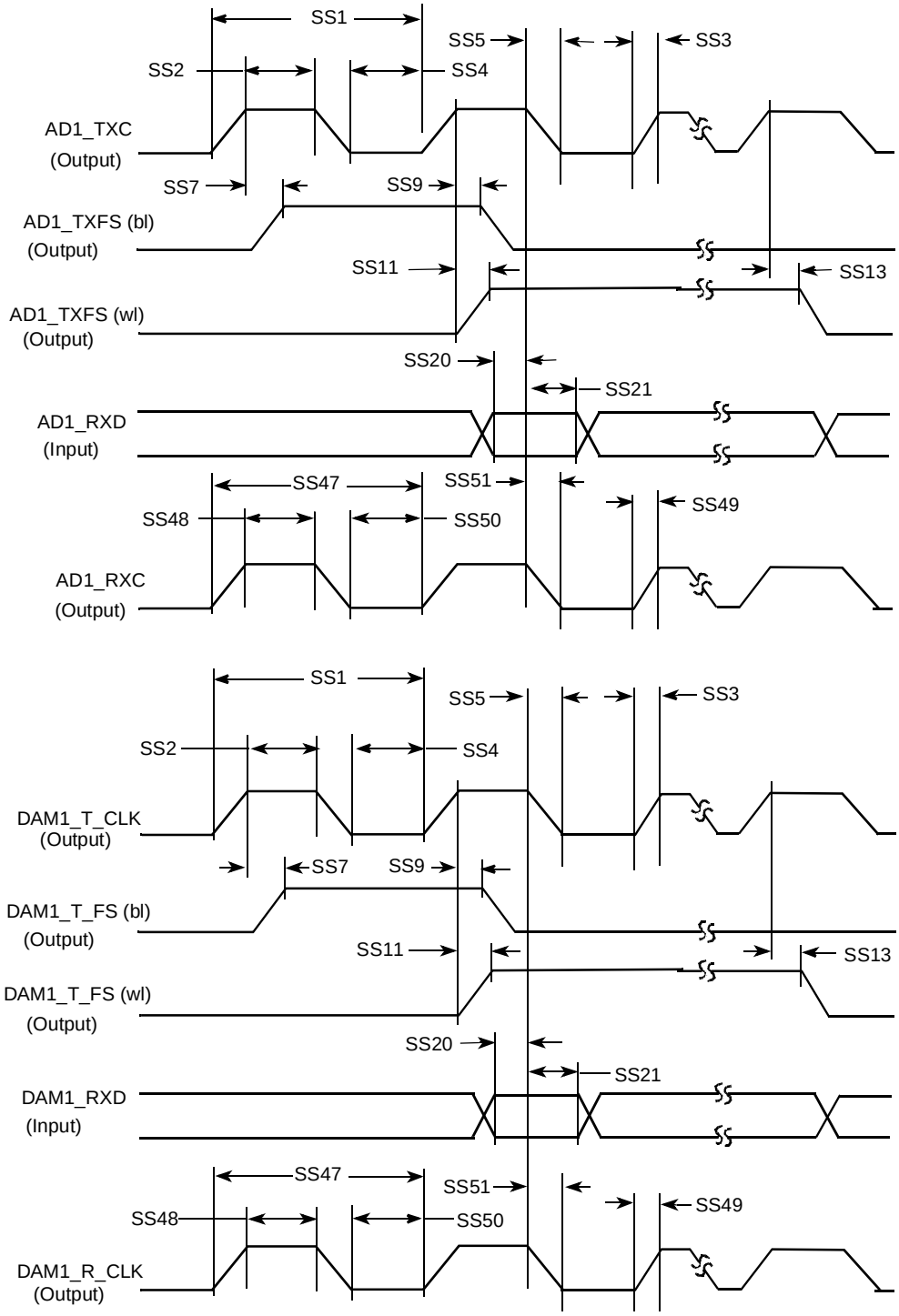
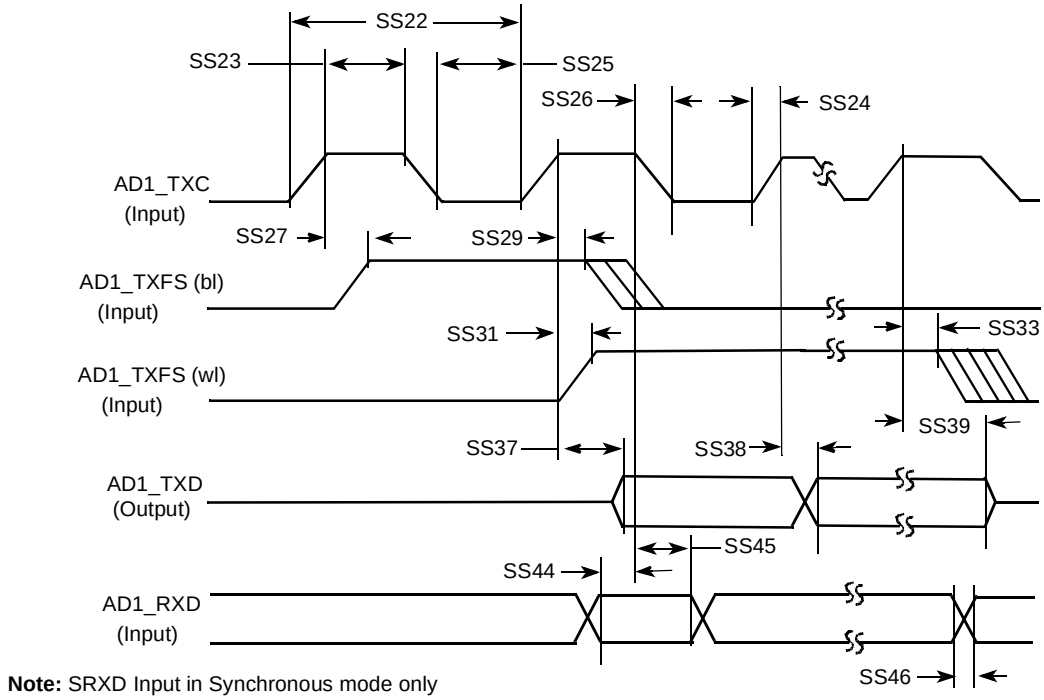


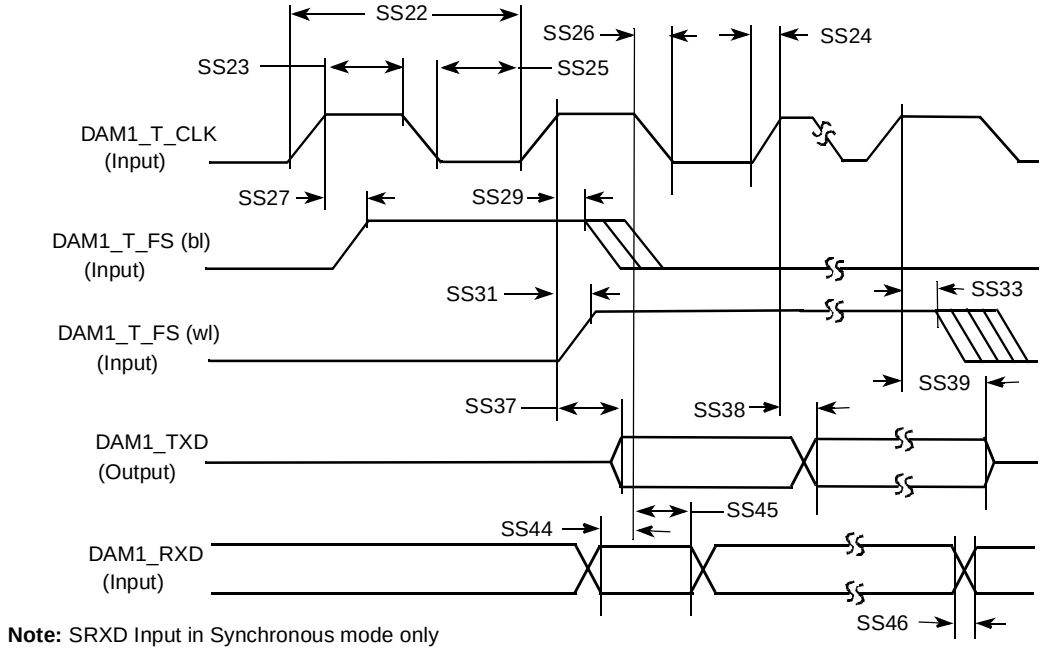

**Figure 81. SSI Receiver with Internal Clock Timing Diagram**

### 4.3.22.3 SSI Transmitter Timing with External Clock

Figure 82 depicts the SSI transmitter timing with external clock, and Table 61 lists the timing parameters.




**Note:** SRXD Input in Synchronous mode only




**Note:** SRXD Input in Synchronous mode only

**Figure 82. SSI Transmitter with External Clock Timing Diagram**

### 5.1.3.2 BGA Signal ID by Ball Grid Location–14 x 14 0.5 mm

Table 65 shows the device connection list for signals only, alpha-sorted by signal identification.

**Table 65. 14 x 14 BGA Signal ID by Ball Grid Location**

| Signal ID | Ball Location |
|---|---|
| A0 | AD6 |
| A1 | AF5 |
| A10 | AF18 |
| A11 | AC3 |
| A12 | AD3 |
| A13 | AD4 |
| A14 | AF17 |
| A15 | AF16 |
| A16 | AF15 |
| A17 | AF14 |
| A18 | AF13 |
| A19 | AF12 |
| A2 | AB5 |
| A20 | AF11 |
| A21 | AF10 |
| A22 | AF9 |
| A23 | AF8 |
| A24 | AF7 |
| A25 | AF6 |
| A3 | AE4 |
| A4 | AA3 |
| A5 | AF4 |
| A6 | AB3 |
| A7 | AE3 |
| A8 | AD5 |
| A9 | AF3 |
| ATA_CS0 | J6 |
| ATA_CS1 | F2 |
| ATA_DIOR | E2 |
| ATA_DIOW | H6 |
| ATA_DMACK | F1 |
| $\overline{\text{ATA\_RESET}}$ | H3 |
| BATT_LINE | F7 |
| BCLK | AB26 |
| BOOT_MODE0 | F20 |
| BOOT_MODE1 | C21 |
| BOOT_MODE2 | D24 |
| BOOT_MODE3 | C22 |
| BOOT_MODE4 | D26 |
| CAPTURE | A22 |
| CAS | AD20 |
| CE_CONTROL | A14 |
| CKIH | F24 |

| Signal ID | Ball Location |
|---|---|
| CKIL | H21 |
| CLKO | C23 |
| CLKSS | G26 |
| COMPARE | G18 |
| CONTRAST | R24 |
| CS0 | AE23 |
| CS1 | AF23 |
| CS2 | AE21 |
| CS3 | AD22 |
| CS4 | AF24 |
| CS5 | AF22 |
| CSI_D10 | M24 |
| CSI_D11 | L26 |
| CSI_D12 | M21 |
| CSI_D13 | M25 |
| CSI_D14 | M20 |
| CSI_D15 | M26 |
| CSI_D4 | L21 |
| CSI_D5 | K25 |
| CSI_D6 | L24 |
| CSI_D7 | K26 |
| CSI_D8 | L20 |
| CSI_D9 | L25 |
| CSI_HSYNC | K20 |
| CSI_MCLK | K24 |
| CSI_PIXCLK | J26 |
| CSI_VSYNC | J25 |
| CSPI1_MISO | P7 |
| CSPI1_MOSI | P2 |
| CSPI1_SCLK | N2 |
| CSPI1_SPI_RDY | N3 |
| CSPI1_SS0 | P3 |
| CSPI1_SS1 | P1 |
| CSPI1_SS2 | P6 |
| CSPI2_MISO | A4 |
| CSPI2_MOSI | E3 |
| CSPI2_SCLK | C7 |
| CSPI2_SPI_RDY | B6 |
| CSPI2_SS0 | B5 |
| CSPI2_SS1 | C6 |
| CSPI2_SS2 | A5 |
| CSPI3_MISO | G3 |
| CSPI3_MOSI | D2 |

**Table 68. 19 x 19 BGA Signal ID by Ball Grid Location (continued)**

| Signal ID | Ball Location |
|---|---|
| BOOT_MODE0 | F17 |
| BOOT_MODE1 | C21 |
| BOOT_MODE2 | D20 |
| BOOT_MODE3 | F18 |
| BOOT_MODE4 | E20 |
| CAPTURE | D18 |
| CAS | AA20 |
| CE_CONTROL | D12 |
| CKIH | F23 |
| CSPI3_SCLK | H7 |
| CSPI3_SPI_RDY | F4 |
| CTS1 | A9 |
| CTS2 | C12 |
| D0 | U6 |
| D1 | W4 |
| D10 | V1 |
| D11 | U4 |
| D12 | U3 |
| D13 | R6 |
| D14 | U2 |
| D15 | U1 |
| D2 | W3 |
| D3 | V4 |
| D3_CLS | P20 |
| D3_REV | P21 |
| D3_SPL | N17 |
| D4 | T7 |
| D5 | W2 |
| D6 | V3 |
| D7 | W1 |
| D8 | T6 |
| D9 | V2 |
| DCD_DCE1 | C10 |
| DCD_DTE1 | D11 |
| $\overline{DE}$ | D16 |
| DQM0 | AB19 |
| DQM1 | Y16 |
| DQM2 | AA18 |
| DQM3 | AB18 |
| DRDY0 | M17 |
| DSR_DCE1 | B10 |
| DSR_DTE1 | A11 |
| DTR_DCE1 | F10 |
| DTR_DCE2 | C11 |
| DTR_DTE1 | A10 |
| DVFS0 | E22 |
| CSPI2_MISO | B4 |
| CSPI2_MOSI | D5 |
| CSPI2_SCLK | B5 |
| CSPI2_SPI_RDY | D6 |
| CSPI2_SS0 | C5 |
| CSPI2_SS1 | A4 |
| CSPI2_SS2 | F7 |
| CSPI3_MISO | D2 |
| CSPI3_MOSI | E4 |
| GPIO1_3 | G20 |
| GPIO1_4 | D21 |
| GPIO1_5 (PWR RDY) | D19 |
| GPIO1_6 | G18 |
| GPIO3_0 | G23 |
| GPIO3_1 | K17 |
| HSYNC | L23 |
| I2C_CLK | J18 |
| I2C_DAT | K18 |
| IOIS16 | J7 |
| KEY_COL0 | A15 |
| KEY_COL1 | B15 |
| KEY_COL2 | D14 |
| KEY_COL3 | C15 |
| KEY_COL4 | F13 |
| KEY_COL5 | A16 |
| KEY_COL6 | B16 |
| KEY_COL7 | A17 |
| KEY_ROW0 | A13 |
| KEY_ROW1 | B13 |
| KEY_ROW2 | C13 |
| KEY_ROW3 | A14 |
| KEY_ROW4 | F12 |
| KEY_ROW5 | D13 |
| KEY_ROW6 | B14 |
| KEY_ROW7 | C14 |
| L2PG | See VPG1 |
| LBA | V17 |
| LCS0 | M22 |
| LCS1 | N23 |
| LD0 | R23 |
| LD1 | R22 |
| LD10 | U22 |
| LD11 | R18 |
| LD12 | U20 |
| LD13 | V23 |
| LD14 | V22 |