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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	79
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 17x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4n16ca-cu

Table 4-4. SAM4N8/16 100-ball VFBGA Pinout

A1	ADVREFP	C6	PC9	F1	VDDOUT	H6	PA12/PGMD0
A2	VDDPLL	C7	TMS/SWDIO/PB6	F2	PA18/PGMD6/AD1	H7	PA9/PGMM1
A3	PB9/PGMCK/XIN	C8	PA1/PGMEN1	F3	PA17/PGMD5/AD0	H8	VDDCORE
A4	PB8/XOUT	C9	PA0/PGMEN0	F4	GND	H9	PA6/PGMNOE
A5	JTAGSEL	C10	PC16	F5	GND	H10	PA5/PGMRDY
A6	PB11	D1	PB1/AD5	F6	PC26	J1	PA20/AD3
A7	PB10	D2	PC30	F7	PA4/PGMNCMD	J2	PC12/AD12
A8	PC20	D3	PC31	F8	PA28	J3	PA16/PGMD4
A9	PC19	D4	PC22	F9	TST	J4	PC6
A10	TDO/TRACESWO/ PB5	D5	PC5	F10	PC8	J5	PA24
B1	GND	D6	PA29	G1	PC15/AD11	J6	PA25
B2	PC25	D7	PA30/AD14	G2	PA19/PGMD7/AD2	J7	PA11/PGMM3
B3	PB14	D8	GND	G3	PA21/PGMD9/AD8	J8	VDDCORE
B4	PB13/DAC0	D9	PC14	G4	PA15/PGMD3	J9	VDDCORE
B5	PC23	D10	PC11	G5	PC3	J10	TDI/PB4
B6	PC21	E1	VDDIN	G6	PA10/PGMM2	K1	PA23
B7	TCK/SWCLK/PB7	E2	PB3/AD7	G7	PC1	K2	PC0
B8	PA31	E3	PB2/AD6	G8	PC28	K3	PC7
B9	PC18	E4	GND	G9	NRST	K4	PA13/PGMD1
B10	PC17	E5	GND	G10	PA27	K5	PA26
C1	PB0/AD4	E6	GND	H1	PC13/AD10	K6	PC2
C2	PC29/AD13	E7	VDDIO	H2	PA22/AD9	K7	VDDIO
C3	PC24	E8	PC10	H3	PC27	K8	VDDIO
C4	ERASE/PB12	E9	PA2/PGMEN2	H4	PA14/PGMD2	K9	PA8/XOUT32/ PGMM0
C5	VDDCORE	E10	PA3	H5	PC4	K10	PA7/XIN32/ PGMNVALID

4.10 48-lead LQFP and QFN Pinout

Table 4-6. 48-pin SAM4N8 Pinout

1	ADVREFP	13	VDDIO	25	TDI/PB4	37	TDO/TRACESWO/PB5
2	GND	14	PA16/PGMD4	26	PA6/PGMNOE	38	JTAGSEL
3	PB0/AD4	15	PA15/PGMD3	27	PA5/PGMRDY	39	TMS/SWDIO/PB6
4	PB1/AD5	16	PA14/PGMD2	28	PA4/PGMNCMD	40	TCK/SWCLK/PB7
5	PB2/AD6	17	PA13/PGMD1	29	NRST	41	VDDCORE
6	PB3/AD7	18	VDDCORE	30	TST	42	ERASE/PB12
7	VDDIN	19	PA12/PGMD0	31	PA3	43	PB10
8	VDDOUT	20	PA11/PGMM3	32	PA2/PGMEN2	44	PB11
9	PA17/PGMD5/AD0	21	PA10/PGMM2	33	VDDIO	45	XOUT/PB8
10	PA18/PGMD6/AD1	22	PA9/PGMM1	34	GND	46	XIN/P/PB9/GMCK
11	PA19/PGMD7/AD2	23	PA8/XOUT32/PGMM0	35	PA1/PGMEN1	47	VDDIO
12	PA20/AD3	24	PA7/XIN32/PGMNVALID	36	PA0/PGMEN0	48	VDDPLL

Note: The bottom pad of the QFN package must be connected to ground.

6. Input/Output Lines

The SAM4N8/16 has several kinds of input/output (I/O) lines such as general purpose I/Os (GPIO) and system I/Os. GPIOs can have alternate functionality due to multiplexing capabilities of the PIO controllers. The same PIO line can be used whether in I/O mode or by the multiplexed peripheral. System I/Os include pins such as test pins, oscillators, erase or analog inputs.

6.1 General Purpose I/O Lines

GPIO lines are managed by PIO controllers. All I/Os have several input or output modes such as pull-up or pull-down, input Schmitt triggers, multi-drive (open-drain), glitch filters, debouncing or input change interrupt. Programming of these modes is performed independently for each I/O line through the PIO controller user interface. For more details, refer to Section 27. “Parallel Input/Output (PIO) Controller”.

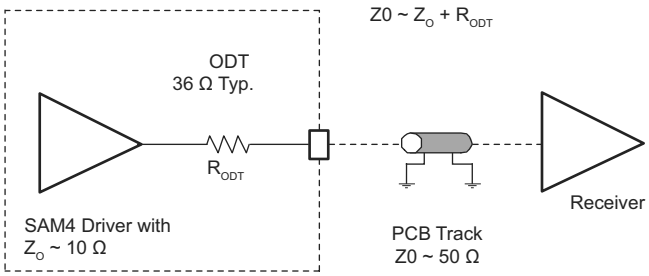
Some GPIOs can have alternate function as analog input. When the GPIO is set in analog mode, all digital features of the I/O are disabled.

The input/output buffers of the PIO lines are supplied through VDDIO power supply rail.

The SAM4N8/16 embeds high-speed pads. See Section 36.10 “AC Characteristics” for more details.

Each I/O line also embeds an ODT (On-Die Termination) (see Figure 6-1). It consists of an internal series resistor termination scheme for impedance matching between the driver output (SAM4N) and the PCB track impedance, preventing signal reflection. The series resistor helps to reduce IOs switching current (di/dt) thereby reducing in turn, EMI. It also decreases overshoot and undershoot (ringing) due to inductance of interconnect between devices or between boards. In conclusion, ODT helps diminish signal integrity issues.

Figure 6-1. On-die Termination



10. Peripherals

10.1 Peripheral Identifiers

Table 10-1 defines the peripheral identifiers of the SAM4N8/16. A peripheral identifier is required for the control of the peripheral interrupt with the Nested Vectored Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 10-1. Peripheral Identifiers

Instance ID	Instance Name	NVIC Interrupt	PMC Clock Control	Instance Description
0	SUPC	X		Supply Controller
1	RSTC	X		Reset Controller
2	RTC	X		Real-time Clock
3	RTT	X		Real-time Timer
4	WDT	X		Watchdog Timer
5	PMC	X		Power Management Controller
6	EFC	X		Enhanced Flash Controller
7	–	–	–	Reserved
8	UART0	X	X	Universal Asynchronous Receiver Transmitter 0
9	UART1	X	X	Universal Asynchronous Receiver Transmitter 1
10	UART2	X	X	Universal Asynchronous Receiver Transmitter 2
11	PIOA	X	X	Parallel I/O Controller A
12	PIOB	X	X	Parallel I/O Controller B
13	PIOC	X	X	Parallel I/O Controller C
14	USART0	X	X	Universal Synchronous Asynchronous Receiver Transmitter 0
15	USART1	X	X	Universal Synchronous Asynchronous Receiver Transmitter 1
16	UART3	X	X	Universal Asynchronous Receiver Transmitter 3
17	USART2	X	X	Universal Synchronous Asynchronous Receiver Transmitter 2
18	–	–	–	Reserved
19	TWI0	X	X	Two-wire Interface 0
20	TWI1	X	X	Two-wire Interface 1
21	SPI	X	X	Serial Peripheral Interface
22	TWI2	X	X	Two-wire Interface 2
23	TC0	X	X	Timer Counter Channel 0
24	TC1	X	X	Timer Counter Channel 1
25	TC2	X	X	Timer Counter Channel 2
26	TC3	X	X	Timer Counter Channel 3
27	TC4	X	X	Timer Counter Channel 4
28	TC5	X	X	Timer Counter Channel 5

11.6.4.1 ADR

Load PC-relative address.

Syntax

```
ADR{cond} Rd, label
```

where:

cond is an optional condition code, see “Conditional Execution” .

Rd is the destination register.

label is a PC-relative expression. See “PC-relative Expressions” .

Operation

ADR determines the address by adding an immediate value to the PC, and writes the result to the destination register.

ADR produces position-independent code, because the address is PC-relative.

If ADR is used to generate a target address for a BX or BLX instruction, ensure that bit[0] of the address generated is set to 1 for correct execution.

Values of *label* must be within the range of –4095 to +4095 from the address in the PC.

Note: The user might have to use the .W suffix to get the maximum offset range or to generate addresses that are not word-aligned. See “Instruction Width Selection” .

Restrictions

Rd must not be SP and must not be PC.

Condition Flags

This instruction does not change the flags.

Examples

```
ADR     R1, TextMessage   ; Write address value of a location labelled as
                          ; TextMessage to R1
```

11.9 System Control Block (SCB)

The System Control Block (SCB) provides system implementation information, and system control. This includes configuration, control, and reporting of the system exceptions.

Ensure that the software uses aligned accesses of the correct size to access the system control block registers:

- Except for the SCB_CFSR and SCB_SHPR1-SCB_SHPR3 registers, it must use aligned word accesses
- For the SCB_CFSR and SCB_SHPR1-SCB_SHPR3 registers, it can use byte or aligned halfword or word accesses.

The processor does not support unaligned accesses to system control block registers.

In a fault handler, to determine the true faulting address:

1. Read and save the MMFAR or SCB_BFAR value.
2. Read the MMARVALID bit in the MMFSR subregister, or the BFARVALID bit in the BFSR subregister. The SCB_MMFAR or SCB_BFAR address is valid only if this bit is 1.

The software must follow this sequence because another higher priority exception might change the SCB_MMFAR or SCB_BFAR value. For example, if a higher priority handler preempts the current fault handler, the other fault might change the SCB_MMFAR or SCB_BFAR value.

17.5 Supply Controller (SUPC) User Interface

The User Interface of the Supply Controller is part of the System Controller User Interface.

17.5.1 System Controller (SYSC) User Interface

Table 17-1. System Controller Registers

Offset	System Controller Peripheral	Name
0x00-0x0c	Reset Controller	RSTC
0x10-0x2C	Supply Controller	SUPC
0x30-0x3C	Real Time Timer	RTT
0x50-0x5C	Watchdog Timer	WDT
0x60-0x8C	Real Time Clock	RTC
0x90-0xDC	General Purpose Backup Register	GPBR
0xE0	Reserved	
0xE4	Write Protect Mode Register	SYSC_WPMR
0xE8-0xF8	Reserved	

17.5.2 Supply Controller (SUPC) User Interface

Table 17-2. Register Mapping

Offset	Register	Name	Access	Reset
0x00	Supply Controller Control Register	SUPC_CR	Write-only	N/A
0x04	Supply Controller Supply Monitor Mode Register	SUPC_SMMR	Read-write	0x0000_0000
0x08	Supply Controller Mode Register	SUPC_MR	Read-write	0x0000_5A00
0x0C	Supply Controller Wake-up Mode Register	SUPC_WUMR	Read-write	0x0000_0000
0x10	Supply Controller Wake-up Inputs Register	SUPC_WUIR	Read-write	0x0000_0000
0x14	Supply Controller Status Register	SUPC_SR	Read-only	0x0000_0000
0x18	Reserved			

22. Bus Matrix (MATRIX)

22.1 Description

The Bus Matrix implements a multi-layer AHB that enables parallel access paths between multiple AHB masters and slaves in a system, which increases the overall bandwidth. Bus Matrix interconnects 3 AHB Masters to 4 AHB Slaves. The normal latency to connect a master to a slave is one cycle except for the default master of the accessed slave which is connected directly (zero cycle latency).

The Bus Matrix user interface also provides a Chip Configuration User Interface with Registers that allow to support application specific features.

22.2 Embedded Characteristics

22.2.1 Matrix Masters

The Bus Matrix of the SAM4N product manages 3 masters, which means that each master can perform an access concurrently with others, to an available slave.

Each master has its own decoder, which is defined specifically for each master. In order to simplify the addressing, all the masters have the same decodings.

Table 22-1. List of Bus Matrix Masters

Master 0	Cortex-M4 Instruction/Data
Master 1	Cortex-M4 System
Master 2	Peripheral DMA Controller (PDC)

22.2.2 Matrix Slaves

The Bus Matrix of the SAM4N product manages 4 slaves. Each slave has its own arbiter, allowing a different arbitration per slave.

Table 22-2. List of Bus Matrix Slaves

Slave 0	Internal SRAM
Slave 1	Internal ROM
Slave 2	Internal Flash
Slave 3	Peripheral Bridge

23.5.4 Transmit Counter Register

Name: PERIPH_TCR

Access: Read-write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
TXCTR							
7	6	5	4	3	2	1	0
TXCTR							

- **TXCTR: Transmit Counter Register**

TXCTR must be set to transmit buffer size.

When a half duplex peripheral is connected to the PDC, RXCTR = TXCTR.

0 = Stops peripheral data transfer to the transmitter

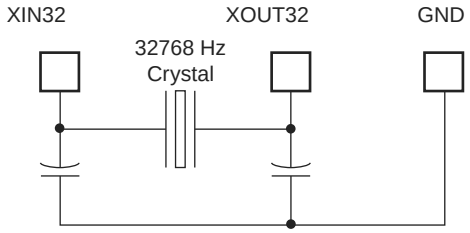
1- 65535 = Starts peripheral data transfer if corresponding channel is active

24.4.2 Slow Clock Crystal Oscillator

The Clock Generator integrates a 32768 Hz low-power oscillator. In order to use this oscillator, the XIN32 and XOUT32 pins must be connected to a 32768 Hz crystal. Two external capacitors must be wired as shown in Figure 24-2. More details are given in the section “DC Characteristics” of the product datasheet.

Note that the user is not obliged to use the Slow Clock Crystal and can use the RC oscillator instead.

Figure 24-2. Typical Slow Clock Crystal Oscillator Connection



The user can select the crystal oscillator to be the source of the slow clock, as it provides a more accurate frequency. The command is made by writing the Supply Controller Control Register (SUPC_CR) with the XTALSEL bit at 1. This results in a sequence which first configures the PIO lines multiplexed with XIN32 and XOUT32 to be driven by the oscillator, then enables the crystal oscillator and then disables the RC oscillator to save power. The switch of the slow clock source is glitch free. The OSCSEL bit of the Supply Controller Status Register (SUPC_SR) tracks the oscillator frequency downstream. It must be read in order to be informed when the switch sequence, initiated when a new value is written in MOSCSEL bit of CKGR_MOR, is done.

Coming back on the RC oscillator is only possible by shutting down the VDDIO power supply. If the user does not need the crystal oscillator, the XIN32 and XOUT32 pins can be left unconnected since by default the XIN32 and XOUT32 system I/O pins are in PIO input mode with pull-up after reset.

The user can also set the crystal oscillator in bypass mode instead of connecting a crystal. In this case, the user has to provide the external clock signal on XIN32. The input characteristics of the XIN32 pin are given in the product electrical characteristics section. In order to set the bypass mode, the OSCBYPASS bit of the Supply Controller Mode Register (SUPC_MR) needs to be set at 1.

The user can set the Slow Clock Crystal Oscillator in bypass mode instead of connecting a crystal. In this case, the user has to provide the external clock signal on XIN32. The input characteristics of the XIN32 pin under these conditions are given in the product electrical characteristics section.

The programmer has to be sure to set the OSCBYPASS bit in the Supply Controller Mode Register (SUPC_MR) and XTALSEL bit in the Supply Controller Control Register (SUPC_CR).

27.7 Parallel Input/Output Controller (PIO) User Interface

Each I/O line controlled by the PIO Controller is associated with a bit in each of the PIO Controller User Interface registers. Each register is 32 bits wide. If a parallel I/O line is not defined, writing to the corresponding bits has no effect. Undefined bits read zero. If the I/O line is notmultiplexed with any peripheral, the I/O line is controlled by the PIO Controller and PIO_PSR returns 1 systematically.

Table 27-2. Register Mapping

Offset	Register	Name	Access	Reset
0x0000	PIO Enable Register	PIO_PER	Write-only	–
0x0004	PIO Disable Register	PIO_PDR	Write-only	–
0x0008	PIO Status Register	PIO_PSR	Read-only	(1)
0x000C	Reserved	–	–	–
0x0010	Output Enable Register	PIO_OER	Write-only	–
0x0014	Output Disable Register	PIO_ODR	Write-only	–
0x0018	Output Status Register	PIO_OSR	Read-only	0x0000 0000
0x001C	Reserved	–	–	–
0x0020	Glitch Input Filter Enable Register	PIO_IFER	Write-only	–
0x0024	Glitch Input Filter Disable Register	PIO_IFDR	Write-only	–
0x0028	Glitch Input Filter Status Register	PIO_IFSR	Read-only	0x0000 0000
0x002C	Reserved	–	–	–
0x0030	Set Output Data Register	PIO_SODR	Write-only	–
0x0034	Clear Output Data Register	PIO_CODR	Write-only	
0x0038	Output Data Status Register	PIO_ODSR	Read-only or(2) Read-write	–
0x003C	Pin Data Status Register	PIO_PDSR	Read-only	(3)
0x0040	Interrupt Enable Register	PIO_IER	Write-only	–
0x0044	Interrupt Disable Register	PIO_IDR	Write-only	–
0x0048	Interrupt Mask Register	PIO_IMR	Read-only	0x00000000
0x004C	Interrupt Status Register(4)	PIO_ISR	Read-only	0x00000000
0x0050	Multi-driver Enable Register	PIO_MDER	Write-only	–
0x0054	Multi-driver Disable Register	PIO_MDDR	Write-only	–
0x0058	Multi-driver Status Register	PIO_MDSR	Read-only	0x00000000
0x005C	Reserved	–	–	–
0x0060	Pull-up Disable Register	PIO_PUDR	Write-only	–
0x0064	Pull-up Enable Register	PIO_PUER	Write-only	–
0x0068	Pad Pull-up Status Register	PIO_PUSR	Read-only	(1)
0x006C	Reserved	–	–	–

- **ARBLST: Arbitration Lost (clear on read)**

This bit is only used in Master mode.

0: Arbitration won.

1: Arbitration lost. Another master of the TWI bus has won the multi-master arbitration. TXCOMP is set at the same time.

- **SCLWS: Clock Wait State (automatically set / reset)**

This bit is only used in Slave mode.

0 = The clock is not stretched.

1 = The clock is stretched. TWI_THR / TWI_RHR buffer is not filled / emptied before the emission / reception of a new character.

SCLWS behavior can be seen in Figure 29-28 on page 558 and Figure 29-29 on page 559.

- **EOSACC: End Of Slave Access (clear on read)**

This bit is only used in Slave mode.

0 = A slave access is being performing.

1 = The Slave Access is finished. End Of Slave Access is automatically set as soon as SVACC is reset.

EOSACC behavior can be seen in Figure 29-30 on page 559 and Figure 29-31 on page 560

- **ENDRX: End of RX buffer**

0 = The Receive Counter Register has not reached 0 since the last write in TWI_RCR or TWI_RNCR.

1 = The Receive Counter Register has reached 0 since the last write in TWI_RCR or TWI_RNCR.

- **ENDTX: End of TX buffer**

0 = The Transmit Counter Register has not reached 0 since the last write in TWI_TCR or TWI_TNCR.

1 = The Transmit Counter Register has reached 0 since the last write in TWI_TCR or TWI_TNCR.

- **RXBUFF: RX Buffer Full**

0 = TWI_RCR or TWI_RNCR have a value other than 0.

1 = Both TWI_RCR and TWI_RNCR have a value of 0.

- **TXBUFE: TX Buffer Empty**

0 = TWI_TCR or TWI_TNCR have a value other than 0.

1 = Both TWI_TCR and TWI_TNCR have a value of 0.

Table 31-11 gives the maximum time-out period for some standard baud rates.

Table 31-11. Maximum Time-out Period

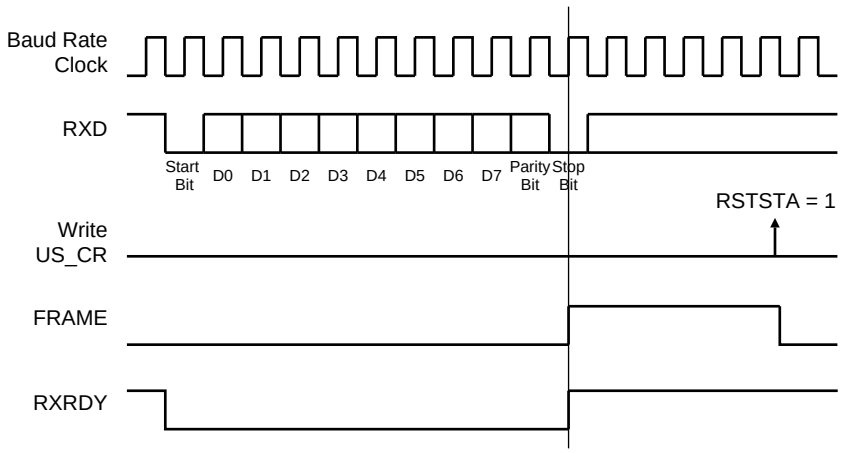
Baud Rate	Bit Time	Time-out
bit/sec	µs	ms
600	1 667	109 225
1 200	833	54 613
2 400	417	27 306
4 800	208	13 653
9 600	104	6 827
14400	69	4 551
19200	52	3 413
28800	35	2 276
38400	26	1 704
56000	18	1 170
57600	17	1 138
200000	5	328

31.7.3.9 Framing Error

The receiver is capable of detecting framing errors. A framing error happens when the stop bit of a received character is detected at level 0. This can occur if the receiver and the transmitter are fully desynchronized.

A framing error is reported on the FRAME bit of the Channel Status Register (US_CSR). The FRAME bit is asserted in the middle of the stop bit as soon as the framing error is detected. It is cleared by writing the Control Register (US_CR) with the RSTSTA bit to 1.

Figure 31-15. Framing Error Status



31.7.3.10 Transmit Break

The user can request the transmitter to generate a break condition on the TXD line. A break condition drives the TXD line low during at least one complete character. It appears the same as a 0x00 character sent with the parity and the stop bits to 0. However, the transmitter holds the TXD line at least during one character until the user requests the break condition to be removed.

31.8.10 USART Interrupt Mask Register (SPI_MODE)

Name: US_IMR (SPI_MODE)

Address: 0x40024010 (0), 0x40028010 (1), 0x4002C010 (2)

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	RXBUFF	TXBUFE	UNRE	TXEMPTY	–
7	6	5	4	3	2	1	0
–	–	OVRE	ENDTX	ENDRX	–	TXRDY	RXRDY

This configuration is relevant only if USART_MODE=0xE or 0xF in “USART Mode Register” on page 633.

- **RXRDY: RXRDY Interrupt Mask**
- **TXRDY: TXRDY Interrupt Mask**
- **OVRE: Overrun Error Interrupt Mask**
- **TXEMPTY: TXEMPTY Interrupt Mask**
- **UNRE: SPI Underrun Error Interrupt Mask**

0: The corresponding interrupt is not enabled.

1: The corresponding interrupt is enabled.

- **ETRGS: External Trigger Status (cleared on read)**

0: External trigger has not occurred since the last read of the Status Register.

1: External trigger has occurred since the last read of the Status Register.

- **ENDRX: End of Receiver Transfer (cleared by writing TC_RCR or TC_RNCR)**

0: The Receive Counter Register has not reached 0 since the last write in TC_RCR[1] or TC_RNCR[1].

1: The Receive Counter Register has reached 0 since the last write in TC_RCR or TC_RNCR.

- **RXBUFF: Reception Buffer Full (cleared by writing TC_RCR or TC_RNCR)**

0: TC_RCR or TC_RNCR have a value other than 0.

1: Both TC_RCR and TC_RNCR have a value of 0.

Note: 1. TC_RCR and TC_RNCR are PDC registers.

- **CLKSTA: Clock Enabling Status**

0: Clock is disabled.

1: Clock is enabled.

- **MTIOA: TIOA Mirror**

0: TIOA is low. If TC_CMRx.WAVE = 0, this means that TIOA pin is low. If TC_CMRx.WAVE = 1, this means that TIOA is driven low.

1: TIOA is high. If TC_CMRx.WAVE = 0, this means that TIOA pin is high. If TC_CMRx.WAVE = 1, this means that TIOA is driven high.

- **MTIOB: TIOB Mirror**

0: TIOB is low. If TC_CMRx.WAVE = 0, this means that TIOB pin is low. If TC_CMRx.WAVE = 1, this means that TIOB is driven low.

1: TIOB is high. If TC_CMRx.WAVE = 0, this means that TIOB pin is high. If TC_CMRx.WAVE = 1, this means that TIOB is driven high.

Table 36-4. Core Power Supply Brownout Detector Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{T-}	Supply Falling Threshold	After trimming	0.98	1.0	1.04	V
V_{hys}	Hysteresis Voltage	—			110	mV
V_{T+}	Supply Rising Threshold	—	0.8	1.0	1.08	V
t_{RST}	Reset Period	V_{DDIO} rising from 0 to 1.2V ± 10%	90	-	320	µs
I_{DDON}	Current Consumption on VDDCORE	Brownout Detector enabled			24	µA
I_{DDOFF}		Brownout Detector disabled			2	
I_{DD33ON}	Current Consumption on VDDIO	Brownout Detector enabled			24	µA
$I_{DD33OFF}$		Brownout Detector disabled			2	
t_{d-}	V_{T-} Detection Propagation Time	VDDCORE = V_{T+} to (V_{T-} - 100 mV)		200	300	ns
t_{START}	Startup Time	From disabled state to enabled state			300	µs

Figure 36-1. Core Brownout Output Waveform

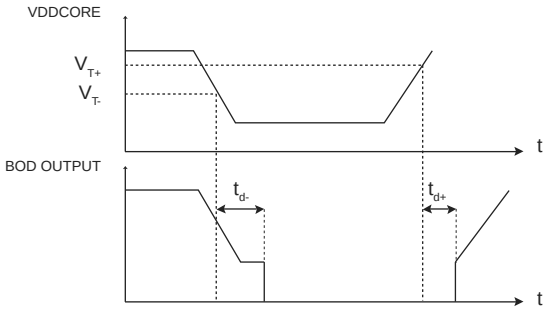


Table 36-5. VDDIO Supply Monitor

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_T	Supply Monitor Threshold	16 selectable steps	1.6		3.4	V
$V_{T(accuracy)}$	Threshold Level Accuracy	-40 to +85°C	-1		+1	%
V_{hys}	Hysteresis Voltage			30	40	mV
I_{DDON}	Current Consumption on VDDCORE	All temperatures, enabled				
		Normal mode			40	µA
		Standby mode			2	µA
I_{DDOFF}		25°C, disabled				
		Normal mode	15.9	18.6	32	µA
		Standby mode	5.9	7.0	10.3	nA
t_{START}	Startup Time	From disabled state to enabled state			300	µs

36.10 AC Characteristics

36.10.1 Master Clock Characteristics

Table 36-40. Master Clock Waveform Parameters

Symbol	Parameter	Conditions	Min	Max	Unit
$1/(t_{CPMCK})$	Master Clock Frequency	VDDCORE @ 1.20V		100	MHz
		VDDCORE @ 1.08V		80	

36.10.2 I/O Characteristics

Criteria used to define the maximum frequency of the I/Os:

- Output duty cycle (40%–60%)
- Minimum output swing: 100 mV to VDDIO - 100 mV
- Minimum output swing: 100 mV to VDDIO - 100 mV
- Addition of rising and falling time inferior to 75% of the period

Table 36-41. I/O Characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
FreqMax1	Pin Group 1 (1) Maximum Output Frequency	10 pF	V_{DDIO} = 1.62V		70	MHz
		25 pF			35	
$PulseminH_1$	Pin Group 1 (1) High Level Pulse Width	10 pF		7.2		ns
		25 pF		14.2		
$PulseminL_1$	Pin Group 1 (1) Low Level Pulse Width	10 pF		7.2		ns
		25 pF		14.2		
FreqMax2	Pin Group 2 (2)Maximum Output Frequency	10 pF			70	MHz
		25 pF			35	
$PulseminH_2$	Pin Group 2 (2) High Level Pulse Width	10 pF		7.2		ns
		25pF		14.2		
$PulseminL_2$	Pin Group 2 (2) Low Level Pulse Width	10 pF		7.2		ns
		25 pF		14.2		
FreqMax3	Pin Group 3(3) Maximum Output Frequency	10 pF			70	MHz
		25 pF			35	
$PulseminH_3$	Pin Group 3 (3) High Level Pulse Width	10 pF		7.2		ns
		25 pF		14.2		
$PulseminL_3$	Pin Group 3 (3) Low Level Pulse Width	10 pF		7.2		ns
		25 pF		14.2		
FreqMax4	Pin Group 4(4)Maximum Output Frequency	10 pF			70	MHz
		25 pF			35	
$PulseminH_4$	Pin Group 4(4) High Level Pulse Width	10 pF		7.2		ns
		25pF		14.2		
$PulseminL_4$	Pin Group 4(4) Low Level Pulse Width	10 pF		7.2		ns
		25 pF		14.2		
FreqMax5	Pin Group 5(5)Maximum Output Frequency	10 pF			70	MHz
		25 pF			35	

36.10.3 SPI Characteristics

Figure 36-14. SPI Master Mode with (CPOL = NCPHA = 0) or (CPOL = NCPHA = 1)

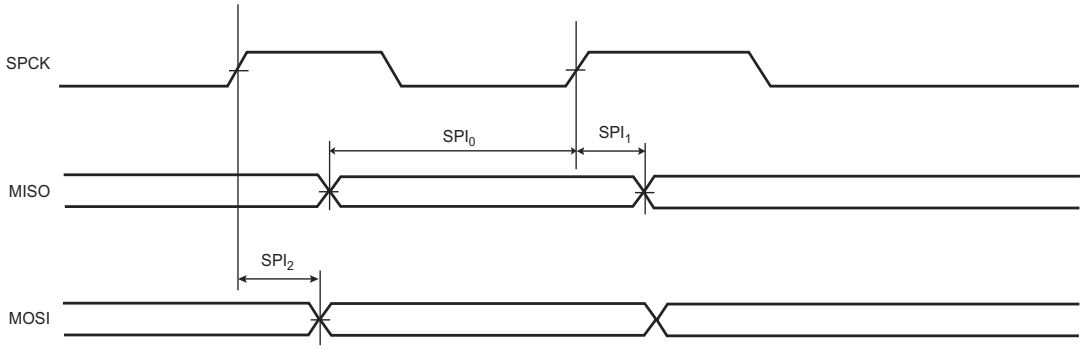


Figure 36-15. SPI Master Mode with (CPOL = 0 and NCPHA = 1) or (CPOL = 1 and NCPHA = 0)

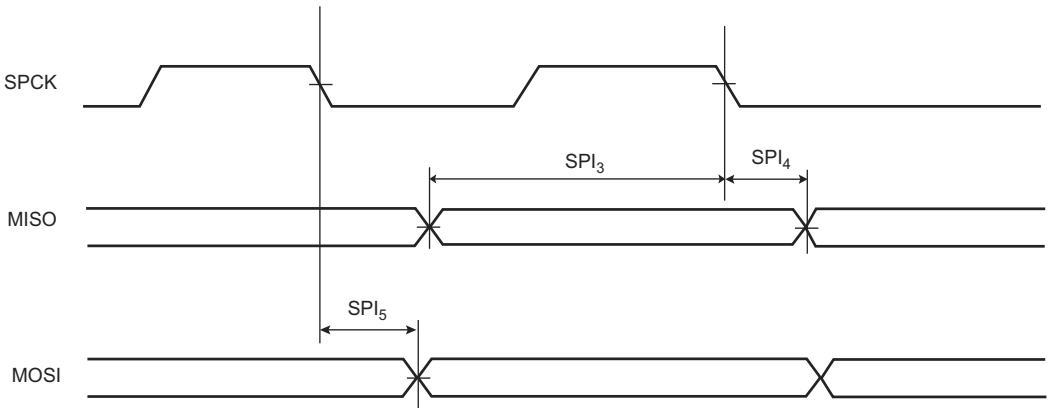


Figure 36-16. SPI Slave Mode with (CPOL = 0 and NCPHA = 1) or (CPOL = 1 and NCPHA = 0)

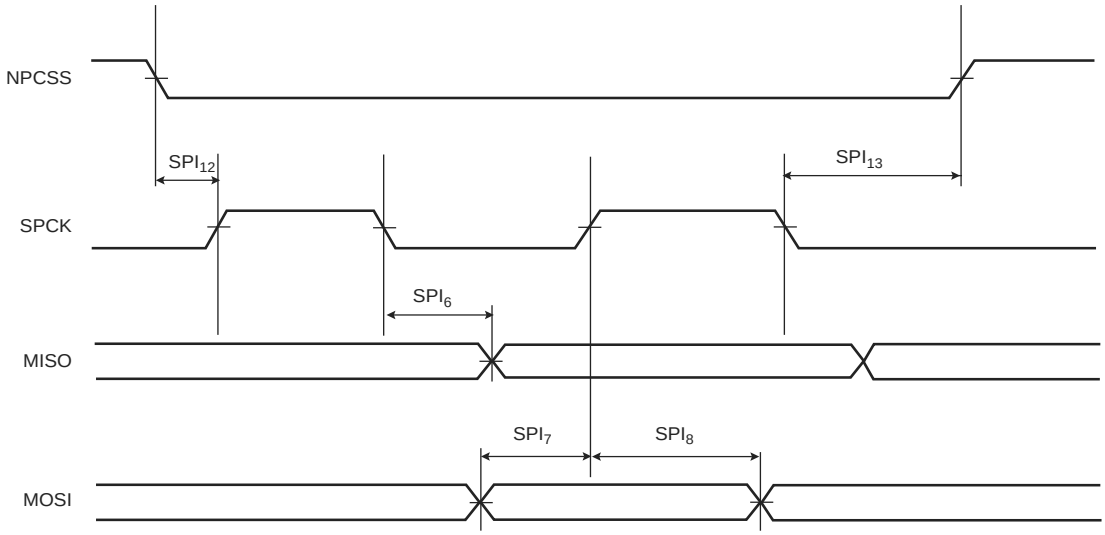


Table 41-1. SAM4N Datasheet Rev. 11158B Revision History (Continued)

Issue Date	Comments
23-Mar-15	Section 32. “Timer Counter (TC)” (cont’d) Section 32.7.5 “TC Counter Value Register”: added notation “IMPORTANT: For 16-bit channels, CV field size is limited to register bits 15:0” Section 32.7.6 “TC Register A”: added notation “IMPORTANT: For 16-bit channels, RA field size is limited to register bits 15:0” Section 32.7.7 “TC Register B”: added notation “IMPORTANT: For 16-bit channels, RB field size is limited to register bits 15:0” Section 32.7.8 “TC Register C”: added notation “IMPORTANT: For 16-bit channels, RC field size is limited to register bits 15:0” Section 32.7.9 “TC Status Register”: updated bit descriptions Section 32.7.14 “TC Block Mode Register”: removed FILTER bit (register bit 19 now reserved); corrected TC2XC2S field configuration values: value 2 is TIOA0 (was TIOA1); value 3 is TIOA1 (was TIOA2) Section 32.7.20 “TC Write Protection Mode Register”: modified register name (was “TC Write Protect Mode Register”); updated WPEN bit description (replaced list of protectable registers with link to Section 32.6.18 “Register Write Protection”) Section 36. “SAM4N Electrical Characteristics” Updated and harmonized parameter symbols Table 36-2 ”DC Characteristics”: replaced two footnotes with single footnote Table 36-3 ”1.2V Voltage Regulator Characteristics”: replaced two footnotes with single footnote in V_{DDIN} conditions; deleted “Cf. External Capacitor Requirements” from CD_{IN} and CD_{OUT} conditions Table 36-4 ”Core Power Supply Brownout Detector Characteristics”: added parameter “Reset Period” Table 36-7 ”Zero-Power-On Reset Characteristics”: modified parameter name “Reset Time-out Period” to “Reset Period” Table 36-20 ”4/8/12 MHz RC Oscillators Characteristics”: updated Startup Time conditions Table 36-21 ”32.768 kHz Crystal Oscillator Characteristics”: added parameter “Allowed Crystal Capacitance Load” Table 36-23 ”3 to 20 MHz Crystal Oscillator Characteristics”: added “pF” unit for “Internal Load Capacitance” parameter; deleted all footnotes Section 36.3.3 “Active Mode Power Consumption”: updated conditions (VDDCORE and ambient temperature) for “CoreMark Active Power Consumption” tables and for Figure 36-9 “SAM4N8/16 Active Power Consumption with VDDCORE @ 1.2V, TA = 25°C” Figure 36-10 “32.768 kHz Crystal Oscillator Schematics”: added caption “$C_{crystal}$” to diagram Updated Figure 36-12 “XIN Clock Timing” Table 36-27 ”PLL Characteristics”: changed parameter “Start-up Time” to “Settling Time” Figure 36-13 “Simplified Acquisition Path”: renamed caption “Csample” to “C_i”; renamed caption “12-bit ADC Core” to “12-bit ADC” Figure 36-19 “USART SPI Slave Mode (Mode 1 or 2)”: inserted correct diagram (was previously TWI diagram) Figure 36-20 “Two-wire Serial Bus Timing”: inserted correct diagram (was previously USART diagram) Section 36.10.3.1 “Maximum SPI Frequency”: updated contents under “Master Write Mode” and “Master Read Mode” Added Table 36-34 ”Programmable Voltage Reference Selection Values” Table 36-38 ”Voltage Reference Characteristics”: in bias current consumption, corrected conditions “Voltage reference OFF, ADC ON OR ADC ON” to “Voltage reference Off, ADC On or DAC On” Table 36-39 ”Temperature Sensor Characteristics”: deleted “After TSON = 1” from Startup Time conditions Table 36-42 ”SPI Timings”: removed footnotes defining 1.8V and 3.3V domains (this information is now found at the beginning of Section 36.10.3.2 “SPI Timings”) Table 36-43 ”USART SPI Timings”: removed footnotes defining 1.8V and 3.3V domains (this information is now found at the beginning of Section 36.10.4.1 “USART SPI TImings”) Table 36-44 ”Two-wire Serial Bus Requirements”: added parameter “Bus free time between a STOP and START condition”

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