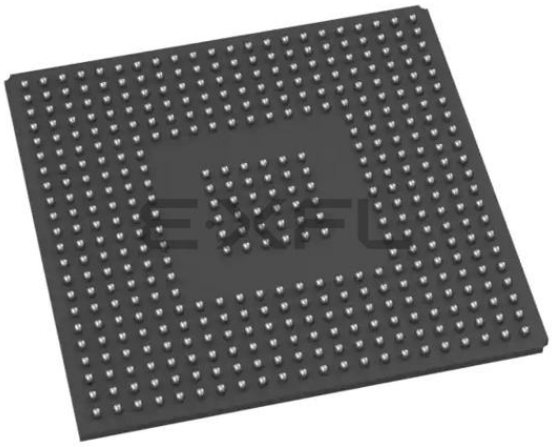

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	LCD, Touchscreen
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (3)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TC)
Security Features	-
Package / Case	420-FBGA
Supplier Device Package	420-PBGA
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spear600-2

List of tables

1.1 Main features

- Dual core ARM926EJ-S 32-bit RISC CPU, up to 333 MHz, each with:
  - 16 Kbytes of instruction cache, 16 Kbytes of data cache
  - 3 instruction sets: 32-bit for high performance, 16-bit (Thumb) for efficient code density, byte Java mode (Jazelle™) for direct execution of Java code.
  - Tightly Coupled Memory
  - AMBA bus interface
- 32-KByte on-chip BootROM
- 8-KByte on-chip SRAM
- Dynamic memory controller managing external DDR1 memory up to 166 MHz and external DDR2 memory up to 333 MHz
- Serial memory interface
- 8/16-bits NAND Flash controller
- Possible NAND Flash or serial NOR flash booting
- Multichannel DMA controller
- Color LCD Controller for STN/TFT display panels
  - Up to 1024 x 768 resolution
  - 24 bpp true color
- Ethernet GMAC 10/100/1000 Mbps (GMII/MII PHY interface)
- Two USB 2.0 host (high-full-low speed) with integrated PHY transceiver
- One USB 2.0 device (high-full speed) with integrated PHY transceiver
- 10 GPIO bidirectional signals with interrupt capability
- JPEG codec accelerator 1clock/pixel
- ADC 10-bit, 1 Msps 8 inputs/1-bit DAC
- 3 SSP master/slave (supporting Motorola, Texas instruments, National Semiconductor protocols) up to 40 Mbps
- I^2C master/slave interface (slow/ fast/high speed, up to 1.2 Mb/s)
- 10 independent 16-bit timers with programmable prescaler
- I/O peripherals
  - Two UARTs (speed rate up to 460.8 kbps)
  - Fast IrDA (FIR/MIR/SIR) 9.6 Kbps to 4 Mbps speed-rate
- Audio block with 3-I2Ss interfaces to support Audio Play (Up to 3.1) and Audio Record functionality.
- Advanced power saving features
  - Normal, Slow, Doze and Sleep modes, CPU clock with software-programmable frequency
  - Enhanced dynamic power-domain management
  - Clock gating functionality
  - Low frequency operating mode
  - Automatic power saving controlled from application activity demands
- Vectored interrupt controller
- System and peripheral controller

  - 4 dual port memory cuts (1024 words x 32 bits)
- Clock system constituted by:
  - 5 clocks coming from the external balls
  - 4 clocks coming from the integrated frequency synthesizers
  - CPU core clock frequency
  - Pll2 frequency
  - 48 MHz clock (USB Pll)
  - 30 MHz clock (Main Oscillator)
  - 32.768 kHz clock (RTC Oscillator)
  - APB clock (programmable)
  - AHB clock (programmable)
  - User Configurable sync/async clock towards Memory Controller port 2 (M2)
- Connection with 84/112 I/Os
- Connection with 9 LVDS lines
- 12 interrupt lines towards CPU1 and CPU2
- 64 interrupt input lines from the various platform IP sources
- 16 peripheral DMA request lines
- 64 user configurable (in the SoC) general purpose input lines
- 64 user configurable (in the RAS) general purpose output lines
- SoC dynamic power management control interface;
- 50 specific ATE Test interface signals dedicated to RAS

2.25 External Port Controller (EXPI I/F)

The port controller is a socket communication interface between the SPEAr600 and an external FPGA device; it implements a simple AHB bidirectional protocol used to compress a couple of std AHB master/slave bus onto 84 PL_GPIOs and 4 PL_CLK primary signals.

Caution: PL_GPIO pins are not configurable by software.

ST provide a symmetric port controller logic solution to be embedded inside the external FPGA with the purpose of interfacing the EXPI bus directly and decompressing the same pair of AHB master/slave ports on the FPGA side in order to interconnect the customer logic as follows (more slave and master agents can be connected to the EXPI):

SPEAr600_AHB-master >> FPGA_AHB-slave

SPEAr600_AHB-slave << FPGA_AHB-master (AHB-full)

The EXPI interface is based on two main groups of signals:

- AHB bidirectional signal bus driven alternatively from the SPEAr600 and FPGA side.
- Unidirectional signals continuously driven from both the SPEAr600 and FPGA sides.

Table 36: EXPI - pad signal assignment lists the EXPI signal names. Further details in these signals are given in the SPEAr600 user manual (UM0510)

3 Pin description

The following tables describe the pinout of the SPEAr600 listed by functional block.

This description refers to the default configuration of SPEAr600 (full features).

More details on the configuration of each pin are given in *Table 16: Multiplexing scheme*.

- *Table 2: System reset, master clock, RTC and configuration pins*
- *Table 3: Power supply pins*
- *Table 4: Debug pins*
- *Table 5: SMI, SSP, UART, FIRDA and I2C pins*
- *Table 6: USB pins*
- *Table 7: Ethernet pins*
- *Table 8: GPIO pins*
- *Table 9: ADC pins*
- *Table 10: NAND Flash I/F pins*
- *Table 11: DDR I/F pins*
- *Table 12: LCD I/F pins*
- *Table 13: LVDS I/F pins*
- *Table 14: EXPI/I2S pins*
- *Table 15: EXPI pins*

List of abbreviations:

PU = Pull Up

PD = Pull Down

3.1 Required external components

1. DDR_COMP_1V8: place an external 121 kΩ resistor between ball V7 and ball V8
2. DDR_COMP_2V5: place an external 121 kΩ resistor between ball V9 and ball V8
3. USB_RREF: connect an external 1.5 kΩ pull-down resistor to ball U4
4. DIGITAL_REXT: place an external 121 kΩ resistor between ball E11 and ball E126.

3.2 Pin descriptions listed by functional block

Table 2. System reset, master clock, RTC and configuration pins

Group	Signal name	Ball	Direction	Function	Pin type
SYSTEM RESET	MRESET	C17	Input	Main reset	TTL Schmitt trigger input buffer, 3.3 V tolerant, PU
CONFIG	DIGITAL_REXT	E11	Ref	Configuration	Analog, 3.3 V capable, See *Note 4*

Table 10. NAND Flash I/F pins

Group	Signal name	Ball	Direction	Function	Pin Type
NAND FLASH I/F	NF_IO_0	H19	I/O	Data	TTL bidirectional buffer, 3.3 V capable, 4 mA, 3.3 V tolerant, PU(1)
	NF_IO_1	H18			
	NF_IO_2	G19			
	NF_IO_3	G18			
	NF_IO_4	F19			
	NF_IO_5	F18			
	NF_IO_6	E18			
	NF_IO_7	E19			
	NF_CE	G20	Output	Chip enable	TTL output buffer, 3.3 V capable, 4 mA, active low
	NF_RE	G22		Read enable	
	NF_WE	H20		Write enable	
	NF_ALE	H21		Address latch enable	TTL output buffer, 3.3 V capable, 4 mA
	NF_CLE	G21		Command latch enable	
	NF_WP	J18		Write protect	
	NF_RB	H22	Input	Read/busy	TTL input buffer 3.3 V tolerant, PU

1. When the pin is not driven, the output voltage is 2.5 V, On the core side, logic ‘1’ state is guaranteed.

Table 11. DDR I/F pins (continued)

Group	Signal name	Ball	Direction	Function	Pin type
DDR I/F	DDR_DATA_5	Y12		Data lines (Lower byte)	SSTL_2 /SSTTL_18
	DDR_DATA_6	AB12			
	DDR_DATA_7	AA12			
	DDR_DQS_0	AB13	I/O	Differential lower Data Strobe	Differential SSTL_2/ SSTTL_18
	DDR_nDQS_0	AA13			
	DDR_DM_0	AA11	Output	Lower data mask	SSTL_2/ SSTTL_18
	DDR_GATE_0	Y13	I/O	Lower gate open	
	DDR_DATA_8	AB15	I/O	Data lines (Upper byte)	
	DDR_DATA_9	AA16			
	DDR_DATA_10	AB16			
	DDR_DATA_11	Y16			
	DDR_DATA_12	Y15			
	DDR_DATA_13	Y14			
	DDR_DATA_14	AB14			
	DDR_DATA_15	AA14			
	DDR_DQS_1	AB17	I/O	Differential upper	Differential
	DDR_nDQS_1	AA17		Data strobe	SSTL_2/ SSTTL_18
	DDR_DM_1	AA15	Output	Upper data mask	SSTL_2/ SSTTL_18
	DDR_GATE_1	Y17	I/O	Upper gate open	
	DDR_VREF	V10	Input	Ref. voltage	Analog
	DDR_COMP_2V5	V9	Ref	Ext. ref resistor	Analog, see *Note 2 on page 24*
	DDR_COMP_GND	V8	-	Common return for Ext. resistors	Power
	DDR_COMP_1V8	V7	Ref	Ext. ref. resistor	Analog, see *Note 1 on page 24*
	DDR2_EN	D11	Input	Configuration	TTL input buffer, 3.3 V tolerant, PU

Table 12. LCD I/F pins

Group	Signal name	Ball	Direction	Function	Pin Type
LCD I/F	CLD_0	Y20	Output	LCD Data	TTL output buffer, 3.3 V capable, 8 mA
	CLD_1	Y21			
	CLD_2	Y22			
	CLD_3	W22			
	CLD_4	W21			
	CLD_5	W20			
	CLD_6	V20			
	CLD_7	V21			
	CLD_8	V22			
	CLD_9	U22			
	CLD_10	U21			
	CLD_11	U20			
	CLD_12	T20			
	CLD_13	T21			
	CLD_14	R21			
	CLD_15	R20			
	CLD_16	P19			
	CLD_17	P20			
	CLD_18	P21			
	CLD_19	N21			
	CLD_20	N20			
	CLD_21	N19			
	CLD_22	M20			
	CLD_23	M21			
	CLAC	T22		STN AC bias drive TFT Data Enable	
	CLCP	R22		LCD Panel Clock	
	CLFP	P22		STN Frame Pulse\TFT Vertical Sync	
	CLLP	N22		STN Line Pulse\TFT Horizontal Sync	
	CLLE	M22		Line End	
	CLPOWER	M19		LCD Power Enable	

Table 15. EXPI pins (continued)

Group	Signal name	Ball	Direction	Function	Pin Type
EXPI	PL_GPIO_32	G3	I/O	Logic I/O	TTL bidirectional buffer 3.3 V capable, 4 mA, 3.3 V tolerant, PU(1)
	PL_GPIO_33	G4			
	PL_GPIO_34	G5			
	PL_GPIO_35	F5			
	PL_GPIO_36	F4			
	PL_GPIO_37	F3			
	PL_GPIO_38	F2			
	PL_GPIO_39	F1			
	PL_GPIO_40	E4			
	PL_GPIO_41	E3			
	PL_GPIO_42	E2			
	PL_GPIO_43	E1			
	PL_GPIO_44	D3			
	PL_GPIO_45	D2			
	PL_GPIO_46	D1			
	PL_GPIO_49	B1			
	PL_GPIO_56	B4			
	PL_GPIO_57	C4			
	PL_GPIO_58	D4			
	PL_GPIO_59	E5			
	PL_GPIO_60	D5			
	PL_GPIO_61	C5			
	PL_GPIO_62	B5			
	PL_GPIO_63	B6			

Table 15. EXPI pins (continued)

Group	Signal name	Ball	Direction	Function	Pin Type
EXPI	PL_GPIO_64	C6	I/O	Logic I/O	TTL bidirectional buffer 3.3 V capable, 3.3 V tolerant, 4 mA, PU(1)
	PL_GPIO_65	D6			
	PL_GPIO_66	E6			
	PL_GPIO_67	F6			
	PL_GPIO_68	F7			
	PL_GPIO_69	E7			
	PL_GPIO_70	D7			
	PL_GPIO_71	C7			
	PL_GPIO_72	B7			
	PL_GPIO_73	E8			
	PL_GPIO_74	D8			
	PL_GPIO_75	C8			
	PL_GPIO_76	B8			
	PL_GPIO_77	A8			
	PL_GPIO_78	C9			
	PL_GPIO_79	D9			
	PL_GPIO_80	E9			
	PL_GPIO_81	E10			
	PL_GPIO_82	D10			
	PL_GPIO_83	C10			
	PL_CLK_1	A7		Logic External Clock	TTL bidirectional buffer, 3.3 V capable, 8 mA, 3.3 V tolerant, PU(1)
	PL_CLK_2	A6			
	PL_CLK_3	A5			

1. When the pin is not driven, the output voltage is 2.5 V, On the core side, logic ‘1’ state is guaranteed

Table 16. Multiplexing scheme (continued)

Ball	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Full RAS	Mode 7
T22	CLAC		NFIO_13_o		CLAC	CLAC		CLAC
R22	CLCP		NFIO_12_o		CLCP	CLCP		CLCP
P22	CLFP		NFIO_11_o		CLFP	CLFP		CLFP
M22	CLLE		NFIO_10_o		CLLE	CLLE		CLLE
N22	CLLP		NFIO_9_o		CLLP	CLLP		CLLP
M19	CLPOWER		NFIO_8_o		CLPOWER	CLPOWER		CLPOWER
L21	SMI_DATAIN				SMI_DATAIN	SMI_DATAIN		SMI_DATAIN
L20	SMI_DATAOUT				SMI_DATAOUT	SMI_DATAOUT		SMI_DATAOUT
L22	SMI_CLK				SMI_CLK	SMI_CLK		SMI_CLK
L19	SMI_CS_0				SMI_CS_0	SMI_CS_0		SMI_CS_0
L18	SMI_CS_1				SMI_CS_1	SMI_CS_1		SMI_CS_1
K22	SSP_2_SCLK				SSP_2_SCLK	SSP_2_SCLK		SSP_2_SCLK
K21	SSP_2_MISO				SSP_2_MISO	SSP_2_MISO		SSP_2_MISO
K20	SSP_2_MOSI				SSP_2_MOSI	SSP_2_MOSI		SSP_2_MOSI
K18	BOOT_SEL							
K19	SSP_2_SS_0				SSP_2_SS_0	SSP_2_SS_0		SSP_2_SS_0
J22	SSP_3_SCLK				SSP_3_SCLK	SSP_3_SCLK		SSP_3_SCLK
J21	SSP_3_MISO				SSP_3_MISO	SSP_3_MISO		SSP_3_MISO
J20	SSP_3_MOSI				SSP_3_MOSI	SSP_3_MOSI		SSP_3_MOSI
J19	SSP_3_SS				SSP_3_SS	SSP_3_SS		SSP_3_SS
H19	NF_IO_0	GPIO_basic[7]			NF_IO_0	NF_IO_0		NF_IO_0
H18	NF_IO_1	GPIO_basic[6]			NF_IO_1	NF_IO_1		NF_IO_1
G19	NF_IO_2	GPIO_basic[5]			NF_IO_2	NF_IO_2		NF_IO_2
G18	NF_IO_3	GPIO_basic[4]			NF_IO_3	NF_IO_3		NF_IO_3
F19	NF_IO_4	GPIO_basic[3]			NF_IO_4	NF_IO_4		NF_IO_4
F18	NF_IO_5	GPIO_basic[2]			NF_IO_5	NF_IO_5		NF_IO_5
E18	NF_IO_6	GPIO_ARM1[7]			NF_IO_6	NF_IO_6		NF_IO_6
E19	NF_IO_7	GPIO_ARM2[7]			NF_IO_7	NF_IO_7		NF_IO_7

Table 16. Multiplexing scheme (continued)

Ball	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Full RAS	Mode 7
G20	NF_CE	nUART1RTS			NF_CE	NF_CE		NF_CE
H20	NF_WE	nUART1CTS			NF_WE	NF_WE		NF_WE
G22	NF_RE	nUART1DCD			NF_RE	NF_RE		NF_RE
H21	NF_ALE	nUART1DTR			NF_ALE	NF_ALE		NF_ALE
G21	NF_CLE	nUART1DSR			NF_CLE	NF_CLE		NF_CLE
H22	NF_RB	nUART1RI			NF_RB	NF_RB		NF_RB
J18	NF_WP	SMICS_OUT_3			NF_WP	NF_WP		NF_WP
C17	MRESET				MRESET	MRESET		MRESET
D11	DDR2_EN				DDR2_EN	DDR2_EN		DDR2_EN
D17	nTRST				nTRST	nTRST		nTRST
E16	TCK				TCK	TCK		TCK
D15	TMS				TMS	TMS		TMS
D16	TDI				TDI	TDI		TDI
E17	TDO				TDO	TDO		TDO
E15/TEST_0	0	0	0	0	0	0	0	0
E14/TEST_1	0	0	0	0	0	0	0	0
D14/TEST_2	0	0	0	0	0	0	0	1
D13/TEST_3	0	1	0	1	0	1	0	0
E13/TEST_4	0	0	1	1	0	0	1	1
D12/TEST_5	0	0	0	0	1	1	1	1
E22	GMII_TXCLK125				GMII_TXCLK125	GMII_TXCLK125		GMII_TXCLK125
F22	GMII_TXCLK			GPIO_basic[7]	GMII_TXCLK	GMII_TXCLK		GMII_TXCLK
D22	MII_TXCLK			GPIO_basic[6]	MII_TXCLK	MII_TXCLK		MII_TXCLK
F21	TXD_0			GPIO_basic[5]	TXD_0	TXD_0		TXD_0
E21	TXD_1			GPIO_basic[4]	TXD_1	TXD_1		TXD_1
F20	TXD_2			GPIO_basic[3]	TXD_2	TXD_2		TXD_2
E20	TXD_3			GPIO_basic[2]	TXD_3	TXD_3		TXD_3
D21	GMII_TXD_4			GPIO_ARM1[7]	GMII_TXD_4	GMII_TXD_4		GMII_TXD_4

Table 16. Multiplexing scheme (continued)

Ball	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Full RAS	Mode 7
B15	PH2n				PH2n	PH2n		PH2n
A14	PH3				PH3	PH3		PH3
B14	PH3n				PH3n	PH3n		PH3n
C14	PH4				PH4	PH4		PH4
C13	PH4n				PH4n	PH4n		PH4n
A13	PH5				PH5	PH5		PH5
B13	PH5n				PH5n	PH5n		PH5n
A12	PH6				PH6	PH6		PH6
B12	PH6n				PH6n	PH6n		PH6n
C12	PH7				PH7	PH7		PH7
C11	PH7n				PH7n	PH7n		PH7n
A11	PH8				PH8	PH8		PH8
B11	PH8n				PH8n	PH8n		PH8n
B9	RTC_XO				RTC_XO	RTC_XO		RTC_XO
A9	RTC_XI				RTC_XI	RTC_XI		RTC_XI
A7								
A6								
A5								
A4								
C10								
D10								
E10								
E9								
D9								
C9								
A8								
B8								
C8								

Table 16. Multiplexing scheme (continued)

Ball	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Full RAS	Mode 7
D8								
E8								
B7								
C7								
D7								
E7								
F7								
F6								
E6								
D6								
C6								
B6								
B5								
C5								
D5								
E5								
D4								
C4								
B4								
A3								
B3								
C3								
A2								
B2								
A1								
B1								
C1								
C2								

3. The maximum current and power values listed above, obtained with typical supply voltages, are not guaranteed to be the highest obtainable. These values are dependent on many factors including the type of applications running, clock rates, use of internal functional capabilities, external interface usage, case temperature, and the power supply voltages. Your specific application can produce significantly different results.

   1 V current and power are primarily dependent on the applications that are running and the use of internal chip functions (DMA, USB, Ethernet, and so on).

   3.3 V current and power are primarily dependent on the capacitive loading, frequency, and utilization of the external buses.

5.3 DC electrical characteristics

The recommended operating conditions are listed in the following table:

Table 21. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD} 1.0	Supply voltage at 1.0	0.95	1	1.10	V
V_{DD} 3.3	Supply voltage at 3.3	3	3.3	3.6	V
V_{DD} 2.5	Supply voltage at 2.5	2.25	2.5	2.75	V
V_{DD} 1.8	Supply voltage at 1.8	1.70	1.8	1.9	V
V_{DD}RTC	Supply voltage at 1.8	1.62	1.8	1.98	V
T_A	Ambient temperature	-40		85	°C
T_J	Junction temperature	-40		125	°C

5.4 Overshoot and undershoot

This product can support the following values of overshoot and undershoot.

Table 22. Overshoot and undershoot specifications

Parameter	3V3 I/Os	2V5 I/Os	1V8 I/Os
Amplitude	500 mV	500 mV	500 mV
Ratio of overshoot (or undershoot) duration with respect to pulse width	1/3	1/3	1/3

If the amplitude of the overshoot/undershoot increases (decreases), the ratio of overshoot/undershoot width to the pulse width decreases (increases). The formula relating the two is:

Amplitude of OS/US = 0.75*(1- ratio of OS (or US) duration with respect to pulse width)

Note: The value of overshoot/undershoot should not exceed the value of 0.5 V. However, the duration of the overshoot/undershoot can be increased by decreasing its amplitude.

Note: 1 The oscillator generates a stable clock 1.5 ms after the power supply becomes stable.

2 The Pll lock time is given by the following formula:

Lock time = 4 ms / (decimal equivalent of PLL charge pump bit setting + 1)

The PLL charge pump (CP) bits are in the PLL1/2_CTR register in the Miscellaneous register block. Please refer to the user manual for more details.

For example, if the application software sets CP = 01110 = 14 (decimal), then:

Lock time = 4 ms / 15 = 267 µs.

5.9 ADC electrical parameters

Table 30. ADC characteristics

Parameters		Min	Typ	Max	Unit
Analog Input	Input range (absolute)	0-0.3		AV_{DD}+0.3	V
	Conversion Range	VREFN		VREFP	V
	Input Capacitance	5	6.4	8	pF
	Input Mux Resistance (Total equivalent Sampling Resistance	1.5K	2K	2.5K	Ω
Power Supply	Analog Supply AV_{DD}	2.25	2.5	2.8	V
	Digital Supply V_{DD}	0.9	1.0	1.1	V
External Reference voltages	VREFP	1.0	2.5	2.8	V
	VREFN	0	0	0.7	V
Clock Frequency		3	14		MHz
Performance parameters	INL			± 1	LSB
	DNL			± 1	LSB
	Gain error			± 2	LSB
	Offset error			± 2	LSB
Temperature range		-40	25	125	°C
Current Consumption	AV_{DD} (External reference mode)	0.6	0.8	1	mA
	AV_{DD} (Power down mode EN=0)			0.4	µA
	V_{DD} (Functional mode)	0.1	0.15	0.2	mA
	V_{DD} (Power down mode)			1	µA

6.6.3 GMII-MII Receive timing specifications

Figure 37. GMII-MII RX waveforms

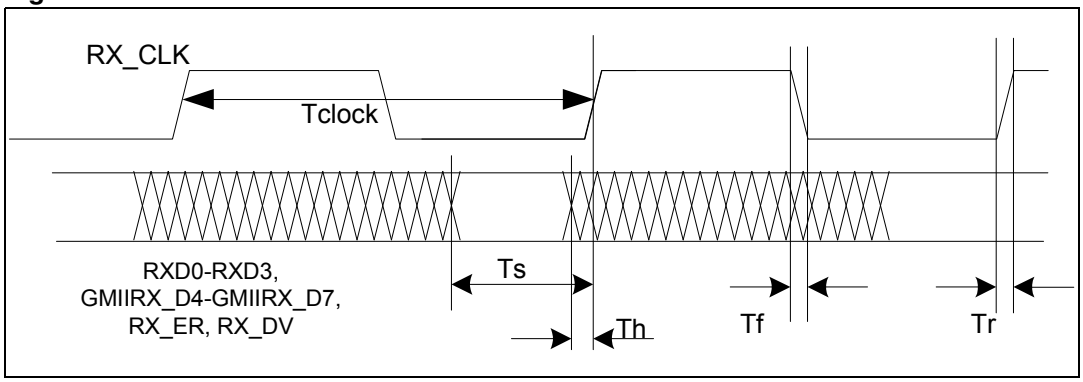


Figure 38. Block diagram of GMII-MII RX pins

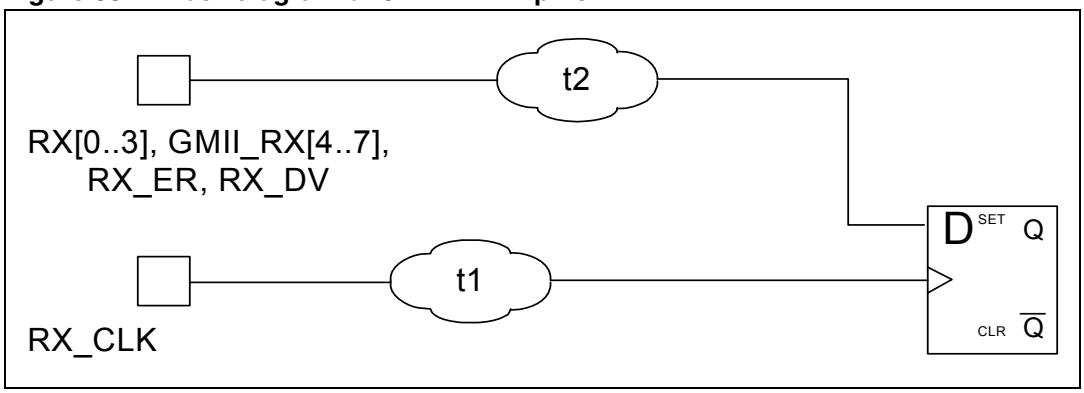


Table 52. GMII-MII RX timings

Parameter	Value using GMII [t_{CLK} period = 8 ns 125 MHz]	Value using MII 100Mb [t_{CLK} period = 40 ns 25 MHz]	Value using MII 10 Mb [t_{CLK} period = 400 ns 2.5 MHz]
$t_{SETUPmax}$ (t_S)= $t2_{max}$ - $t1_{min}$	2.26 ns	2.26 ns	2.26 ns
$t_{HOLDmin}$ (t_H)= $t2_{min}$ - $t1_{max}$	-0.11 ns	-0.11 ns	-0.11 ns

Note: The input stage is the same for all the interfaces (GMII and MII10/100) so t_{SETUP} and t_{HOLD} values are equal in all the cases.

The receive path is optimized for the GMII interface: this also ensures correct capture of data for the MII10/100 interface.

6.8 SSP timing characteristics

The device SPEAr600 contains 3 SSP modules. The Low Speed Connectivity Subsystem contains SSP1 and SSP2, the Application Subsystem contains SSP3. These 3 identical modules provide a programmable length shift register which allows serial communication with other SSP devices through a 3 or 4 wire interface (SSP_SCLK, SSP_MISO, SSP_MOSI and SSP_SS). The SSP module supports the following features:

- Master/Slave mode operations
- Programmable clock bit rate and prescaler
- Programmable choice of interface operation: SPI, Microwire or TI synchronous serial

Programmable data frame size from 5 to 16 bits

- Separate transmit and receive FIFO, 16 bits wide, 8 locations deep

The features of the Motorola SPI-compatible interface are:

- Full duplex, four-wire synchronous transfers (SSP_SCLK, SSP_MISO, SSP_MOSI and SSP_SS)
- Programmable Clock Polarity (CPOL) and Clock Phase (CPHA)

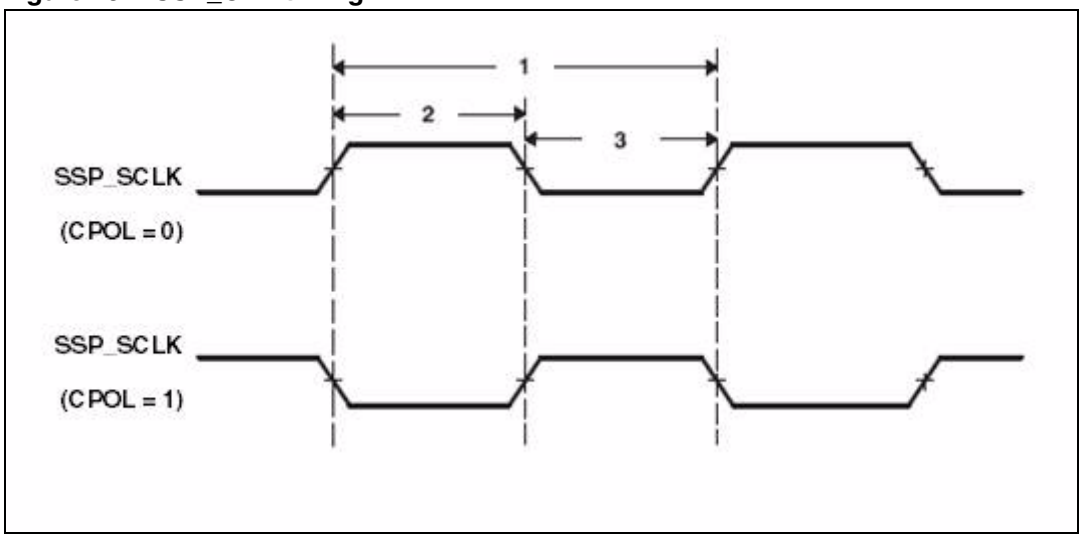
The following Tables show the Timing Requirements of the SPI four-wire synchronous transfer for the 3 SSP modules present in the Spear600 configured in master mode (indicated in the tables as SPI1, SPI2 and SPI3). Both the Timings on MISO (master input slave output) pad and MOSI (master output slave input) pad are provided.

Table 56. Timing requirements for SSP (all modes)

No.	parameters		value	unit
1	Tc(CLK)	Cycle time, SSP_SCLK	24 (min)	ns
2	Tw(CLKH)	Pulse duration, SSP_SCLK high	.49T - .51T	ns
3	Tw(CLKL)	Pulse duration, SSP_SCLK low	.51T - .49T	ns

T = Tc(CLK) = SSP_CLK period is equal to the SSP module master clock divided by a configurable divider.

Figure 43. SSP_CLK timing



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

SPEAr600 is ROHS-6 compliant.

Table 63. Document revision history (continued)

Date	Revision	Changes
8-Feb-2010	2	Added I2S to *Table 18: Memory map*. Modified pin list of I2S and EXPI *Table 14: EXPI/I2S pins* and *Table 15: EXPI pins*. Updated sections *Features*, *Main features* and *I2S audio block* improving the description of I2S feature. Updated *Table 19: Absolute maximum ratings* Updated section *DDR2 timing characteristics*. Updated *Table 27: Driver characteristics*. Updated *Section 5.1: Absolute maximum ratings* Updated *Table 21: Recommended operating conditions*. Updated *Section 2.15: UARTs* Updated introduction of *Chapter 7: Package information* Updated *Table 10: NAND Flash I/F pins*. Updated *Table 3: Power supply pins*. Updated *Table 6: USB pins*. Updated *Figure 1: Functional block diagram* and *Figure 2: Typical system architecture using SPEAr600* Changed “SPI” with “SSP” where necessary. Inserted the new *Section 6.8: SSP timing characteristics* Corrected the frequency of DDR1. Separated the *Electrical characteristics* and *Timing characteristics* in two chapters Changed the title of the *Section 5.5: 3.3V I/O characteristics* Added *Table 62: SPEAr600 PBGA420 thermal resistance characteristics*. Updated *Figure 25*, *Figure 26*, *Figure 27*, *Figure 30*, *Figure 31*, *Figure 32*. Added a line of explanation in the introduction of *Section 3: Pin description*. Added new *Section 3.3: Configuration modes*. Added new *Section 2.25: External Port Controller (EXPI I/F)*.

Table 63. Document revision history (continued)

Date	Revision	Changes
09-May-2012	3	Modified FSMC feature *on page 1* *Figure 2: Typical system architecture using SPEAr600*: – Deleted SRAM and ROM blocks which were connected to the FSMC block – Substituted SSP with 3xSSP – Added the RAS block. *Section 1.1: Main features on page 9*: – Deleted the word “/parallel” from bullet seven (about FSMC) – Replaced SPI with SSP in bullet sixteen. – Modified number of GPIOs to 10 – Added information about RAS (Reconfigurable Array Subsystem) *Chapter 2: Architecture overview*: reviewed the first introduction part. *Section 2.4: Flexible static memory controller*: – Updated the introduction. – Main features: changed the sentence “Provides independent chip select for each memory bank" by "Provides only one chip select for the first memory bank" *Table 3: Power supply pins*: swapped ball R1 from the “Digital ground group” to the “Analog ground group”. *Section 2.15: UARTs*: corrected the value of the baud rate to 3 Mbps *Table 48: Timing characteristics for 8-bit NAND Flash configuration* and *Table 49: Timing characteristics for 16-bit NAND Flash configuration*: added three footnotes. *Table 3: Power supply pins*: swapped ball R1 from the “Digital ground group” to the “Analog ground group”. *Section 2.15: UARTs*: corrected the value of the baud rate in 3 Mbps *Table 48: Timing characteristics for 8-bit NAND Flash configuration* and *Table 49: Timing characteristics for 16-bit NAND Flash configuration*: added three footnotes. Created the new *Section 2.24: Reconfigurable array subsystem connectivity (RAS)*. *Section 3.3: Configuration modes* and *Section Table 16.: Multiplexing scheme*: removed additional PL_GPIOs, PL_CLK signals and renamed GPIOs to EXPI IOs *Section 6.6.3: GMII-MII Receive timing specifications*: added *Table 52: GMII-MII RX timings*. Changed parameter T_O to T_A and added T_J in *Table 21: Recommended operating conditions* Updated *Table 62: SPEAr600 PBGA420 thermal resistance characteristics*.