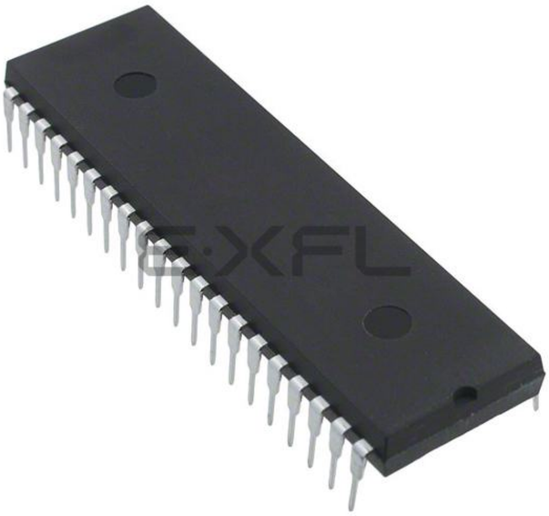
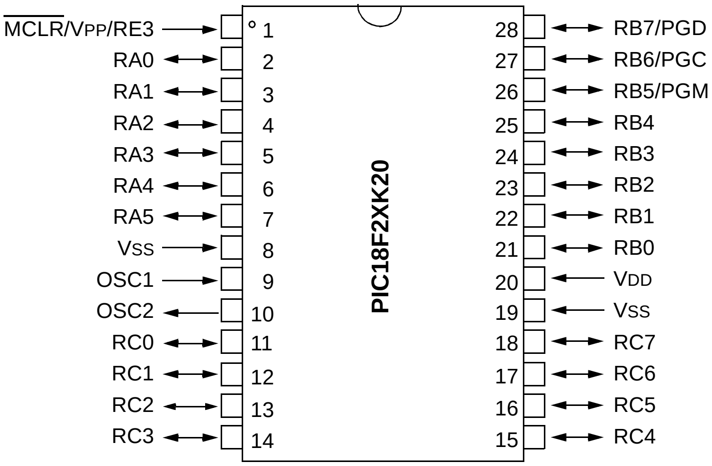
Microchip Technology - PIC18F43K20-E/P Datasheet



Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f43k20-e-p

FIGURE 2-1: 28-PIN SDIP, SSOP AND SOIC PIN DIAGRAMS

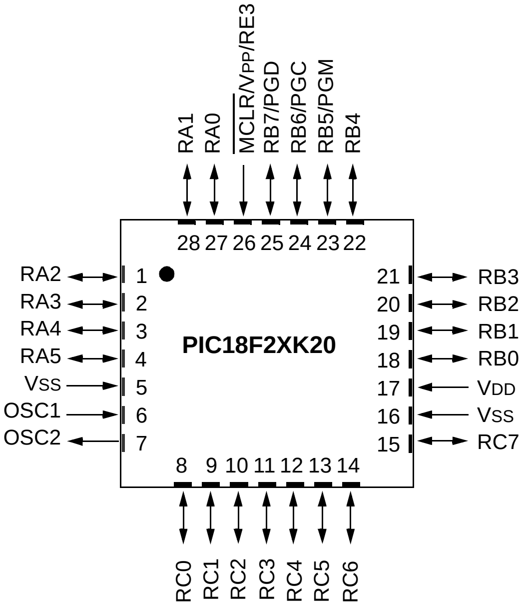
SDIP, SSOP, SOIC (300 MIL)



Note: The following devices are included in 28-pin SDIP, SSOP and SOIC parts: PIC18F23K20, PIC18F24K20, PIC18F25K20, PIC18F26K20.

FIGURE 2-2: 28-PIN QFN PIN DIAGRAMS

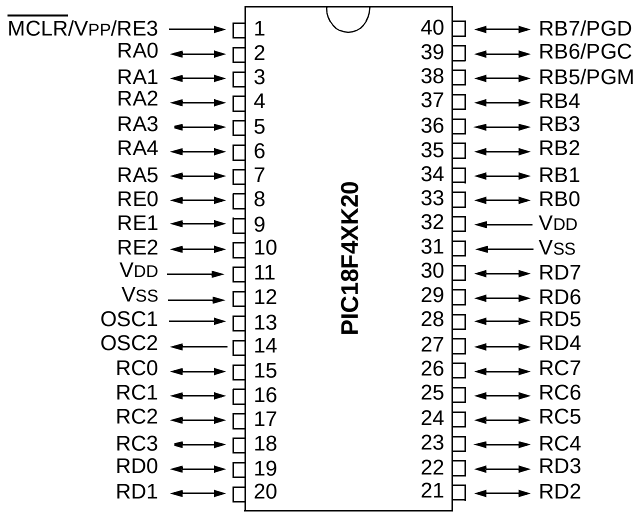
28-Pin QFN



Note: The following devices are included in 28-pin QFN parts: PIC18F23K20, PIC18F24K20, PIC18F25K20, PIC18F26K20.

FIGURE 2-3: 40-PIN PDIP PIN DIAGRAMS

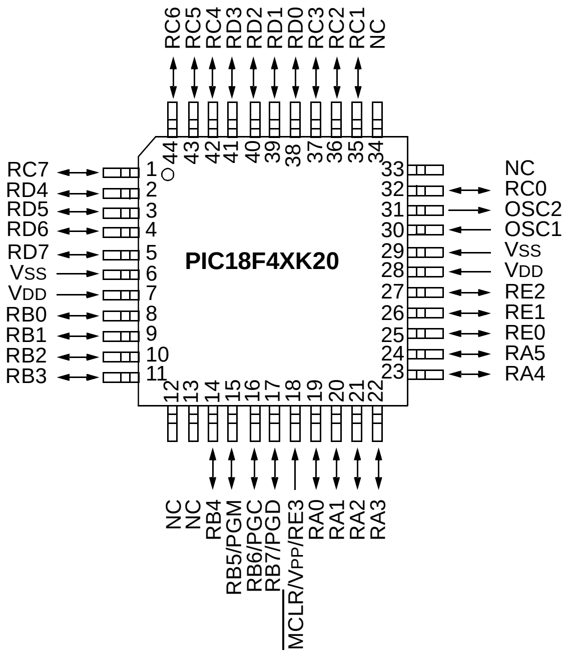
40-PIN PDIP (600 MIL)



Note: The following devices are included in 40-pin PDIP parts: PIC18F43K20, PIC18F44K20, PIC18F45K20, PIC18F46K20.

FIGURE 2-4: 44-PIN TQFP PIN DIAGRAMS

44-PIN TQFP



Note: The following devices are included in 44-pin TQFP parts: PIC18F43K20, PIC18F44K20, PIC18F45K20, PIC18F46K20.

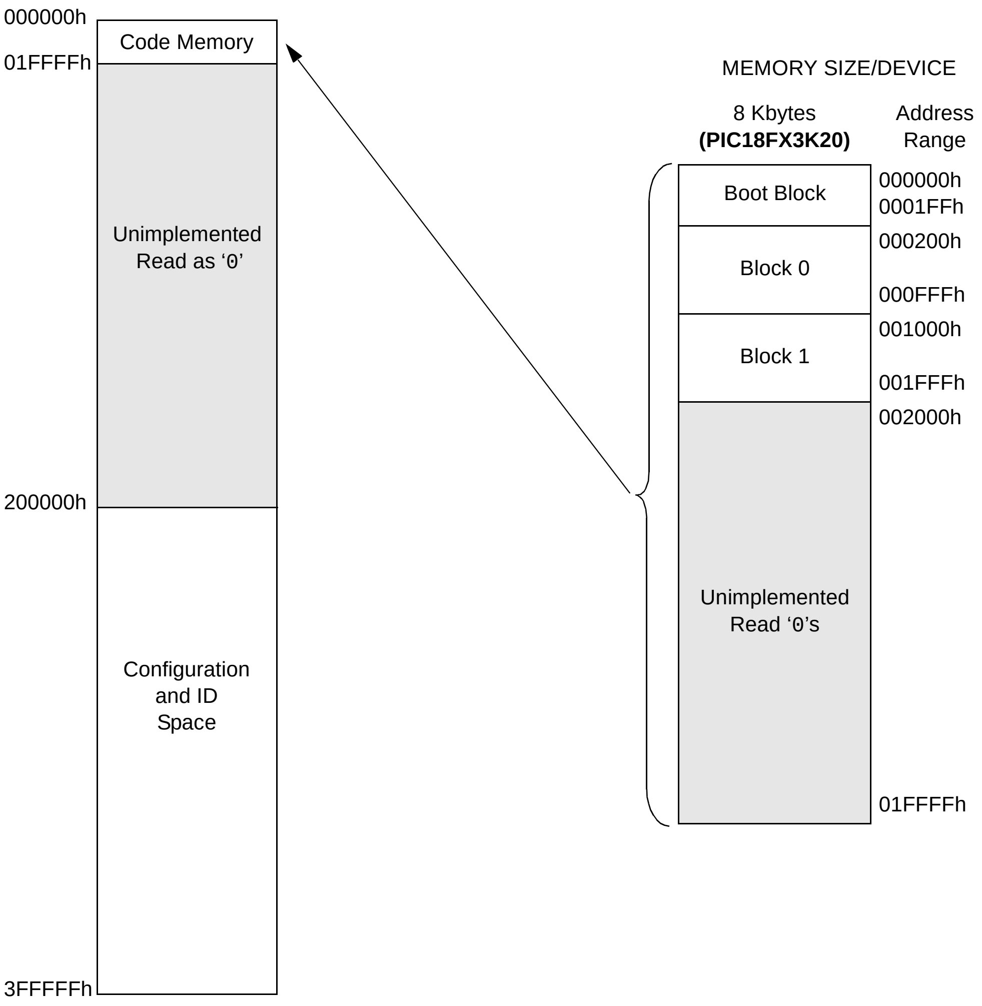
2.3 Memory Maps

For the PIC18FX3K20 devices, the code memory space extends from 0000h to 01FFFh (8 Kbytes) in two 4-Kbyte blocks. Addresses 0000h through 01FFh, however, define a “Boot Block” region that is treated separately from Block 0. All of these blocks define code protection boundaries within the code memory space.

TABLE 2-2: IMPLEMENTATION OF CODE MEMORY

Device	Code Memory Size (Bytes)
PIC18F23K20	000000h-001FFFh (8K)
PIC18F43K20	

FIGURE 2-6: MEMORY MAP AND THE CODE MEMORY SPACE FOR PIC18FX3K20 DEVICES



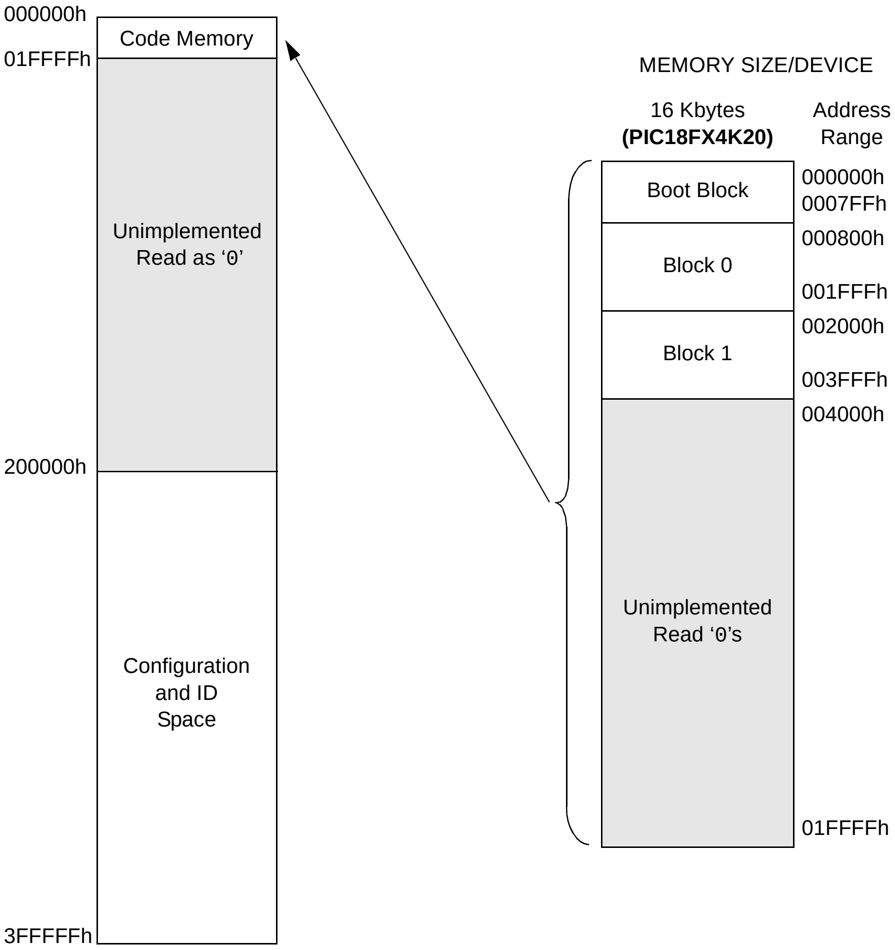
Note: Sizes of memory areas are not to scale.

For PIC18FX4K20 devices, the code memory space extends from 000000h to 003FFFh (16 Kbytes) in two 8-Kbyte blocks. Addresses 000000h through 0007FFh, however, define a “Boot Block” region that is treated separately from Block 0. All of these blocks define code protection boundaries within the code memory space.

TABLE 2-3: IMPLEMENTATION OF CODE MEMORY

Device	Code Memory Size (Bytes)
PIC18F24K20	000000h-003FFFh (16K)
PIC18F44K20	

FIGURE 2-7: MEMORY MAP AND THE CODE MEMORY SPACE FOR PIC18FX4K20 DEVICES



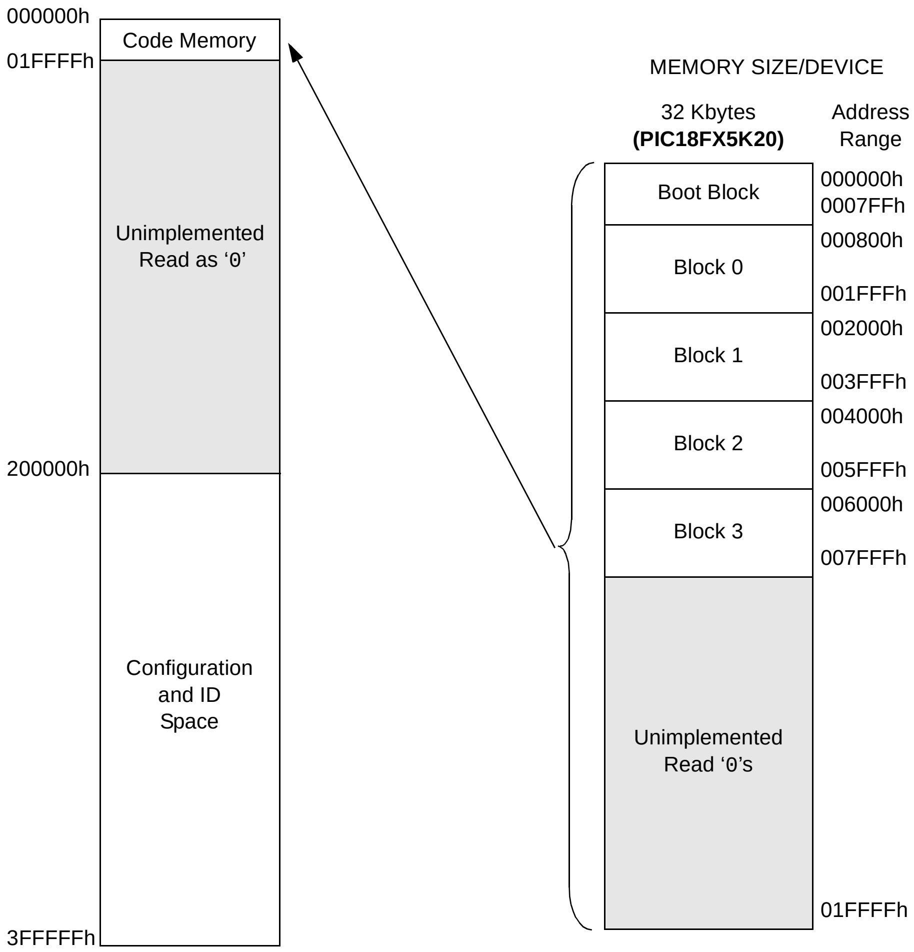
Note: Sizes of memory areas not to scale.

For PIC18FX5K20 devices, the code memory space extends from 000000h to 007FFFh (32 Kbytes) in four 8-Kbyte blocks. Addresses 000000h through 0007FFh, however, define a “Boot Block” region that is treated separately from Block 0. All of these blocks define code protection boundaries within the code memory space.

TABLE 2-4: IMPLEMENTATION OF CODE MEMORY

Device	Code Memory Size (Bytes)
PIC18F25K20	000000h-007FFFh (32K)
PIC18F45K20	

FIGURE 2-8: MEMORY MAP AND THE CODE MEMORY SPACE FOR PIC18FX5K20 DEVICES

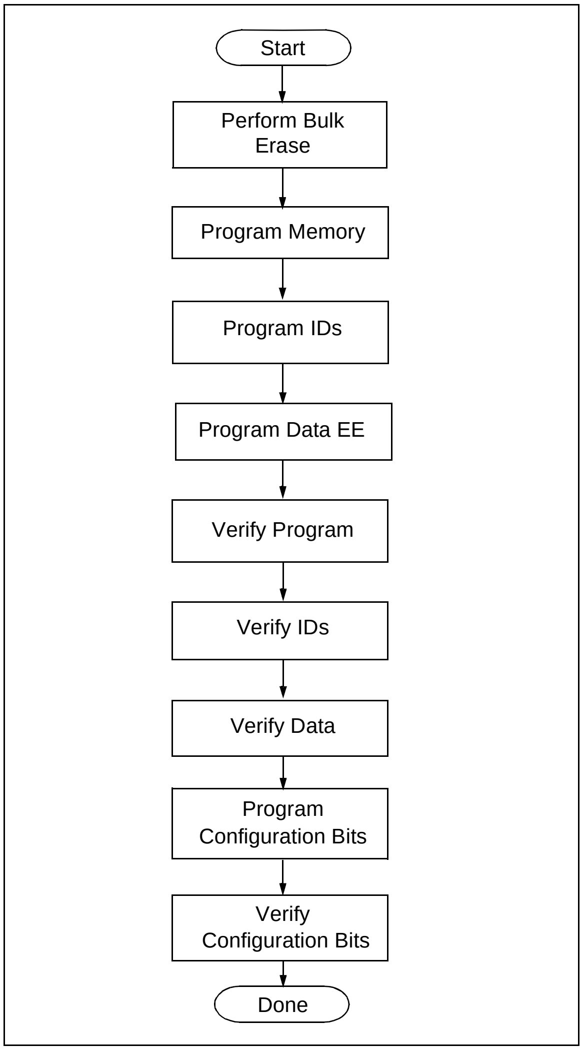


Note: Sizes of memory areas not to scale.

2.4 High-Level Overview of the Programming Process

Figure 2-11 shows the high-level overview of the programming process. First, a Bulk Erase is performed. Next, the code memory, ID locations and data EEPROM are programmed. These memories are then verified to ensure that programming was successful. If no errors are detected, the Configuration bits are then programmed and verified.

FIGURE 2-11: HIGH-LEVEL PROGRAMMING FLOW



2.5 Entering and Exiting High-Voltage ICSP Program/Verify Mode

As shown in Figure 2-12, the High-Voltage ICSP Program/Verify mode is entered by holding PGC and PGD low and then raising $\overline{\text{MCLR}}$/VPP/RE3 to VIHH (high voltage). Once in this mode, the code memory, data EEPROM, ID locations and Configuration bits can be accessed and programmed in serial fashion. Figure 2-13 shows the exit sequence.

The sequence that enters the device into the Program/Verify mode places all unused I/Os in the high-impedance state.

FIGURE 2-12: ENTERING HIGH-VOLTAGE PROGRAM/VERIFY MODE

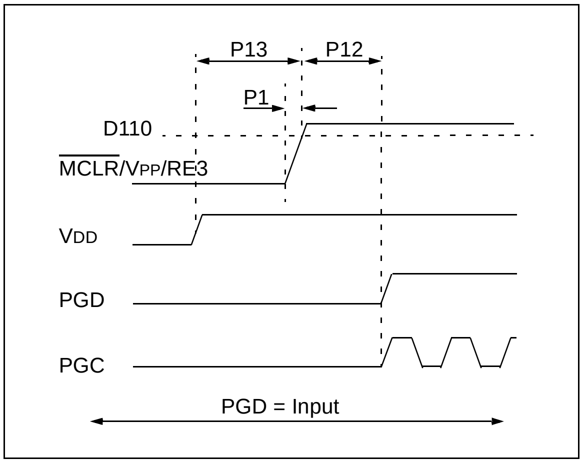
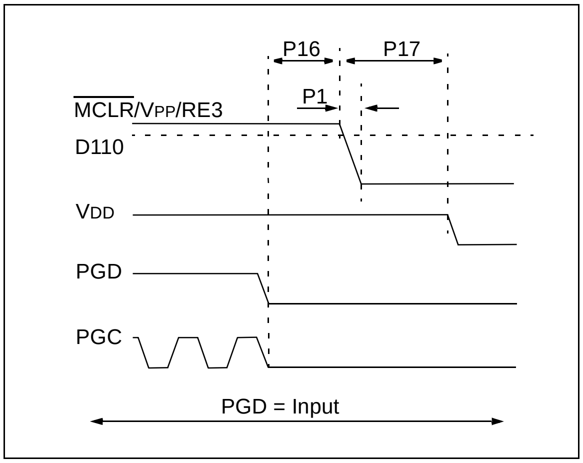


FIGURE 2-13: EXITING HIGH-VOLTAGE PROGRAM/VERIFY MODE



3.0 DEVICE PROGRAMMING

Programming includes the ability to erase or write the various memory regions within the device.

In all cases, except high-voltage ICSP Bulk Erase, the EECON1 register must be configured in order to operate on a particular memory region.

When using the EECON1 register to act on code memory, the EEPGD bit must be set (EECON1<7> = `1`) and the CFGS bit must be cleared (EECON1<6> = `0`). The WREN bit must be set (EECON1<2> = `1`) to enable writes of any sort (e.g., erases) and this must be done prior to initiating a write sequence. The FREE bit must be set (EECON1<4> = `1`) in order to erase the program space being pointed to by the Table Pointer. The erase or write sequence is initiated by setting the WR bit (EECON1<1> = `1`). It is strongly recommended that the WREN bit only be set immediately prior to a program or erase.

3.1 ICSP Erase

3.1.1 HIGH-VOLTAGE ICSP BULK ERASE

Erasing code or data EEPROM is accomplished by configuring two Bulk Erase Control registers located at 3C0004h and 3C0005h. Code memory may be erased portions at a time, or the user may erase the entire device in one action. Bulk Erase operations will also clear any code-protect settings associated with the memory block erased. Erase options are detailed in Table 3-1. If data EEPROM is code-protected (CPD = `0`), the user must request an erase of data EEPROM (e.g., 0084h as shown in Table 3-1).

TABLE 3-1: BULK ERASE OPTIONS

Description	Data (3C0005h:3C0004h)
Chip Erase	0F8Fh
Erase User ID	0088h
Erase Data EEPROM	0084h
Erase Boot Block	0081h
Erase Config Bits	0082h
Erase Code EEPROM Block 0	0180h
Erase Code EEPROM Block 1	0280h
Erase Code EEPROM Block 2	0480h
Erase Code EEPROM Block 3	0880h

The actual Bulk Erase function is a self-timed operation. Once the erase has started (falling edge of the 4th PGC after the `NOP` command), serial execution will cease until the erase completes (parameter P11). During this time, PGC may continue to toggle but PGD must be held low.

The code sequence to erase the entire device is shown in Table 3-2 and the flowchart is shown in Figure 3-1.

Note:	A Bulk Erase is the only way to reprogram code-protect bits from an “on” state to an “off” state.

TABLE 3-2: BULK ERASE COMMAND SEQUENCE

4-Bit Command	Data Payload	Core Instruction
`0000`	0E 3C	`MOVLW 3Ch`
`0000`	6E F8	`MOVWF TBLPTRU`
`0000`	0E 00	`MOVLW 00h`
`0000`	6E F7	`MOVWF TBLPTRH`
`0000`	0E 05	`MOVLW 05h`
`0000`	6E F6	`MOVWF TBLPTRL`
`1100`	0F 0F	`Write 0Fh to 3C0005h`
`0000`	0E 3C	`MOVLW 3Ch`
`0000`	6E F8	`MOVWF TBLPTRU`
`0000`	0E 00	`MOVLW 00h`
`0000`	6E F7	`MOVWF TBLPTRH`
`0000`	0E 04	`MOVLW 04h`
`0000`	6E F6	`MOVWF TBLPTRL`
`1100`	8F 8F	`Write 8F8Fh TO 3C0004h to erase entire device.`
`0000`	00 00	`NOP`
`0000`	00 00	`Hold PGD low until erase completes.`

FIGURE 3-1: BULK ERASE FLOW

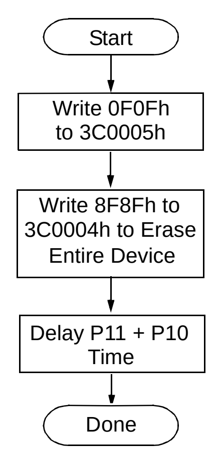
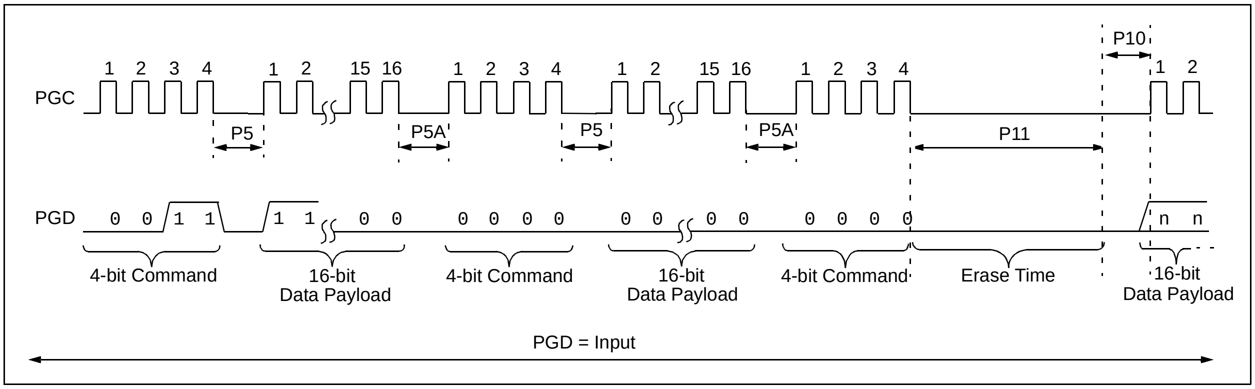


FIGURE 3-2: BULK ERASE TIMING DIAGRAM



3.1.2 LOW-VOLTAGE ICSP BULK ERASE

When using low-voltage ICSP, the part must be supplied by the voltage specified in parameter D111 if a Bulk Erase is to be executed. All other Bulk Erase details as described above apply.

If it is determined that a program memory erase must be performed at a supply voltage below the Bulk Erase limit, refer to the erase methodology described in **Section 3.1.3 "ICSP Row Erase"** and **Section 3.2.1 "Modifying Code Memory"**.

If it is determined that a data EEPROM erase must be performed at a supply voltage below the Bulk Erase limit, follow the methodology described in **Section 3.3 "Data EEPROM Programming"** and write '1's to the array.

3.1.3 ICSP ROW ERASE

Regardless of whether high or low-voltage ICSP is used, it is possible to erase one row (64 bytes of data), provided the block is not code or write-protected. Rows are located at static boundaries beginning at program memory address 000000h, extending to the internal program memory limit (see **Section 2.3 "Memory Maps"**).

The Row Erase duration is self-timed. After the WR bit in EECON1 is set, two `NOP`s are issued. Erase starts upon the 4th PGC of the second `NOP`. It ends when the WR bit is cleared by hardware.

The code sequence to Row Erase a PIC18F2XK20/4XK20 device is shown in Table 3-3. The flowchart shown in Figure 3-3 depicts the logic necessary to completely erase a PIC18F2XK20/4XK20 device. The timing diagram for Row Erase is identical to the data EEPROM write timing shown in Figure 3-7.

Note:	The TBLPTR register can point at any byte within the row intended for erase.

TABLE 3-3: ERASE CODE MEMORY CODE SEQUENCE

4-bit Command	Data Payload	Core Instruction
Step 1: Direct access to code memory and enable writes.		
0000	8E A6	BSF EECON1, EEPGD
0000	9C A6	BCF EECON1, CFGS
0000	84 A6	BSF EECON1, WREN
Step 2: Point to first row in code memory.		
0000	6A F8	CLRF TBLPTRU
0000	6A F7	CLRF TBLPTRH
0000	6A F6	CLRF TBLPTRL
Step 3: Enable erase and erase single row.		
0000	88 A6	BSF EECON1, FREE
0000	82 A6	BSF EECON1, WR
0000	00 00	NOP
0000	00 00	NOP Erase starts on the 4th clock of this instruction
Step 4: Poll WR bit. Repeat until bit is clear.		
0000	50 A6	MOVF EECON1, W, 0
0000	6E F5	MOVWF TABLAT
0000	00 00	NOP
0010	<MSB><LSB>	Shift out data(1)
Step 5: Hold PGC low for time P10.		
Step 6: Repeat step 3 with Address Pointer incremented by 64 until all rows are erased.		
Step 7: Disable writes.		
0000	94 A6	BCF EECON1, WREN

Note 1: See Figure 4-4 for details on shift out data timing.

FIGURE 3-4: PROGRAM CODE MEMORY FLOW

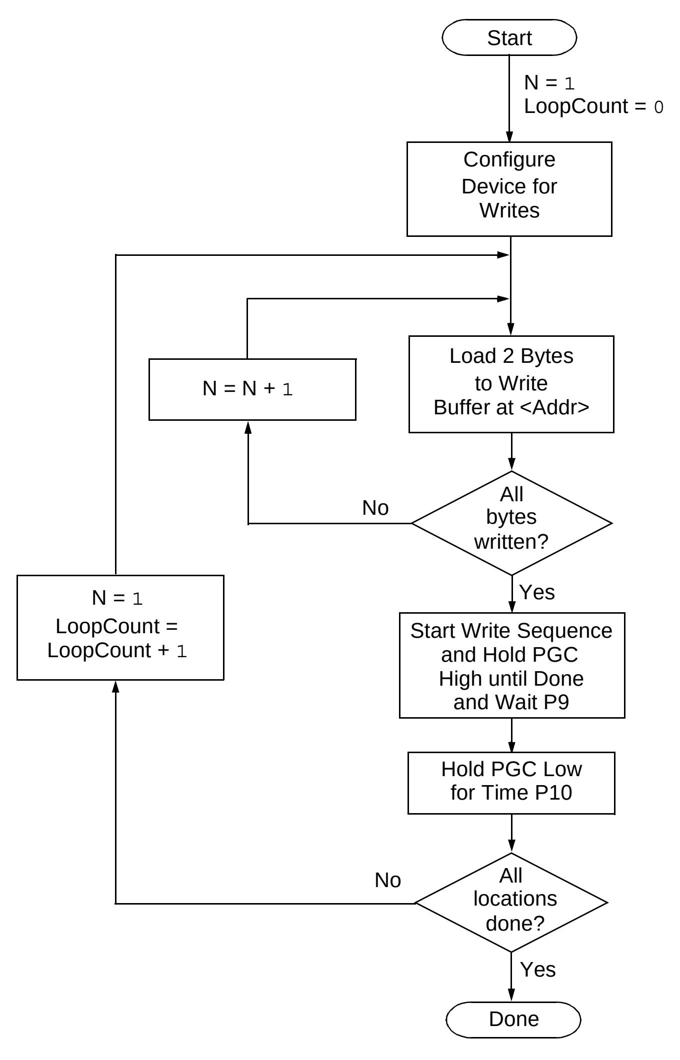
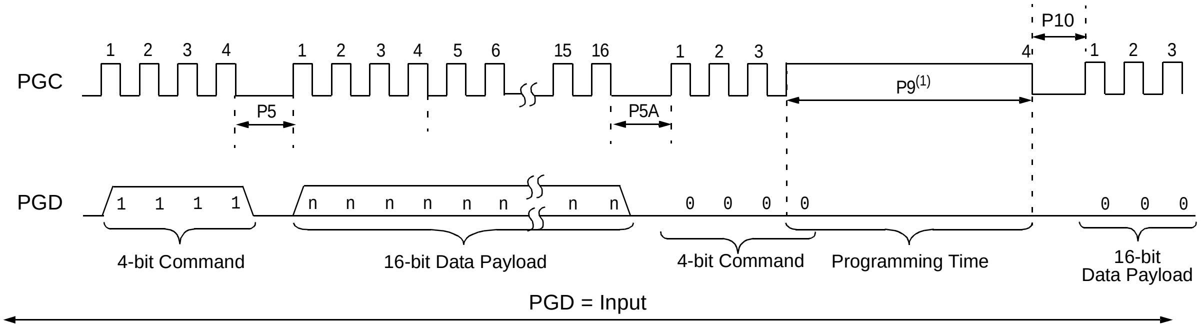


FIGURE 3-5: TABLE WRITE AND START PROGRAMMING INSTRUCTION TIMING DIAGRAM (`1111`)



Note 1: Use P9A for User ID and Configuration Word programming.

3.2.1 MODIFYING CODE MEMORY

The previous programming example assumed that the device has been Bulk Erased prior to programming (see **Section 3.1.1 “High-Voltage ICSP Bulk Erase”**). It may be the case, however, that the user wishes to modify only a section of an already programmed device.

The appropriate number of bytes required for the erase buffer must be read out of code memory (as described in **Section 4.2 “Verify Code Memory and ID Locations”**) and buffered. Modifications can be made on this buffer. Then, the block of code memory that was read out must be erased and rewritten with the modified data.

The WREN bit must be set if the WR bit in EECON1 is used to initiate a write sequence.

TABLE 3-6: MODIFYING CODE MEMORY

4-bit Command	Data Payload	Core Instruction
Step 1: Direct access to code memory.		
0000	8E A6	BSF EECON1, EEPGD
0000	9C A6	BCF EECON1, CFGS
Step 2: Read code memory into buffer (**Section 4.1 “Read Code Memory, ID Locations and Configuration Bits”**).		
Step 3: Set the Table Pointer for the block to be erased.		
0000	0E <Addr[21:16]>	MOVLW <Addr[21:16]>
0000	6E F8	MOVWF TBLPTRU
0000	0E <Addr[8:15]>	MOVLW <Addr[8:15]>
0000	6E F7	MOVWF TBLPTRH
0000	0E <Addr[7:0]>	MOVLW <Addr[7:0]>
0000	6E F6	MOVWF TBLPTRL
Step 4: Enable memory writes and setup an erase.		
0000	84 A6	BSF EECON1, WREN
0000	88 A6	BSF EECON1, FREE
Step 5: Initiate erase.		
0000	88 A6	BSF EECON1, FREE
0000	82 A6	BSF EECON1, WR
0000	00 00	NOP
0000	00 00	NOP Erase starts on the 4th clock of this instruction
Step 6: Poll WR bit. Repeat until bit is clear.		
0000	50 A6	MOVF EECON1, W, 0
0000	6E F5	MOVWF TABLAT
0000	00 00	NOP
0000	<MSB><LSB>	Shift out data(1)
Step 7: Load write buffer. The correct bytes will be selected based on the Table Pointer.		
0000	0E <Addr[21:16]>	MOVLW <Addr[21:16]>
0000	6E F8	MOVWF TBLPTRU
0000	0E <Addr[8:15]>	MOVLW <Addr[8:15]>
0000	6E F7	MOVWF TBLPTRH
0000	0E <Addr[7:0]>	MOVLW <Addr[7:0]>
0000	6E F6	MOVWF TBLPTRL
1101	<MSB><LSB>	Write 2 bytes and post-increment address by 2.
•	•	
•	•	Repeat as many times as necessary to fill the write buffer
•	•	Write 2 bytes and start programming.
1111	<MSB><LSB>	NOP - hold PGC high for time P9 and low for time P10.
0000	00 00	
To continue modifying data, repeat Steps 2 through 6, where the Address Pointer is incremented by the appropriate number of bytes (see Table 3-4) at each iteration of the loop. The write cycle must be repeated enough times to completely rewrite the contents of the erase buffer.		
Step 8: Disable writes.		
0000	94 A6	BCF EECON1, WREN

3.3 Data EEPROM Programming

Data EEPROM is accessed one byte at a time via an Address Pointer (register pair EEADRH:EEADR) and a data latch (EEDATA). Data EEPROM is written by loading EEADRH:EEADR with the desired memory location, EEDATA with the data to be written and initiating a memory write by appropriately configuring the EECON1 register. A byte write automatically erases the location and writes the new data (erase-before-write).

When using the EECON1 register to perform a data EEPROM write, both the EEPGD and CFGS bits must be cleared (EECON1<7:6> = `00`). The WREN bit must be set (EECON1<2> = `1`) to enable writes of any sort and this must be done prior to initiating a write sequence. The write sequence is initiated by setting the WR bit (EECON1<1> = `1`).

The write begins on the falling edge of the 24th PGC after the WR bit is set. It ends when the WR bit is cleared by hardware.

After the programming sequence terminates, PGC must be held low for the time specified by parameter P10 to allow high-voltage discharge of the memory array.

FIGURE 3-6: PROGRAM DATA FLOW

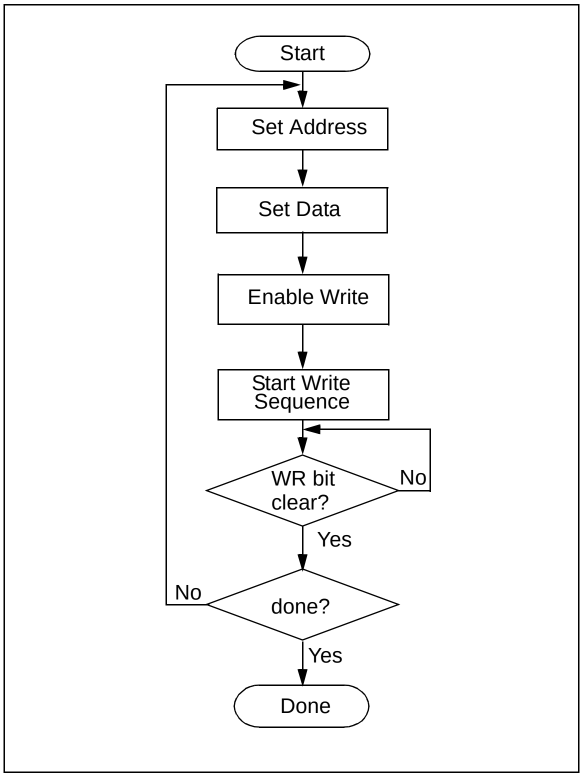


FIGURE 3-7: DATA EEPROM WRITE TIMING DIAGRAM

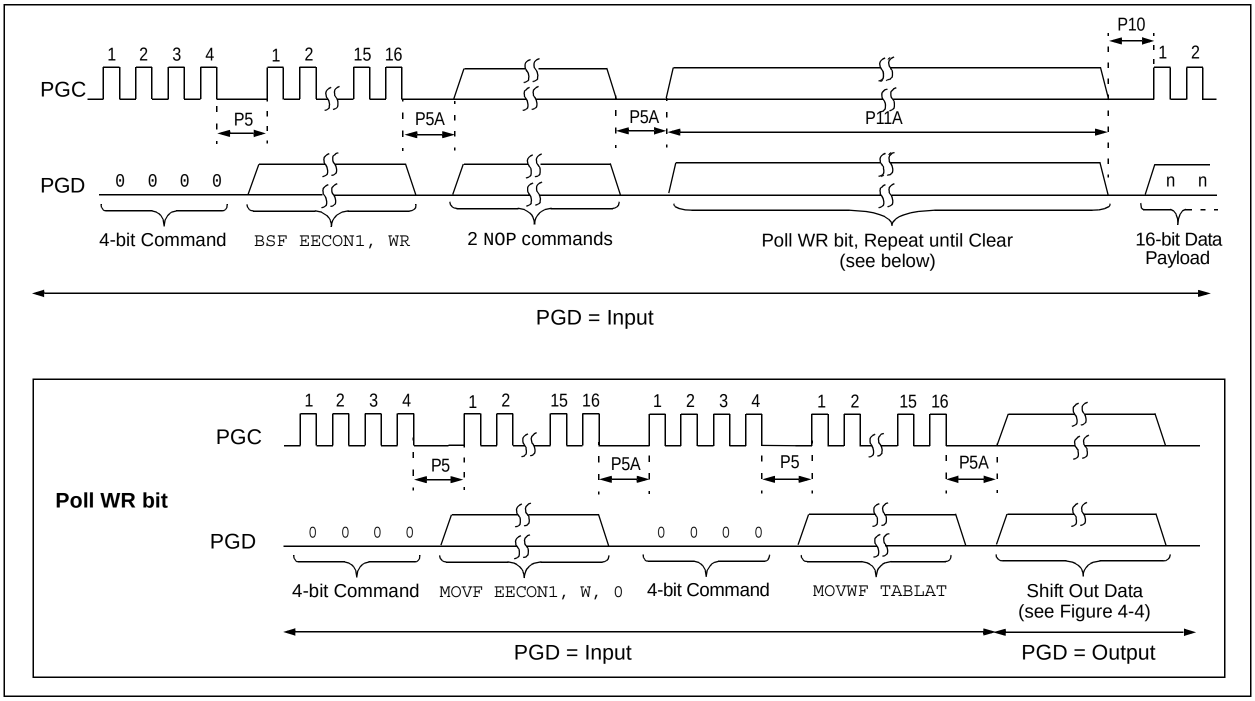


TABLE 3-7: PROGRAMMING DATA MEMORY

4-bit Command	Data Payload	Core Instruction
Step 1: Direct access to data EEPROM.		
`0000` `0000`	9E A6 9C A6	`BCF EECON1, EEPGD` `BCF EECON1, CFGS`
Step 2: Set the data EEPROM Address Pointer.		

`0000`
`0000`
`0000`
`0000`
	0E <Addr>
	6E A9
	OE <AddrH>
	6E AA
		`MOVLW <Addr>`
		`MOVWF EEADR`
		`MOVLW <AddrH>`
		`MOVWF EEADRH`

Step 3: Load the data to be written.		
`0000` `0000`	0E <Data> 6E A8	`MOVLW <Data>` `MOVWF EEDATA`
Step 4: Enable memory writes.		
`0000`	84 A6	`BSF EECON1, WREN`
Step 5: Initiate write.		

`0000`
`0000`
`0000`
	82 A6
	00 00
	00 00
		`BSF EECON1, WR`
		`NOP`
		`NOP ;write starts on 4th clock of this instruction`

Step 6: Poll WR bit, repeat until the bit is clear.		

`0000`
`0000`
`0000`
`0010`
	50 A6
	6E F5
	00 00
	<MSB><LSB>
		`MOVF EECON1, W, 0`
		`MOVWF TABLAT`
		`NOP`
		`Shift out data`(1)

Step 7: Hold PGC low for time P10.		
Step 8: Disable writes.		
`0000`	94 A6	`BCF EECON1, WREN`
Repeat steps 2 through 8 to write more data.		

Note 1: See Figure 4-4 for details on shift out data timing.

4.0 READING THE DEVICE

4.1 Read Code Memory, ID Locations and Configuration Bits

Code memory is accessed one byte at a time via the 4-bit command, '`1001`' (table read, post-increment). The contents of memory pointed to by the Table Pointer (TBLPTRU:TBLPTRH:TBLPTRL) are serially output on PGD.

The 4-bit command is shifted in LSb first. The read is executed during the next 8 clocks, then shifted out on PGD during the last 8 clocks, LSb to MSb. A delay of P6 must be introduced after the falling edge of the 8th PGC of the operand to allow PGD to transition from an input to an output. During this time, PGC must be held low (see Figure 4-1). This operation also increments the Table Pointer by one, pointing to the next byte in code memory for the next read.

This technique will work to read any memory in the 000000h to 3FFFFFh address space, so it also applies to the reading of the ID and Configuration registers.

Note:	When table read protection is enabled, the first read access to a protected block should be discarded and the read repeated to retrieve valid data. Subsequent reads of the same block can be performed normally.

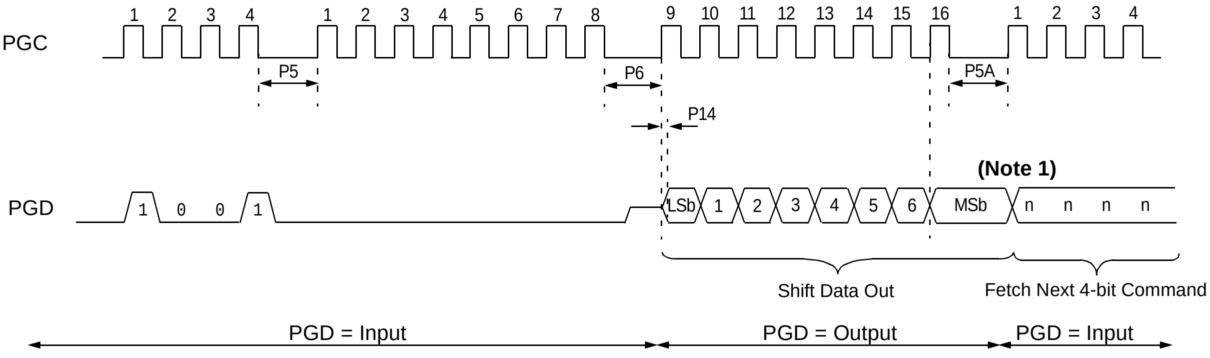
TABLE 4-1: READ CODE MEMORY SEQUENCE

4-bit Command	Data Payload	Core Instruction
Step 1: Set Table Pointer		

`0000`
`0000`
`0000`
`0000`
`0000`
`0000`
	0E <Addr[21:16]>
	6E F8
	0E <Addr[15:8]>
	6E F7
	0E <Addr[7:0]>
	6E F6
		`MOVLW Addr[21:16]`
		`MOVWF TBLPTRU`
		`MOVLW <Addr[15:8]>`
		`MOVWF TBLPTRH`
		`MOVLW <Addr[7:0]>`
		`MOVWF TBLPTRL`

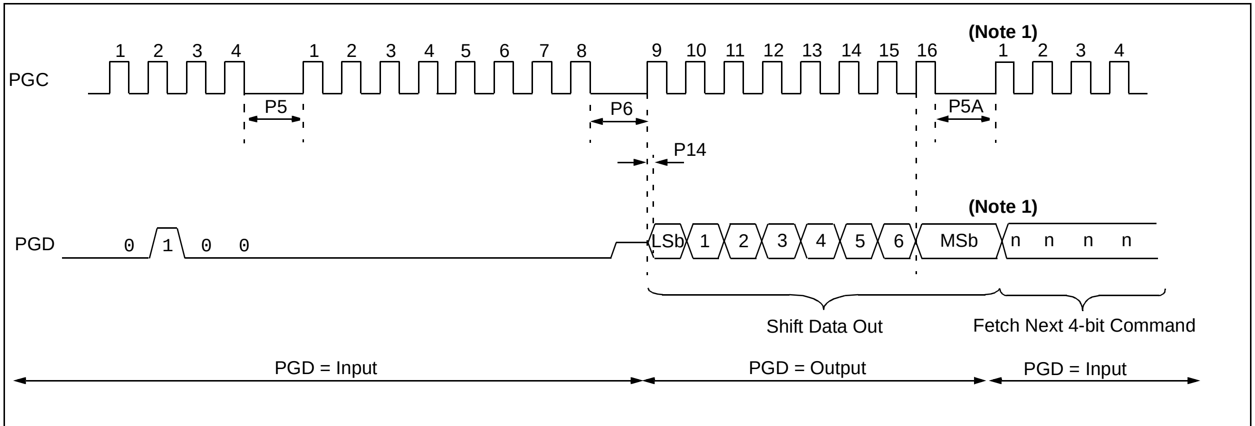
Step 2: Read memory and then shift out on PGD, LSb to MSb		
`1001`	00 00	`TBLRD *+`

FIGURE 4-1: TABLE READ POST-INCREMENT INSTRUCTION TIMING DIAGRAM (`1001`)



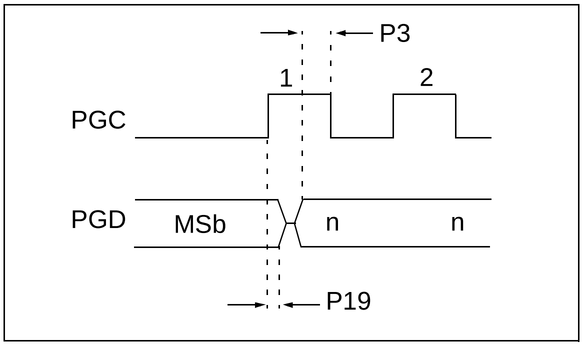
Note 1: Magnification of the high-impedance delay between PGC and PGD is shown in Figure 4-6.

FIGURE 4-4: SHIFT OUT DATA HOLDING REGISTER TIMING DIAGRAM (`0010`)



Note 1: Magnification of the High-Impedance delay between PGC and PGD is shown in Figure 4-5.

FIGURE 4-5: HIGH-IMPEDANCE DELAY



4.5 Verify Data EEPROM

A data EEPROM address may be read via a sequence of core instructions (4-bit command, ‘`0000`’) and then output on PGD via the 4-bit command, ‘`0010`’ (TABLAT register). The result may then be immediately compared to the appropriate data in the programmer’s memory for verification. Refer to **Section 4.4 “Read Data EEPROM Memory”** for implementation details of reading data EEPROM.

4.6 Blank Check

The term “Blank Check” means to verify that the device has no programmed memory cells. All memories must be verified: code memory, data EEPROM, ID locations and Configuration bits. The device ID registers (3FFFFEh:3FFFFFh) should be ignored.

A “blank” or “erased” memory cell will read as a ‘`1`’. Therefore, Blank Checking a device merely means to verify that all bytes read as FFh except the Configuration bits. Unused (reserved) Configuration bits will read ‘`0`’ (programmed). Refer to Table 5-1 for blank configuration expect data for the various PIC18F2XK20/4XK20 devices.

Given that Blank Checking is merely code and data EEPROM verification with FFh expect data, refer to **Section 4.4 “Read Data EEPROM Memory”** and **Section 4.2 “Verify Code Memory and ID Locations”** for implementation details.

FIGURE 4-6: BLANK CHECK FLOW

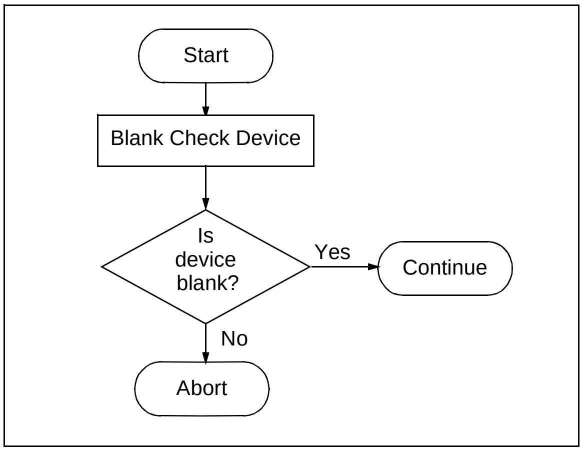


TABLE 5-3: PIC18F2XK20/4XK20 BIT DESCRIPTIONS (CONTINUED)

Bit Name	Configuration Words	Description
CP3	CONFIG5L	Code Protection bits (Block 3 code memory area) `1` = Block 3 is not code-protected `0` = Block 3 is code-protected
CP2	CONFIG5L	Code Protection bits (Block 2 code memory area) `1` = Block 2 is not code-protected `0` = Block 2 is code-protected
CP1	CONFIG5L	Code Protection bits (Block 1 code memory area) `1` = Block 1 is not code-protected `0` = Block 1 is code-protected
CP0	CONFIG5L	Code Protection bits (Block 0 code memory area) `1` = Block 0 is not code-protected `0` = Block 0 is code-protected
CPD	CONFIG5H	Code Protection bits (Data EEPROM) `1` = Data EEPROM is not code-protected `0` = Data EEPROM is code-protected
CPB	CONFIG5H	Code Protection bits (Boot Block memory area) `1` = Boot Block is not code-protected `0` = Boot Block is code-protected
WRT3	CONFIG6L	Write Protection bits (Block 3 code memory area) `1` = Block 3 is not write-protected `0` = Block 3 is write-protected
WRT2	CONFIG6L	Write Protection bits (Block 2 code memory area) `1` = Block 2 is not write-protected `0` = Block 2 is write-protected
WRT1	CONFIG6L	Write Protection bits (Block 1 code memory area) `1` = Block 1 is not write-protected `0` = Block 1 is write-protected
WRT0	CONFIG6L	Write Protection bits (Block 0 code memory area) `1` = Block 0 is not write-protected `0` = Block 0 is write-protected
WRTD	CONFIG6H	Write Protection bit (Data EEPROM) `1` = Data EEPROM is not write-protected `0` = Data EEPROM is write-protected
WRTB	CONFIG6H	Write Protection bit (Boot Block memory area) `1` = Boot Block is not write-protected `0` = Boot Block is write-protected
WRTC	CONFIG6H	Write Protection bit (Configuration registers) `1` = Configuration registers are not write-protected `0` = Configuration registers are write-protected

.

TABLE 5-3: PIC18F2XK20/4XK20 BIT DESCRIPTIONS (CONTINUED)

Bit Name	Configuration Words	Description
EBTR3	CONFIG7L	Table Read Protection bit (Block 3 code memory area) `1` = Block 3 is not protected from table reads executed in other blocks `0` = Block 3 is protected from table reads executed in other blocks
EBTR2	CONFIG7L	Table Read Protection bit (Block 2 code memory area) `1` = Block 2 is not protected from table reads executed in other blocks `0` = Block 2 is protected from table reads executed in other blocks
EBTR1	CONFIG7L	Table Read Protection bit (Block 1 code memory area) `1` = Block 1 is not protected from table reads executed in other blocks `0` = Block 1 is protected from table reads executed in other blocks
EBTR0	CONFIG7L	Table Read Protection bit (Block 0 code memory area) `1` = Block 0 is not protected from table reads executed in other blocks `0` = Block 0 is protected from table reads executed in other blocks
EBTRB	CONFIG7H	Table Read Protection bit (Boot Block memory area) `1` = Boot Block is not protected from table reads executed in other blocks `0` = Boot Block is protected from table reads executed in other blocks
DEV<10:3>	DEVID2	Device ID bits These bits are used with the DEV<2:0> bits in the DEVID1 register to identify part number.
DEV<2:0>	DEVID1	Device ID bits These bits are used with the DEV<10:3> bits in the DEVID2 register to identify part number.
REV<4:0>	DEVID1	Revision ID bits These bits are used to indicate the revision of the device.

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6.0 AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE

Standard Operating Conditions
Operating Temperature: 25°C is recommended

Param No.	Sym.	Characteristic	Min.	Max.	Units	Conditions
D110	VIHH	High-Voltage Programming Voltage on $\overline{\text{MCLR}}$/VPP/RE3	VDD + 4.5	9	V	
D110A	VIHL	Low-Voltage Programming Voltage on $\overline{\text{MCLR}}$/VPP/RE3	1.80	3.60	V	
D111	VDD	Supply Voltage During Programming	1.80	3.60	V	Row Erase/Write
			2.7	3.60	V	Bulk Erase operations
D112	IPP	Programming Current on $\overline{\text{MCLR}}$/VPP/RE3	—	300	μA	
D113	IDDP	Supply Current During Programming	—	10	mA	
D031	VIL	Input Low Voltage	VSS	0.2 VDD	V	
D041	VIH	Input High Voltage	0.8 VDD	VDD	V	
D080	VOL	Output Low Voltage	—	0.6	V	IOL = X.X mA @ 2.7V
D090	VOH	Output High Voltage	VDD – 0.7	—	V	IOH = -Y.Y mA @ 2.7V
D012	CIO	Capacitive Loading on I/O pin (PGD)	—	50	pF	To meet AC specifications
P1	TR	$\overline{\text{MCLR}}$/VPP/RE3 Rise Time to enter Program/Verify mode	—	1.0	μs	**(Note 1)**
P2	TPGC	Serial Clock (PGC) Period	100	—	ns	VDD = 3.6V
			1	—	μs	VDD = 1.8V
P2A	TPGCL	Serial Clock (PGC) Low Time	40	—	ns	VDD = 3.6V
			400	—	ns	VDD = 1.8V
P2B	TPGCH	Serial Clock (PGC) High Time	40	—	ns	VDD = 3.6V
			400	—	ns	VDD = 1.8V
P3	TSET1	Input Data Setup Time to Serial Clock ↓	15	—	ns	
P4	THLD1	Input Data Hold Time from PGC ↓	15	—	ns	
P5	TDLY1	Delay between 4-bit Command and Command Operand	40	—	ns	
P5A	TDLY1A	Delay between 4-bit Command Operand and next 4-bit Command	40	—	ns	
P6	TDLY2	Delay between Last PGC ↓ of Command Byte to First PGC ↑ of Read of Data Word	20	—	ns	
P9	TDLY5	PGC High Time (minimum programming time)	1	—	ms	Externally Timed
P9A	TDLY5A	PGC High Time	5		ms	Configuration Word programming time
P10	TDLY6	PGC Low Time after Programming (high-voltage discharge time)	200	—	μs	
P11	TDLY7	Delay to allow Self-Timed Data Write or Bulk Erase to occur	5	—	ms	
P11A	TDRWT	Data Write Polling Time	4	—	ms	

Note 1: Do not allow excess time when transitioning $\overline{\text{MCLR}}$ between VIL and VIHH; this can cause spurious program executions to occur. The maximum transition time is:
1 TCY + TPWRT (if enabled) + 1024 TOSC (for LP, HS, HS/PLL and XT modes only) + 2 ms (for HS/PLL mode only) + 1.5 μs (for EC mode only) where TCY is the instruction cycle time, TPWRT is the Power-up Timer period and TOSC is the oscillator period. For specific values, refer to the Electrical Characteristics section of the device data sheet for the particular device.

6.0 AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/ VERIFY TEST MODE (CONTINUED)

Standard Operating Conditions
Operating Temperature: 25°C is recommended

Param No.	Sym.	Characteristic	Min.	Max.	Units	Conditions
P12	THLD2	Input Data Hold Time from $\overline{\text{MCLR}}$/VPP/RE3 ↑	2	—	µs	
P13	TSET2	VDD ↑ Setup Time to $\overline{\text{MCLR}}$/VPP/RE3 ↑	100	—	ns	
P14	TVALID	Data Out Valid from PGC ↑	10	—	ns	
P15	TSET3	PGM ↑ Setup Time to $\overline{\text{MCLR}}$/VPP/RE3 ↑	2	—	µs	
P16	TDLY8	Delay between Last PGC ↓ and $\overline{\text{MCLR}}$/VPP/RE3 ↓	0	—	s	
P17	THLD3	$\overline{\text{MCLR}}$/VPP/RE3 ↓ to VDD ↓	—	100	ns	
P18	THLD4	$\overline{\text{MCLR}}$/VPP/RE3 ↓ to PGM ↓	0	—	s	
P19	THIZ	Delay from PGC ↑ to PGD High-Z	3	10	nS	
P20	TPPDP	Hold time after VPP changes	5	—	µs	

Note 1: Do not allow excess time when transitioning $\overline{\text{MCLR}}$ between VIL and VIHH; this can cause spurious program executions to occur. The maximum transition time is:
1 TCY + TPWRT (if enabled) + 1024 TOSC (for LP, HS, HS/PLL and XT modes only) + 2 ms (for HS/PLL mode only) + 1.5 µs (for EC mode only) where TCY is the instruction cycle time, TPWRT is the Power-up Timer period and TOSC is the oscillator period. For specific values, refer to the Electrical Characteristics section of the device data sheet for the particular device.

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