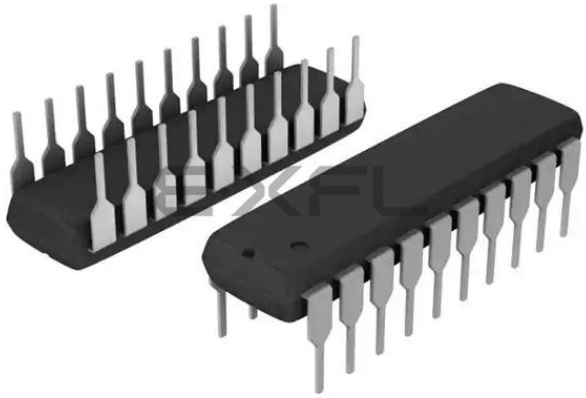

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	15
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7flite25f1b6

2 Pin description

Figure 2. 20-pin SO package pinout

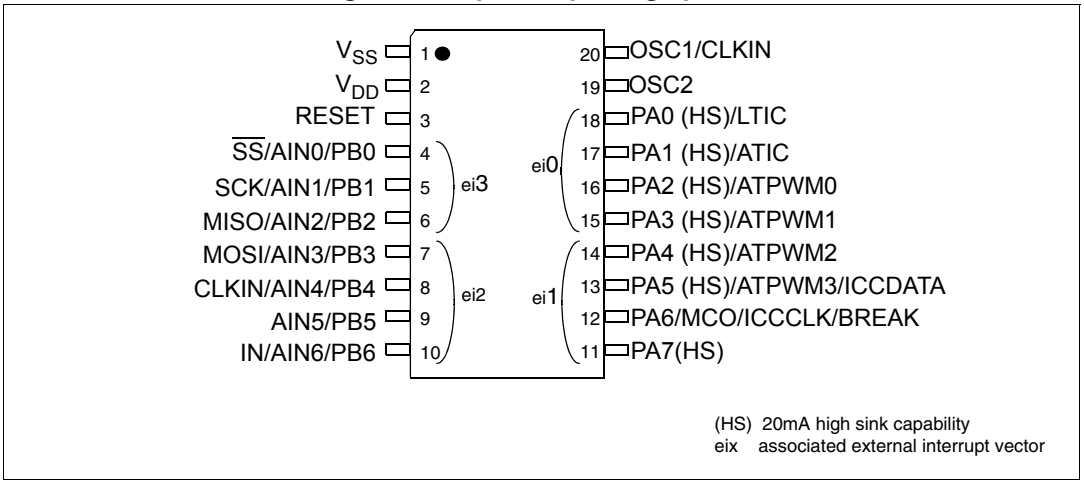
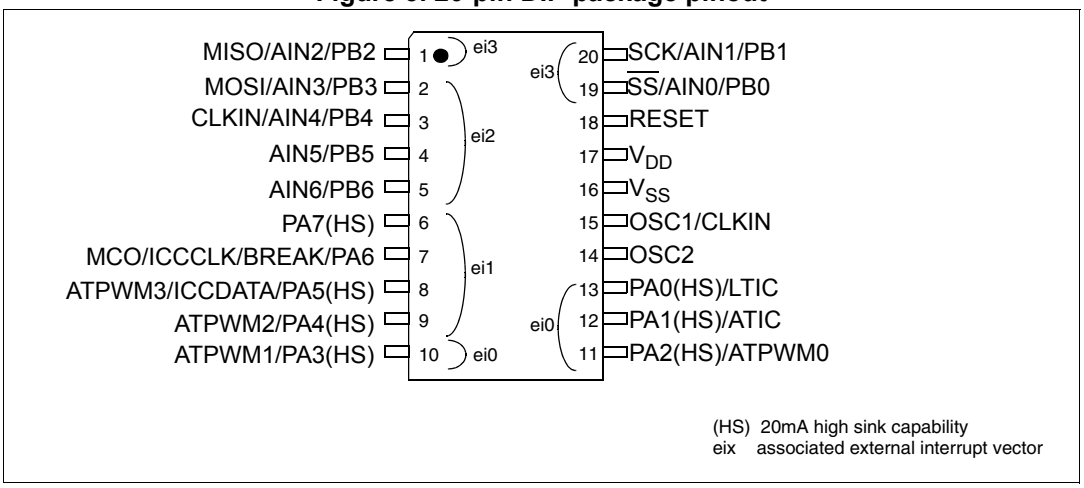


Figure 3. 20-pin DIP package pinout



Legend and abbreviations for device pin description (see *Table 2* below):

- Type:
  - I = input
  - O = output
  - S = supply
- In/Output level:
  - C_T= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger
- Output level:
  - HS = 20mA high sink (on N-buffer only)

5 Data EEPROM

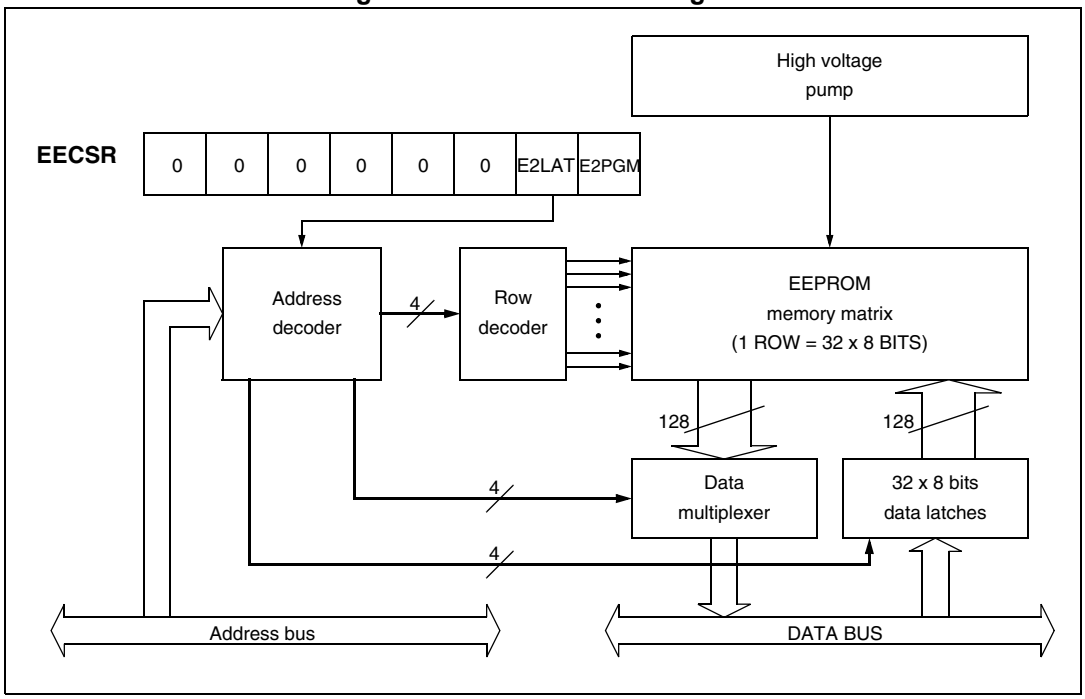
5.1 Introduction

The Electrically Erasable Programmable Read Only Memory can be used as a non-volatile backup for storing data. Using the EEPROM requires a basic access protocol described in this chapter.

5.2 Main features

- Up to 32 bytes programmed in the same cycle
- EEPROM mono-voltage (charge pump)
- Chained erase and programming cycles
- Internal control of the global programming cycle duration
- WAIT mode management
- Read-out protection

Figure 6. EEPROM block diagram



5.3 Memory access

The Data EEPROM memory read/write access modes are controlled by the E2LAT bit of the EEPROM Control/Status register (EECSR). The flowchart in *Figure 7* describes these different memory access modes.

6 Central processing unit

6.1 Introduction

This CPU has a full 8-bit architecture and contains six internal registers allowing efficient 8-bit data manipulation.

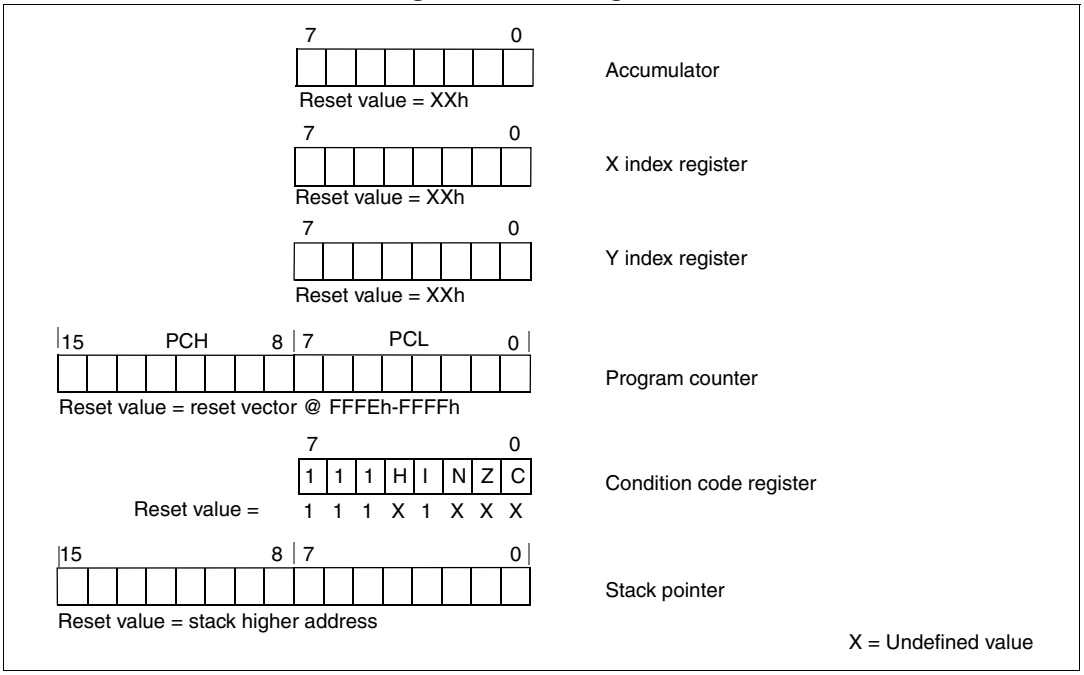
6.2 Main features

- 63 basic instructions
- Fast 8-bit by 8-bit multiply
- 17 main addressing modes
- Two 8-bit index registers
- 16-bit stack pointer
- Low power modes
- Maskable hardware interrupts
- Non-maskable software interrupt

6.3 CPU registers

The 6 CPU registers shown in *Figure 10* are not present in the memory mapping and are accessed by specific instructions.

Figure 10. CPU registers



9 Power saving modes

9.1 Introduction

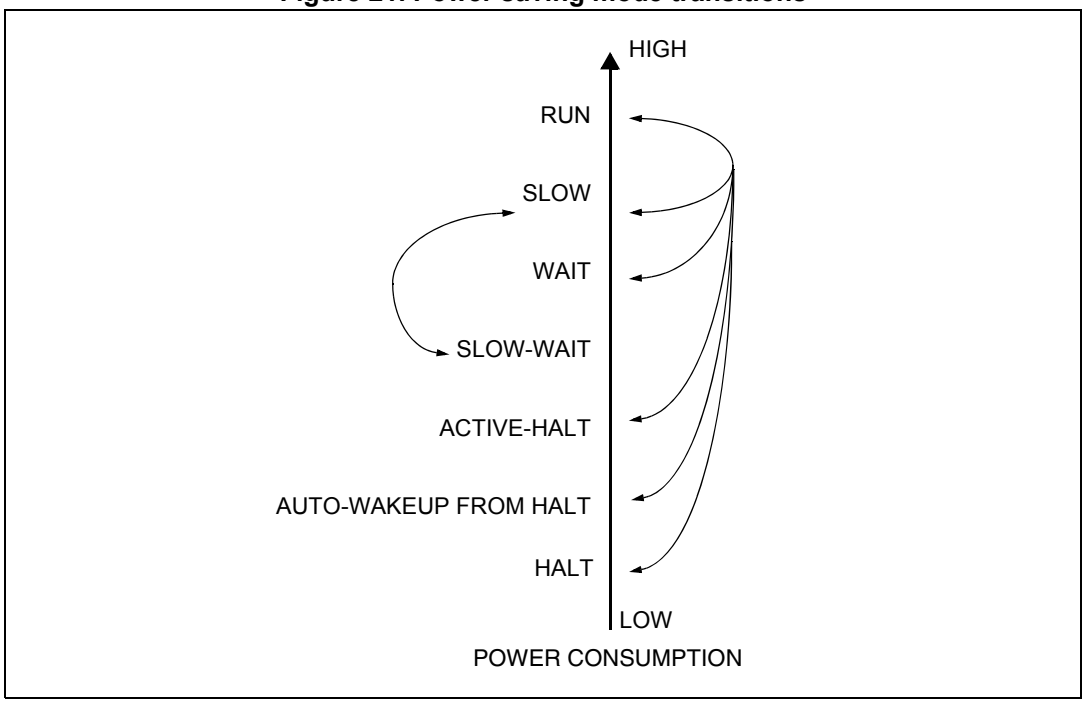
To give a large measure of flexibility to the application in terms of power consumption, five main power saving modes are implemented in the ST7 (see *Figure 21*):

- Slow
- Wait (and Slow-Wait)
- Active Halt
- Auto Wake up From Halt (AWUF)
- Halt

After a RESET the normal operating mode is selected by default (Run mode). This mode drives the device (CPU and embedded peripherals) by means of a master clock which is based on the main oscillator frequency divided or multiplied by 2 (f_{OSC2}).

From RUN mode, the different power saving modes may be selected by setting the relevant register bits or by calling the specific ST7 software instruction whose action depends on the oscillator status.

Figure 21. Power saving mode transitions

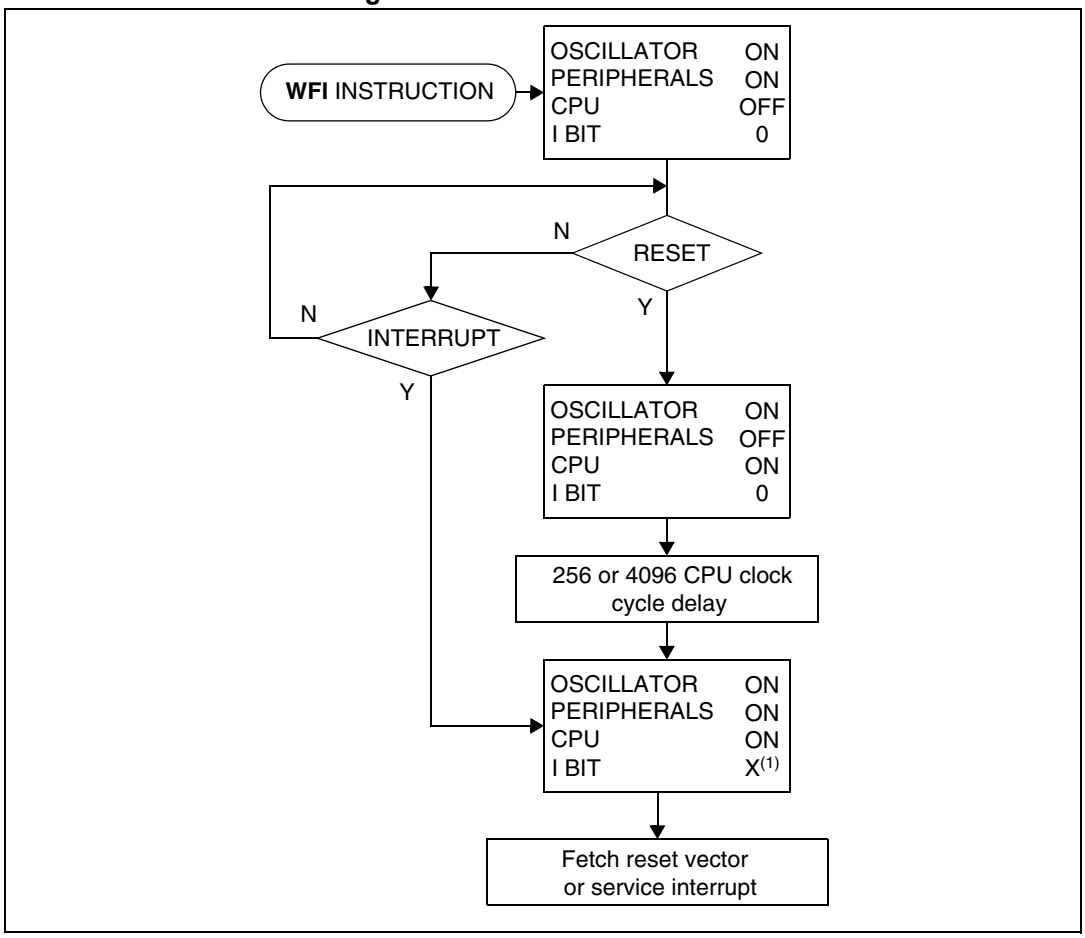


9.2 SLOW mode

This mode has two targets:

- To reduce power consumption by decreasing the internal clock in the device,
- To adapt the internal clock frequency (f_{CPU}) to the available supply voltage.

Figure 23. WAIT mode flowchart



1. Before servicing an interrupt, the CC register is pushed on the stack. The I bit of the CC register is set during the interrupt routine and cleared when the CC register is popped.

9.4 HALT mode

The HALT mode is the lowest power consumption mode of the MCU. It is entered by executing the "HALT" instruction when ACTIVVE-HALT is disabled (see *Section 9.5: ACTIVE-HALT mode* for more details) and when the AWUEN bit in the AWUCSR register is cleared.

The MCU can exit HALT mode on reception of either a specific interrupt (see *Table 12: Interrupt mapping*) or a reset. When exiting HALT mode by means of a reset or an interrupt, the oscillator is immediately turned on and the 256 or 4096 CPU cycle delay is used to stabilize the oscillator. After the startup delay, the CPU resumes operation by servicing the interrupt or by fetching the reset vector which woke it up (see *Figure 25: HALT mode flowchart*).

When entering HALT mode, the I bit in the CC register is forced to 0 to enable interrupts. Therefore, if an interrupt is pending, the MCU wakes up immediately.

In HALT mode, the main oscillator is turned off causing all internal processing to be stopped, including the operation of the on-chip peripherals. All peripherals are not clocked except the

instruction. The main reason for this is that the I/O may be wrongly configured due to external interference or by an unforeseen logical condition.

- For the same reason, reinitialize the level sensitiveness of each external interrupt as a precautionary measure.
- The opcode for the HALT instruction is 0x8E. To avoid an unexpected HALT instruction due to a program counter failure, it is advised to clear all occurrences of the data value 0x8E from memory. For example, avoid defining a constant in program memory with the value 0x8E.
- As the HALT instruction clears the interrupt mask in the CC register to allow interrupts, the user may choose to clear all pending interrupt bits before executing the HALT instruction. This avoids entering other peripheral interrupt routines after executing the external interrupt routine corresponding to the wake-up event (reset or external interrupt).

9.5 ACTIVE-HALT mode

ACTIVE-HALT mode is the lowest power consumption mode of the MCU with a real time clock available. It is entered by executing the 'HALT' instruction.

The decision to enter either in ACTIVEHALT or HALT mode is given by the LTCSR/ATCSR register status as shown in the following table:

Table 18. ACTIVE-HALT mode

LTCSR1 TB1IE bit	ATCSR OVFIE bit	ATCSRCK1 bit	ATCSRCK0 bit	Meaning
0	x	x	0	ACTIVE-HALT mode disabled
0	0	x	x	
1	x	x	x	ACTIVE-HALT mode enabled
x	1	0	1	

The MCU can exit ACTIVE-HALT mode on reception of a specific interrupt (see *Table 12: Interrupt mapping*) or a RESET:

- When exiting ACTIVE-HALT mode by means of a RESET, a 256 or 4096 CPU cycle delay occurs. After the start up delay, the CPU resumes operation by fetching the reset vector which woke it up (see *Figure 27: ACTIVE-HALT mode Flow-chart*).
- When exiting ACTIVE-HALT mode by means of an interrupt, the CPU immediately resumes operation by servicing the interrupt vector which woke it up (see *Figure 27: ACTIVE-HALT mode Flow-chart*).

When entering ACTIVE-HALT mode, the I bit in the CC register is cleared to enable interrupts.

Therefore, if an interrupt is pending, the MCU wakes up immediately.

In ACTIVE-HALT mode, only the main oscillator and the selected timer counter (LT/AT) are running to keep a wake-up time base. All other peripherals are not clocked except those which get their clock supply from another clock generator (such as external or auxiliary oscillator).

11 On-chip peripherals

11.1 Watchdog timer (WDG)

11.1.1 Introduction

The Watchdog timer is used to detect the occurrence of a software fault, usually generated by external interference or by unforeseen logical conditions, which causes the application program to abandon its normal sequence. The Watchdog circuit generates an MCU reset on expiry of a programmed time period, unless the program refreshes the counter's contents before the T6 bit becomes cleared.

11.1.2 Main features

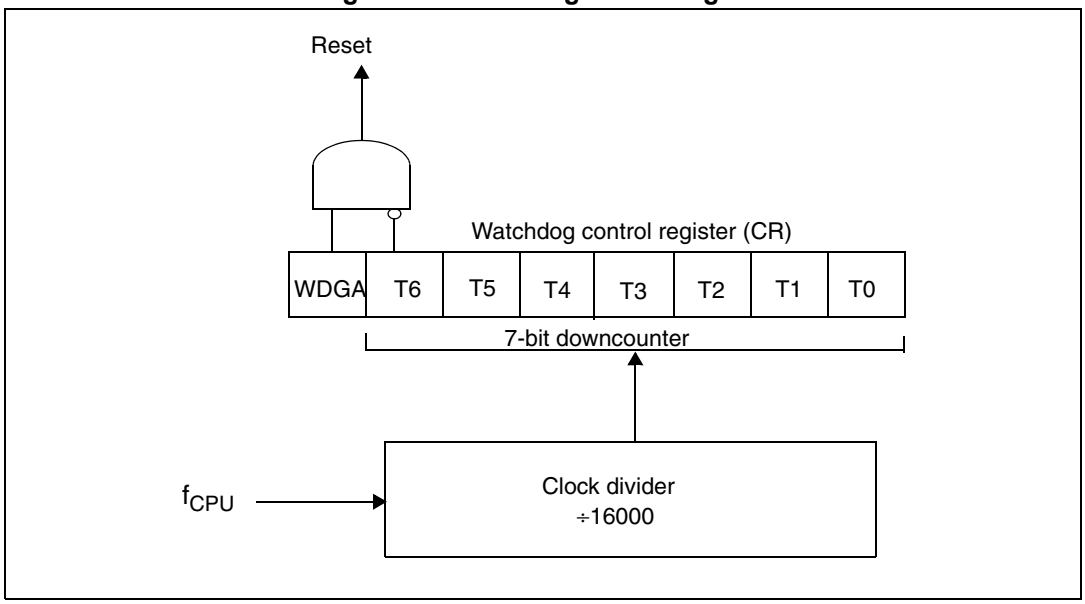
- Programmable free-running downcounter (64 increments of 16000 CPU cycles)
- Programmable reset
- Reset (if watchdog activated) when the T6 bit reaches zero
- Optional reset on HALT instruction (configurable by option byte)
- Hardware Watchdog selectable by option byte.

11.1.3 Functional description

The counter value stored in the CR register (bits T[6:0]), is decremented every 16000 machine cycles, and the length of the time-out period can be programmed by the user in 64 increments.

If the watchdog is activated (the WDGA bit is set) and when the 7-bit timer (bits T[6:0]) rolls over from 40h to 3Fh (T6 becomes cleared), it initiates a reset cycle pulling low the reset pin for typically 30µs.

Figure 33. Watchdog block diagram



11.1.6 Register description

Control register (CR)

Read/Write

Reset value: 0111 1111 (7Fh)

7							0
WDGA	T6	T5	T4	T3	T2	T1	T0

- Bit 7 = **WDGA** *Activation bit*.
  This bit is set by software and only cleared by hardware after a reset.
  When WDGA = 1, the watchdog can generate a reset.
  0: Watchdog disabled
  1: Watchdog enabled

Note: This bit is not used if the hardware watchdog option is enabled by option byte.

- Bits 6:0 = **T[6:0]** *7-bit timer (MSB to LSB).*
  These bits contain the decremented value. A reset is produced when it rolls over from 40h to 3Fh (T6 becomes cleared).

Table 32. Watchdog timer register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
002Eh	WDGCR	WDGA	T6	T5	T4	T3	T2	T1	T0
	Reset value	0	1	1	1	1	1	1	1

11.2 12-bit autoreload timer 2 (AT2)

11.2.1 Introduction

The 12-bit Autoreload Timer can be used for general-purpose timing functions. It is based on a free-running 12-bit upcounter with an input capture register and four PWM output channels. There are 6 external pins:

- Four PWM outputs
- ATIC pin for the Input Capture function
- BREAK pin for forcing a break condition on the PWM outputs.

11.2.6 Register description

Timer control status register (ATCSR)

Read / Write

Reset value: 0x00 0000 (x0h)

7							0
0	ICF	ICIE	CK1	CK0	OVF	OVFIE	CMPIE

- Bit 7 = Reserved.
- Bit 6 = **ICF** *Input capture flag*
  This bit is set by hardware and cleared by software by reading the ATICR register (a read access to ATICRH or ATICRL will clear this flag). Writing to this bit does not change the bit value.
  0: No input capture
  1: An input capture has occurred
- Bit 5 = **ICIE** *IC interrupt enable*
  This bit is set and cleared by software.
  0: Input capture interrupt disabled
  1: Input capture interrupt enabled
- Bits 4:3 = **CK[1:0]** *Counter clock selection*
  These bits are set and cleared by software and cleared by hardware after a reset. They select the clock frequency of the counter.

Table 35. Counter clock selection

Counter clock selection	CK1	CK0
OFF	0	0
f_{LTIMER} (1 ms timebase @ 8 MHz) (1)	0	1
f_{CPU}	1	0
32 MHz (2)	1	1

1. PWM mode and Output Compare modes are not available at this frequency.
2. ATICR counter may return inaccurate results when read. It is therefore not recommended to use Input Capture mode at this frequency.

- Bit 2 = **OVF** *Overflow flag*
  This bit is set by hardware and cleared by software by reading the TCSR register. It indicates the transition of the counter from FFFh to ATR value.
  0: No counter overflow occurred
  1: Counter overflow occurred
- Bit 1 = **OVFIE** *Overflow interrupt enable*
  This bit is read/write by software and cleared by hardware after a reset.
  0: OVF interrupt disabled.
  1: OVF interrupt enabled.
- Bit 0 = **CMPIE** *Compare interrupt enable*
  This bit is read/write by software and cleared by hardware after a reset. It can be used to mask the interrupt generated when the CMPF bit is set.

0: CMPF interrupt disabled.
1: CMPF interrupt enabled.

Counter register high (CNTRH)

Read only

Reset value: 0000 0000 (000h)

15							8
0	0	0	0	CNTR11	CNTR10	CNTR9	CNTR8

Counter register low (CNTRL)

Read only

Reset value: 0000 0000 (000h)

7							0
CNTR7	CNTR6	CNTR5	CNTR4	CNTR3	CNTR2	CNTR1	CNTR0

- Bits 15:12 = Reserved
- Bits 11:0 = **CNTR[11:0]** *Counter value*
  This 12-bit register is read by software and cleared by hardware after a reset. The counter is incremented continuously as soon as a counter clock is selected. To obtain the 12-bit value, software should read the counter value in two consecutive read operations, LSB first. When a counter overflow occurs, the counter restarts from the value specified in the ATR register.

Autoreload register (ATRH)

Read / Write

Reset Value: 0000 0000 (00h)

15							8
0	0	0	0	ATR11	ATR10	ATR9	ATR8

- Bits 15:12 = Reserved
- Bits 11:0 = **ATR[11:0]** *Counter value*
  This 12-bit register is read by software and cleared by hardware after a reset. The counter is incremented continuously as soon as a counter clock is selected. To obtain the 12-bit value, software should read the counter value in two consecutive read operations, LSB first. When a counter overflow occurs, the counter restarts from the value specified in the ATR register.

Autoreload register (ATRL)

Read / Write

Reset Value: 0000 0000 (00h)

7							0
ATR7	ATR6	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0

PWM output control register (PWMCR)

Read/Write

Reset Value: 0000 0000 (00h)

7							0
0	OE3	0	OE2	0	OE1	0	OE0

- Bits 7:0 = **OE[3:0]** *PWMx output enable*
  These bits are set and cleared by software and cleared by hardware after a reset.
  0: PWM mode disabled. PWMx output alternate function disabled: I/O pin free for general purpose I/O after an overflow event.
  1: PWM mode enabled

PWMx control status register (PWMxCSR)

Read / Write

Reset Value: 0000 0000 (00h)

7							0
0	0	0	0	0	0	OPx	OE0

- Bits 7:2 = Reserved, must be kept cleared
- Bit 1 = **OPx** *PWMx Output Polarity*
  This bit is read/write by software and cleared by hardware after a reset. This bit selects the polarity of the PWM signal.
  0: The PWM signal is not inverted
  1: The PWM signal is inverted
- Bit 0 = **CMPFx** PWMx *Compare Flag*
  This bit is set by hardware and cleared by software by reading the PWMxCSR register. It indicates that the upcounter value matches the DCRx register value.
  0: Upcounter value does not match DCR value.
  1: Upcounter value matches DCR value

11.3.3 Functional description

Timebase counter 1

The 8-bit value of Counter 1 cannot be read or written by software. After an MCU reset, it starts incrementing from 0 at a frequency of $f_{OSC}/32$. An overflow event occurs when the counter rolls over from F9h to 00h. If f_{OSC} = 8 MHz, then the time period between two counter overflow events is 1 ms. This period can be doubled by setting the TB bit in the LTCSR1 register.

When Counter 1 overflows, the TB1F bit is set by hardware and an interrupt request is generated if the TB1IE bit is set. The TB1F bit is cleared by software reading the LTCSR1 register.

Input capture

The 8-bit input capture register is used to latch the free-running upcounter (Counter 1) 1 after a rising or falling edge is detected on the LTIC pin. When an input capture occurs, the ICF bit is set and the LTICR1 register contains the MSB of Counter 1. An interrupt is generated if the ICIE bit is set. The ICF bit is cleared by reading the LTICR register.

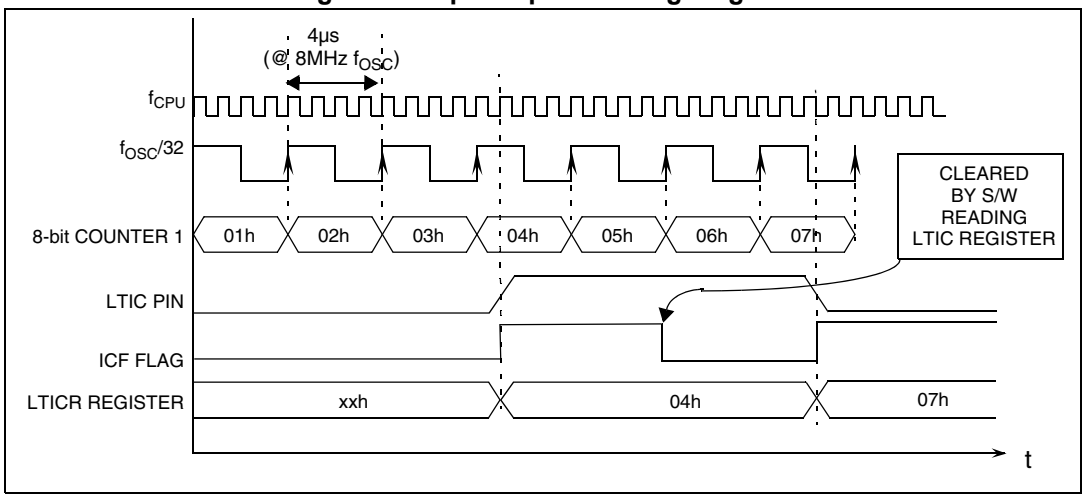
The LTICR is a read-only register and always contains the data from the last input capture. Input capture is inhibited if the ICF bit is set.

Timebase counter 2

Counter 2 is an 8-bit autoreload upcounter. It can be read by accessing the LTCNTR register. After an MCU reset, it increments at a frequency of $f_{OSC}/32$ starting from the value stored in the LTARR register. A counter overflow event occurs when the counter rolls over from FFh to the LTARR reload value. Software can write a new value at anytime in the LTARR register, this value will be automatically loaded in the counter when the next overflow occurs.

When Counter 2 overflows, the TB2F bit in the LTCSR2 register is set by hardware and an interrupt request is generated if the TB2IE bit is set. The TB2F bit is cleared by software reading the LTCSR2 register.

Figure 41. Input capture timing diagram



11.5.4 Low power modes

Table 44. Low power modes effects

Mode	Description
WAIT	No effect on A/D Converter
HALT	A/D Converter disabled. After wakeup from HALT mode, the A/D Converter requires a stabilization time t_{STAB} (see Electrical Characteristics) before accurate conversions can be performed.

Note: The A/D converter may be disabled by resetting the ADON bit. This feature allows reduced power consumption when no conversion is needed and between single shot conversions.

11.5.5 Interrupts

None.

11.5.6 Register Description

Control/status register (ADCCSR)

Read/Write (Except Bit 7 read only)

Reset Value: 0000 0000 (00h)

7							0
EOC	SPEED	ADON	0	CH3	CH2	CH1	CH0

- Bit 7 = **EOC** *End of Conversion*
  This bit is set by hardware. It is cleared by software reading the ADCDRH register.
  0: Conversion is not complete
  1: Conversion complete.
- Bit 6 = **SPEED** *ADC clock selection*
  This bit is set and cleared by software. It is used together with the SLOW bit to configure the ADC clock speed. Refer to the table in the SLOW bit description.
- Bit 5 = **ADON** *A/D Converter on*
  This bit is set and cleared by software.
  0: A/D converter and amplifier are switched off
  1: A/D converter and amplifier are switched on.
- Bits 4:3 = **Reserved.** Must be kept cleared.
- Bits 2:0 = **CH[2:0]** *Channel Selection*
  These bits are set and cleared by software. They select the analog input to convert.

Table 45. Channel selection bits

Channel pin(1)	CH2	CH1	CH0
AIN0	0	0	0
AIN1	0	0	1
AIN2	0	1	0

Table 53. Short instructions supporting direct, indexed, indirect and indirect indexed addressing modes

Short instructions only	Function
CLR	Clear
INC, DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2 Complement
BSET, BRES	Bit operations
BTJT, BTJF	Bit Test and Jump operations
SLL, SRL, SRA, RLC, RRC	Shift and Rotate operations
SWAP	Swap nibbles
CALL, JP	Call or Jump sub-routine

12.1.7 Relative mode (direct, indirect)

This addressing mode is used to modify the PC register value, by adding an 8-bit signed offset to it.

Table 54. Relative direct and indirect instructions and functions

Available relative direct/indirect instructions	Function
JRxx	Conditional Jump
CALLR	Call Relative

The relative addressing mode consists of two submodes:

- Relative (direct)
  The offset follows the opcode.
- Relative (indirect)
  The offset is defined in the memory, the address of which follows the opcode.

12.2 Instruction groups

The ST7 family devices use an Instruction Set consisting of 63 instructions. The instructions may be subdivided into 13 main groups as illustrated in *Table 55*:

Table 55. Instruction groups

Group	Instructions							
Load and Transfer	LD	CLR	–	–	–	–	–	–
Stack operation	PUSH	POP	RSP	–	–	–	–	–
Increment/Decrement	INC	DEC	–	–	–	–	–	–
Compare and Tests	CP	TNZ	BCP	–	–	–	–	–
Logical operations	AND	OR	XOR	CPL	NEG	–	–	–

Table 56. Instruction set overview (continued)

Mnemo	Description	Function/example	Dst	Src	H	I	N	Z	C
JRUGT	Jump if (C + Z = 0)	Unsigned >	–	–	–	–	–	–	–
JRULE	Jump if (C + Z = 1)	Unsigned <=	–	–	–	–	–	–	–
LD	Load	dst <= src	reg, M	M, reg	–	–	N	Z	–
MUL	Multiply	X,A = X * A	A, X, Y	X, Y, A	0	–	–	–	0
NEG	Negate (2's compl)	neg $10	reg, M	–	–	–	N	Z	C
NOP	No Operation	–	–	–	–	–	–	–	–
OR	OR operation	A = A + M	A	M	–	–	N	Z	–
POP	Pop from the Stack	pop reg	reg	M	–	–	–	–	–
		pop CC	CC	M	H	I	N	Z	C
PUSH	Push onto the Stack	push Y	M	reg, CC	–	–	–	–	–
RCF	Reset carry flag	C = 0	–	–	–	–	–	–	0
RET	Subroutine return	–	–	–	–	–	–	–	–
RIM	Enable Interrupts	I = 0	–	–	–	0	–	–	–
RLC	Rotate Left true C	C <= Dst <= C	reg, M	–	–	–	N	Z	C
RRC	Rotate Right true C	C => Dst => C	reg, M	–	–	–	N	Z	C
RSP	Reset Stack Pointer	S = Max allowed	–	–	–	–	–	–	–
SBC	Subtract with Carry	A = A - M - C	A	M	–	–	N	Z	C
SCF	Set carry flag	C = 1	–	–	–	–	–	–	1
SIM	Disable Interrupts	I = 1	–	–	–	1	–	–	–
SLA	Shift Left Arithmetic	C <= Dst <= 0	reg, M	–	–	–	N	Z	C
SLL	Shift Left Logic	C <= Dst <= 0	reg, M	–	–	–	N	Z	C
SRL	Shift Right Logic	0 => Dst => C	reg, M	–	–	–	0	Z	C
SRA	Shift Right Arithmetic	Dst7 => Dst => C	reg, M	–	–	–	N	Z	C
SUB	Subtraction	A = A - M	A	M	–	–	N	Z	C
SWAP	SWAP nibbles	Dst[7..4] <=> Dst[3..0]	reg, M	–	–	–	N	Z	–
TNZ	Test for Neg and Zero	tnz lbl1	–	–	–	–	N	Z	–
TRAP	S/W TRAP	S/W interrupt	–	–	–	1	–	–	–
WFI	WAIT for Interrupt	–	–	–	–	0	–	–	–
XOR	Exclusive OR	A = A XOR M	A	M	–	–	N	Z	–

13 Electrical characteristics

13.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

13.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A=25°C and T_A=$T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

13.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25 °C, V_{DD}=5 V (for the 4.5V≤V_{DD}≤ 5.5 V voltage range) and V_{DD}=3.3 V (for the 3 V≤V_{DD}≤4 V voltage range). They are given only as design guidelines and are not tested.

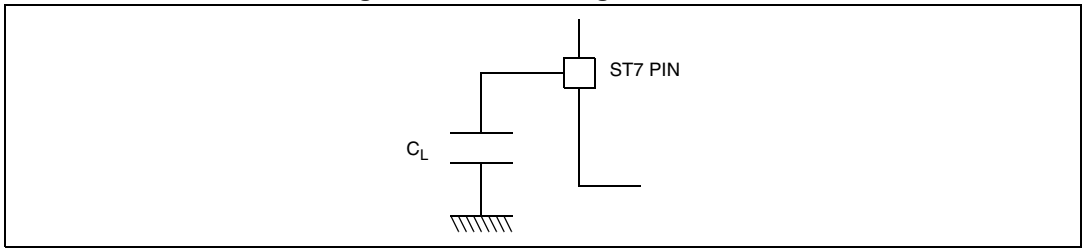
13.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

13.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 50*.

Figure 50. Pin loading conditions



13.1.5 Pin input voltage

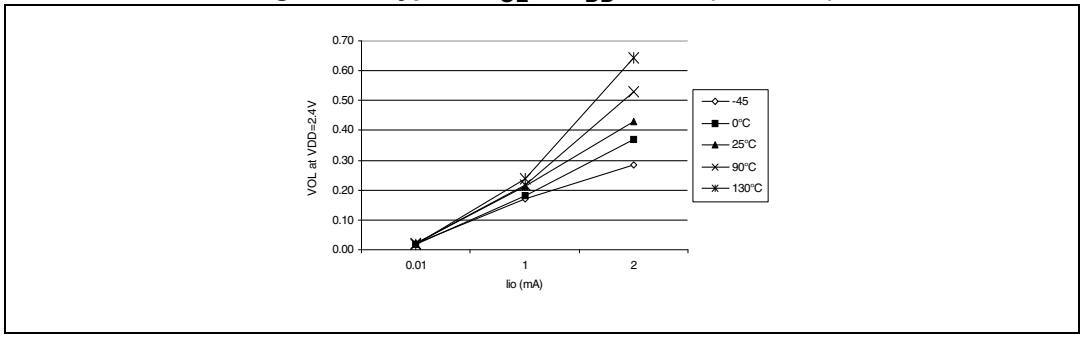
The input voltage measurement on a pin of the device is described in *Figure 51*.

Table 81. Output driving current(1)

Symbol	Parameter	Conditions		Min	Max	Unit
V_{OL}(2)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time (see *Figure 72*)	V_{DD}=5V	I_{IO}=+5mA $T_A \le 85°C$ $T_A \ge 85°C$		1.0 1.2	V
			I_{IO}=+2mA $T_A \le 85°C$ $T_A \ge 85°C$		0.4 0.5	
	Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time (see *Figure 74*)		I_{IO}=+20mA $T_A \le 85°C$ $T_A \ge 85°C$		1.3 1.5	
			I_{IO}=+8mA $T_A \le 85°C$ $T_A \ge 85°C$		0.75 0.85	
V_{OH}(3)	Output high level voltage for an I/O pin when 4 pins are sourced at same time (see *Figure 80*)		I_{IO}=-5mA $T_A \le 85°C$ $T_A \ge 85°C$	V_{DD}-1.5 V_{DD}-1.6		
			I_{IO}=-2mA $T_A \le 85°C$ $T_A \ge 85°C$	V_{DD}-0.8 V_{DD}-1.0		
V_{OL}(2)(4)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time (see *Figure 71*)	V_{DD}=3.3V	I_{IO}=+2mA $T_A \le 85°C$ $T_A \ge 85°C$		0.5 0.6	
	Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time		I_{IO}=+8mA $T_A \le 85°C$ $T_A \ge 85°C$		0.5 0.6	
V_{OH}(3)(4)	Output high level voltage for an I/O pin when 4 pins are sourced at same time		I_{IO}=-2mA $T_A \le 85°C$ $T_A \ge 85°C$	V_{DD}-0.8 V_{DD}-1.0		
V_{OL}(2)(4)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time (see *Figure 69*)	V_{DD}=2.7V	I_{IO}=+2mA $T_A \le 85°C$ $T_A \ge 85°C$		0.6 0.7	
	Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time		I_{IO}=+8mA $T_A \le 85°C$ $T_A \ge 85°C$		0.6 0.7	
V_{OH}(3)(4)	Output high level voltage for an I/O pin when 4 pins are sourced at same time (see *Figure 77*)		I_{IO}=-2mA $T_A \le 85°C$ $T_A \ge 85°C$	V_{DD}-0.9 V_{DD}-1.0		

1. Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A unless otherwise specified.
2. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 58: Current characteristics* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
3. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Table 58: Current characteristics* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Not tested in production, based on characterization results.

Figure 69. Typical V_{OL} at V_{DD} = 2.4V (standard)



14 Package characteristics

14.1 Package mechanical data

Figure 93. 20-pin plastic small outline package, 300-mil width

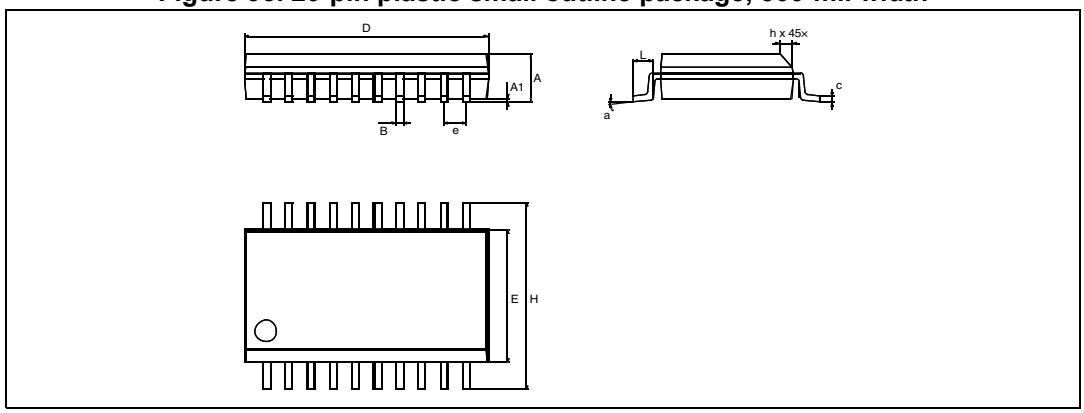


Table 88. Small outline package characteristics

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.35	–	2.65	0.093	–	0.104
A1	0.10	–	0.30	0.004	–	0.012
B	0.33	–	0.51	0.013	–	0.020
C	0.23	–	0.32	0.009	–	0.013
D(1)	12.60	–	13.00	0.496	–	0.512
E	7.40	–	7.60	0.291	–	0.299
e	–	1.27	–	–	0.050	–
H	10.00	–	10.65	0.394	–	0.419
h	0.25	–	0.75	0.010	–	0.030
α	0°	–	8°	0°	–	8°
L	0.40	–	1.27	0.016	–	0.050
	Number of Pins					
N	20					

1. *Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side*

15 Device configuration

Each device is available for production in user programmable versions (FLASH) as well as in factory coded versions (FASTROM).

ST7FLITE2 devices are FLASH versions. ST7PLITE2 devices are Factory Advanced Service Technique ROM (FASTROM) versions: they are factory programmed FLASH devices.

ST7FLITE2 devices are shipped to customers with a default program memory content (FFh), while FASTROM factory coded parts contain the code supplied by the customer. This implies that FLASH devices have to be configured by the customer using the Option Bytes while the FASTROM devices are factory configured.

15.1 Option bytes

The two option bytes allow the hardware configuration of the microcontroller to be selected.

The option bytes can be accessed only in programming mode (for example using a standard ST7 programming tool).

15.1.1 Option byte 0

- OPT7 = Reserved, must always be 1
- OPT6:4 = **OSCRANGE[2:0]** *Oscillator range*
  When the internal RC oscillator is not selected (Option OSC=1), these option bits select the range of the resonator oscillator current source or the external clock source.

Table 92. Option bytes values

			OSCRANGE		
			2	**1**	**0**
Typ. frequency range with Resonator	LP	1~2MHz	0	0	0
	MP	2~4MHz	0	0	1
	MS	4~8MHz	0	1	0
	HS	8~16MHz	0	1	1
	VLP	32.768kHz	1	0	0
External Clock source: CLKIN	on OSC1		1	0	1
	on PB4		1	1	1
Reserved			1	1	0

Note: When the internal RC oscillator is selected, the OSCRANGE option bits must be kept at their default value in order to select the 256 clock cycle delay (see Section 7.5: Reset sequence manager (RSM)).

- OPT3:2 = **SEC[1:0]** *Sector 0 size definition*
  These option bits indicate the size of sector 0 according to *Table 93*.