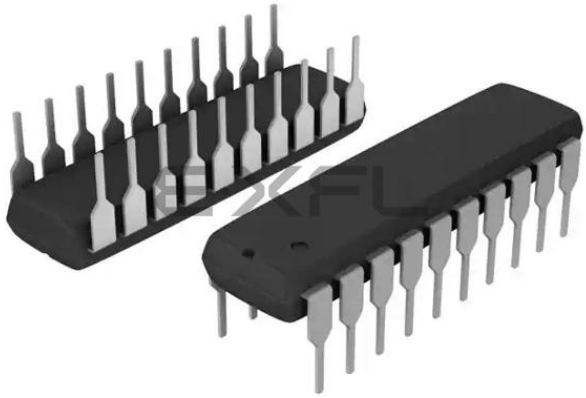

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	15
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7flite25f2b6

Read operation (E2LAT=0)

The EEPROM can be read as a normal ROM location when the E2LAT bit of the EECSR register is cleared.

On this device, Data EEPROM can also be used to execute machine code. Take care not to write to the Data EEPROM while executing from it. This would result in an unexpected code being executed.

Write operation (E2LAT=1)

To access the write mode, the E2LAT bit has to be set by software (the E2PGM bit remains cleared). When a write access to the EEPROM area occurs, the value is latched inside the 32 data latches according to its address.

When PGM bit is set by the software, all the previous bytes written in the data latches (up to 32) are programmed in the EEPROM cells. The effective high address (row) is determined by the last EEPROM write sequence. To avoid wrong programming, the user must take care that all the bytes written between two programming sequences have the same high address: only the five Least Significant Bits of the address can change.

At the end of the programming cycle, the PGM and LAT bits are cleared simultaneously.

Note: Care should be taken during the programming cycle. Writing to the same memory location will over-program the memory (logical AND between the two write access data result) because the data latches are only cleared at the end of the programming cycle and by the falling edge of the E2LAT bit.
It is not possible to read the latched data.
This note is illustrated by the Figure 9: Data EEPROM programming cycle.

Figure 7. Data EEPROM programming flowchart

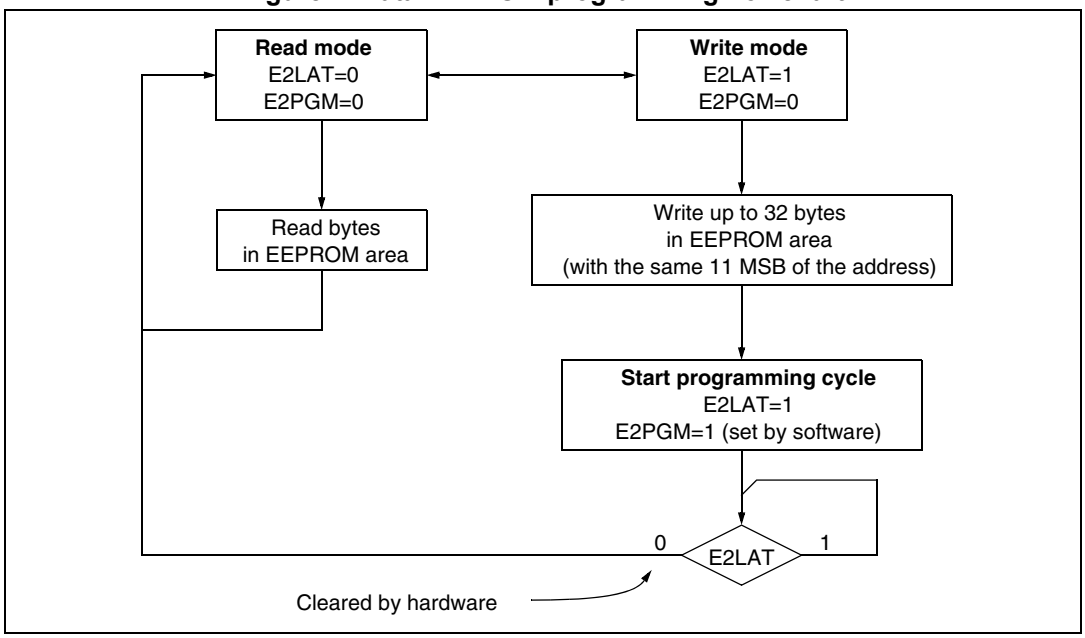


Table 5. DATA EEPROM register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0030h	**EECSR** Reset Value	0	0	0	0	0	0	E2LAT 0	E2PGM 0

Note: See Section 13: Electrical characteristics for more information on the frequency and accuracy of the RC oscillator.

To improve clock stability and frequency accuracy, it is recommended to place a decoupling capacitor, typically 100nF, between the V_{DD} and V_{SS} pins as close as possible to the ST7 device.

These two bytes are systematically programmed by ST, including on FASTROM devices. Consequently, customers intending to use FASTROM service must not use these two bytes.

RCCR0 and RCCR1 calibration values will be erased if the Read-out protection bit is reset after it has been set. See *Section 4.5.1: Read-out protection*.

Caution: If the voltage or temperature conditions change in the application, the frequency may need to be recalibrated.
Refer to application note AN1324 for information on how to calibrate the RC frequency using an external reference signal.

7.2 Phase locked loop (PLL)

The PLL can be used to multiply a 1 MHz frequency from the RC oscillator or the external clock by 4 or 8 to obtain f_{OSC} of 4 or 8 MHz. The PLL is enabled and the multiplication factor of 4 or 8 is selected by 2 option bits.

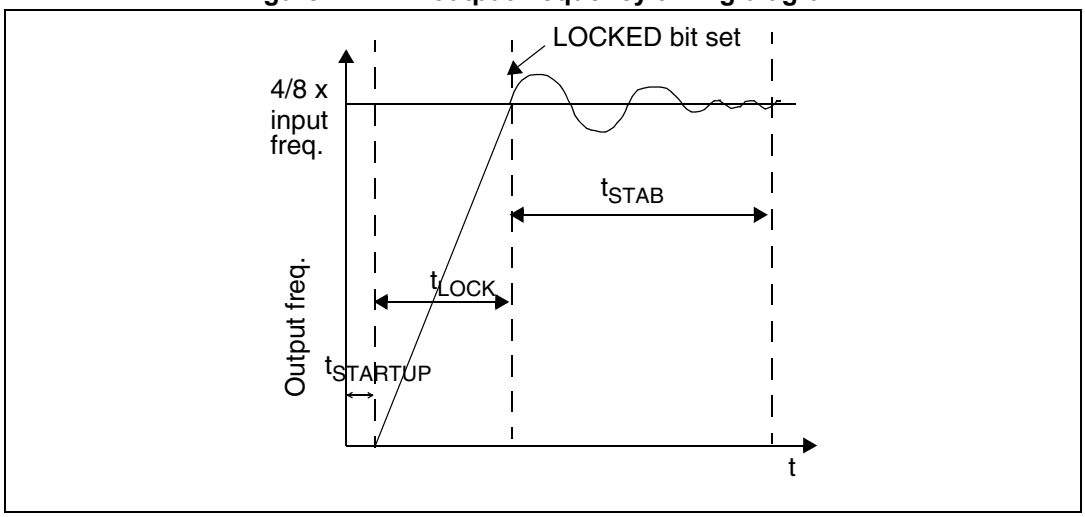
- The x4 PLL is intended for operation with V_{DD} in the 2.4 V to 3.3 V range
- The x8 PLL is intended for operation with V_{DD} in the 3.3 V to 5.5 V range

Note: Refer to Section 15.1: Option bytes for the option byte description.

If the PLL is disabled and the RC oscillator is enabled, then f_{OSC} = 1 MHz.

If both the RC oscillator and the PLL are disabled, f_{OSC} is driven by the external clock.

Figure 12. PLL output frequency timing diagram



When the PLL is started, after reset or wakeup from HALT mode or AWUF mode, it outputs the clock after a delay of $t_{STARTUP}$.

When the PLL output signal reaches the operating frequency, the LOCKED bit in the SICSCR register is set. Full PLL accuracy (ACC_{PLL}) is reached after a stabilization time of t_{STAB} (see *Figure 12* below and *Figure 64: RC oscillator and PLL characteristics (tested*

7.5 Reset sequence manager (RSM)

7.5.1 Introduction

The reset sequence manager includes three RESET sources as shown in *Figure 15: Reset block diagram*:

- External $\overline{\text{RESET}}$ source pulse
- Internal LVD RESET (low voltage detection)
- Internal WATCHDOG RESET

Note: A reset can also be triggered following the detection of an illegal opcode or prebyte code. Refer to Section 12.2.1: Illegal opcode reset for further details.

These sources act on the $\overline{\text{RESET}}$ pin and it is always kept low during the delay phase.

The RESET service routine vector is fixed at addresses FFFEh-FFFFh in the ST7 memory map.

The basic RESET sequence consists of 3 phases as shown in *Figure 14*:

- Active Phase depending on the RESET source
- 256 or 4096 CPU clock cycle delay (see table below)
- RESET vector fetch.

The 256 or 4096 CPU clock cycle delay allows the oscillator to stabilise and ensures that recovery has taken place from the Reset state. The shorter or longer clock cycle delay is automatically selected depending on the clock source chosen by option byte:

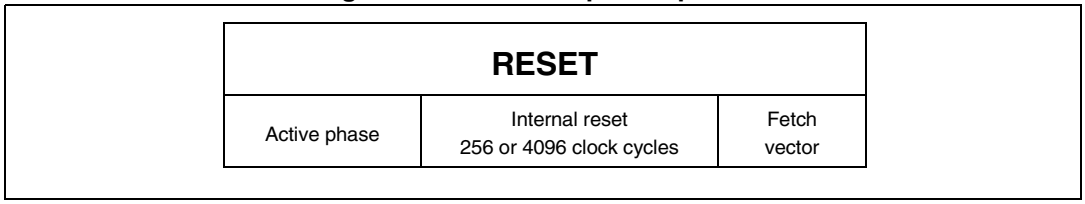
Table 8. CPU clock cycle delay

Clock source	CPU clock cycle delay
Internal RC oscillator	256
External clock (connected to CLKIN pin)	256
External crystal/ceramic oscillator (connected to OSC1/OSC2 pins)	4096

The RESET vector fetch phase duration is 2 clock cycles.

If the PLL is enabled by option byte, it outputs the clock after an additional delay of $t_{STARTUP}$ (see *Figure 12: PLL output frequency timing diagram*).

Figure 14. RESET sequence phases



7.6.4 Register description

System integrity (SI) control/status register (SICSR)

Read/Write

Reset Value: 0000 0xx0 (0xh)

7							0
0	0	0	WDGRF	LOCKED	LVDRF	AVDF	AVDIE

- Bit 7:5 = Reserved, must be kept cleared.
- Bit 4 = **WDGRF** *Watchdog reset flag*
  This bit indicates that the last Reset was generated by the Watchdog peripheral. It is set by hardware (watchdog reset) and cleared by software (writing zero) or an LVD Reset (to ensure a stable cleared state of the WDGRF flag when CPU starts). Combined with the LVDRF flag information, the flag description is given by the following table:

Table 11. Flag description

RESET sources	LVDRF	WDGRF
External $\overline{\text{RESET}}$ pin	0	0
Watchdog	0	1
LVD	1	X

- Bit 3 = **LOCKED** *PLL Locked Flag*
  This bit is set and cleared by hardware. It is set automatically when the PLL reaches its operating frequency.
  0: PLL not locked
  1: PLL locked
- Bit 2 = **LVDRF** *LVD reset flag*
  This bit indicates that the last Reset was generated by the LVD block. It is set by hardware (LVD reset) and cleared by software (by reading). When the LVD is disabled by OPTION BYTE, the LVDRF bit value is undefined.
- Bit 1 = **AVDF** *Voltage Detector flag*
  This read-only bit is set and cleared by hardware. If the AVDIE bit is set, an interrupt request is generated when the AVDF bit is set.
  0: V_{DD} over AVD threshold
  1: V_{DD} under AVD threshold

Note: Refer to *Monitoring the VDD main supply on page 43* and to *Figure 19: Using the AVD to monitor VDD* for additional details.

- Bit 0 = **AVDIE** *Voltage detector interrupt enable*
  This bit is set and cleared by software. It enables an interrupt to be generated when the AVDF flag is set. The pending interrupt information is automatically cleared when software enters the AVD interrupt routine.
  0: AVD interrupt disabled
  1: AVD interrupt enabled

9 Power saving modes

9.1 Introduction

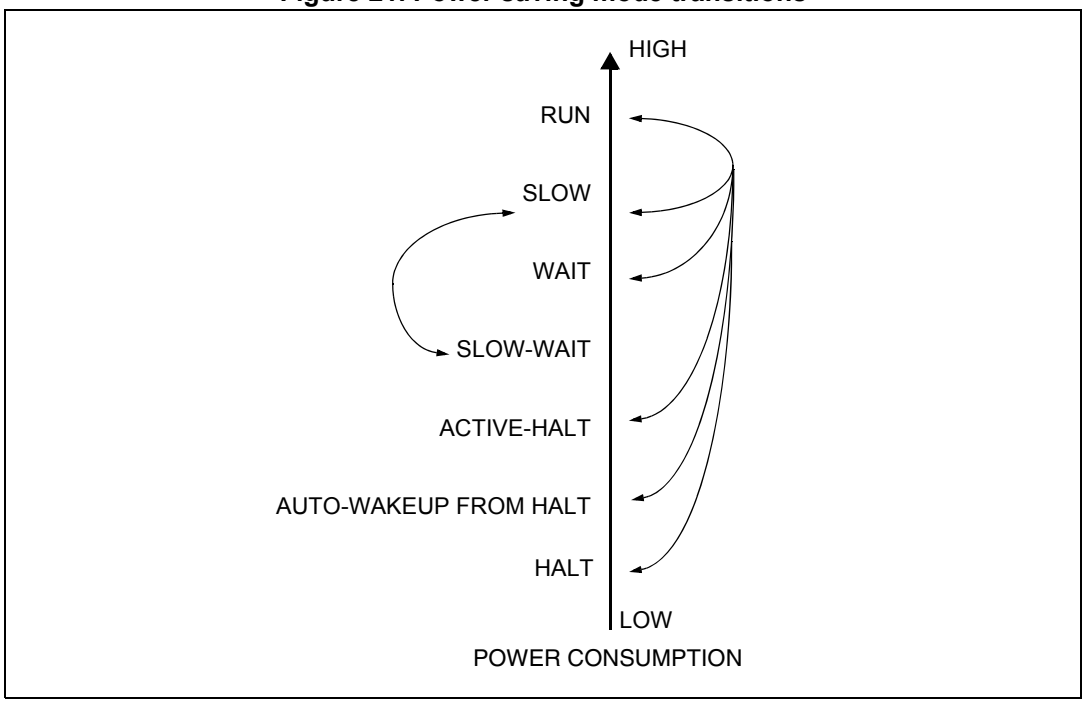
To give a large measure of flexibility to the application in terms of power consumption, five main power saving modes are implemented in the ST7 (see *Figure 21*):

- Slow
- Wait (and Slow-Wait)
- Active Halt
- Auto Wake up From Halt (AWUF)
- Halt

After a RESET the normal operating mode is selected by default (Run mode). This mode drives the device (CPU and embedded peripherals) by means of a master clock which is based on the main oscillator frequency divided or multiplied by 2 (f_{OSC2}).

From RUN mode, the different power saving modes may be selected by setting the relevant register bits or by calling the specific ST7 software instruction whose action depends on the oscillator status.

Figure 21. Power saving mode transitions

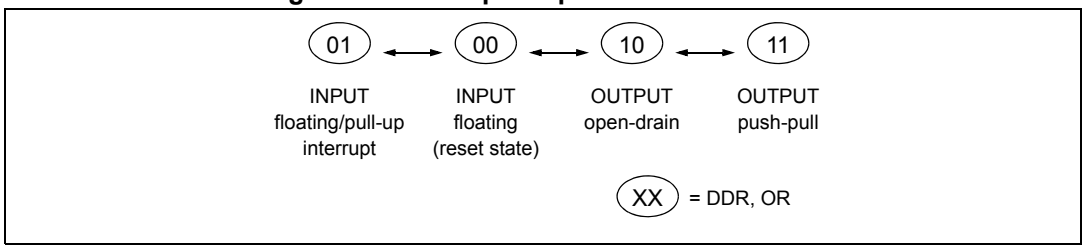


9.2 SLOW mode

This mode has two targets:

- To reduce power consumption by decreasing the internal clock in the device,
- To adapt the internal clock frequency (f_{CPU}) to the available supply voltage.

Figure 32. Interrupt I/O port state transitions



10.4 Unused I/O pins

Unused I/O pins must be connected to fixed voltage levels. Refer to *Section 13.8: I/O port pin characteristics*.

10.5 Low power modes

Table 24. Effect of low power modes on I/O ports

Mode	Description
WAIT	No effect on I/O ports. External interrupts cause the device to exit from WAIT mode.
HALT	No effect on I/O ports. External interrupts cause the device to exit from HALT mode.

10.6 Interrupts

The external interrupt event generates an interrupt if the corresponding configuration is selected with DDR and OR registers and if the I bit in the CC register is cleared (RIM instruction).

Table 25. I/O port interrupt control/wake-up capability

Interrupt event	Event flag	Enable control bit	Exit from WAIT	Exit from HALT
External interrupt on selected external event	-	DDRx ORx	Yes	Yes

10.7 Device-specific I/O port configuration

The I/O port register configurations are summarized as follows:

Standard ports

Table 26. Ports PA7:0, PB6:0

Mode	DDR	OR
Floating input	0	0
Pull-up input	0	1

0: CMPF interrupt disabled.
1: CMPF interrupt enabled.

Counter register high (CNTRH)

Read only

Reset value: 0000 0000 (000h)

15							8
0	0	0	0	CNTR11	CNTR10	CNTR9	CNTR8

Counter register low (CNTRL)

Read only

Reset value: 0000 0000 (000h)

7							0
CNTR7	CNTR6	CNTR5	CNTR4	CNTR3	CNTR2	CNTR1	CNTR0

- Bits 15:12 = Reserved
- Bits 11:0 = **CNTR[11:0]** *Counter value*
  This 12-bit register is read by software and cleared by hardware after a reset. The counter is incremented continuously as soon as a counter clock is selected. To obtain the 12-bit value, software should read the counter value in two consecutive read operations, LSB first. When a counter overflow occurs, the counter restarts from the value specified in the ATR register.

Autoreload register (ATRH)

Read / Write

Reset Value: 0000 0000 (00h)

15							8
0	0	0	0	ATR11	ATR10	ATR9	ATR8

- Bits 15:12 = Reserved
- Bits 11:0 = **ATR[11:0]** *Counter value*
  This 12-bit register is read by software and cleared by hardware after a reset. The counter is incremented continuously as soon as a counter clock is selected. To obtain the 12-bit value, software should read the counter value in two consecutive read operations, LSB first. When a counter overflow occurs, the counter restarts from the value specified in the ATR register.

1: A Counter 2 overflow has occurred.

Lite timer autoreload register (LTARR)

Read / Write

Reset Value: 0000 0000 (00h)

7							0
AR7	AR7	AR7	AR7	AR3	AR2	AR1	AR0

- Bits 7:0 = **AR[7:0]** *Counter 2 Reload Value*
  These bits register is read/write by software. The LTARR value is automatically loaded into Counter 2 (LTCNTR) when an overflow occurs.

Lite timer counter 2 (LTCNTR)

Read only

Reset Value: 0000 0000 (00h)

7							0
CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0

- Bits 7:0 = **CNT[7:0]** *Counter 2 Reload Value*
  This register is read by software. The LTARR value is automatically loaded into Counter 2 (LTCNTR) when an overflow occurs.

Lite timer control/status register (LTCSR1)

Read / Write

Reset Value: 0x00 0000 (x0h)

7							0
ICIE	ICF	TB	TB1IE	TB1F	–	–	–

- Bit 7 = **ICIE** *Interrupt Enable*
  This bit is set and cleared by software.
  0: Input Capture (IC) interrupt disabled
  1: Input Capture (IC) interrupt enabled
- Bit 6 = **ICF** *Input Capture Flag*
  This bit is set by hardware and cleared by software by reading the LTICR register. Writing to this bit does not change the bit value.
  0: No input capture
  1: An input capture has occurred

Note: After an MCU reset, software must initialise the ICF bit by reading the LTICR register

- Bit 5 = **TB** *Timebase period selection*
  This bit is set and cleared by software.

11.5.2 Main features

- 10-bit conversion
- Up to 7 channels with multiplexed input
- Linear successive approximation
- Data register (DR) which contains the results
- Conversion complete status flag
- On/off bit (to reduce consumption)

The block diagram is shown in *Figure 49*.

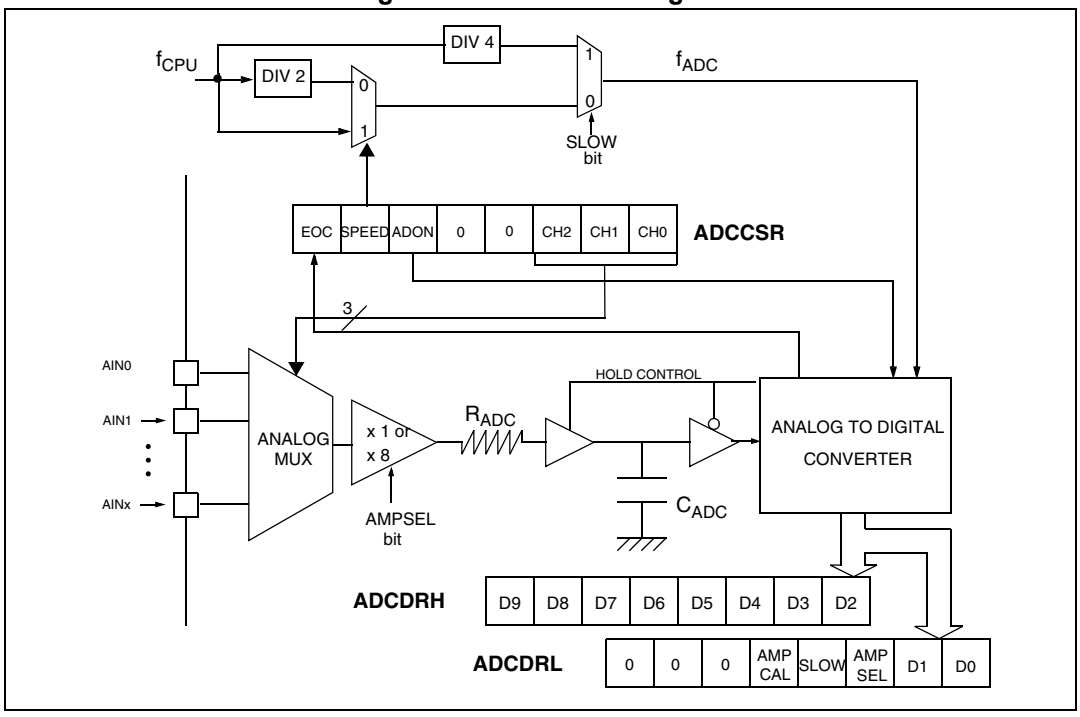
11.5.3 Functional description

Analog power supply

V_{DDA} and V_{SSA} are the high and low level reference voltage pins. In some devices (refer to device pin out description) they are internally connected to the V_{DD} and V_{SS} pins.

Conversion accuracy may therefore be impacted by voltage drops and noise in the event of heavily loaded or badly decoupled power supply lines.

Figure 49. ADC block diagram



Input voltage amplifier

The input voltage can be amplified by a factor of 8 by enabling the AMPSEL bit in the ADCDRL register.

When the amplifier is enabled, the input range is 0 V to $V_{DD}/8$.

Table 47. ADC register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0034h	**ADCCSR** Reset Value	EOC 0	SPEED 0	ADON 0	0 0	0 0	CH2 0	CH1 0	CH0 0
0035h	**ADCDRH** Reset Value	D9 x	D8 x	D7 x	D6 x	D5 x	D4 x	D3 x	D2 x
0036h	**ADCDRL** Reset Value	0 0	0 0	0 0	AMPCAL 0	SLOW 0	AMPSEL 0	D1 x	D0 x

Table 50. Inherent instructions (continued)

Instruction	Function
PUSH/POP	Push/Pop to/from the stack
INC/DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2 Complement
MUL	Byte Multiplication
SLL, SRL, SRA, RLC, RRC	Shift and Rotate operations
SWAP	Swap nibbles

12.1.2 Immediate

Immediate instructions have two bytes: The first byte contains the opcode and the second byte contains the operand value.

Table 51. Immediate instructions

Instruction	Function
LD	Load
CP	Compare
BCP	Bit Compare
AND, OR, XOR	Logical operations
ADC, ADD, SUB, SBC	Arithmetic operations

12.1.3 Direct

In Direct instructions, the operands are referenced by their memory address. The direct addressing mode consists of two submodes:

- Direct (short)
  The address is a byte, thus requiring only one byte after the opcode, but only allows 00 - FF addressing space.
- Direct (long)
  The address is a word, thus allowing 64 Kbyte addressing space, but requires 2 bytes after the opcode.

12.1.4 Indexed (no offset, short, long)

In this mode, the operand is referenced by its memory address, which is defined by the unsigned addition of an index register (X or Y) with an offset.

Table 55. Instruction groups (continued)

Group	Instructions							
Bit operation	BSET	BRES	–	–	–	–	–	–
Conditional Bit Test and Branch	BTJT	BTJF	–	–	–	–	–	–
Arithmetic operations	ADC	ADD	SUB	SBC	MUL	–	–	–
Shift and Rotates	SLL	SRL	SRA	RLC	RRC	SWAP	SLA	–
Unconditional Jump or Call	JRA	JRT	JRF	JP	CALL	CALLR	NOP	RET
Conditional Branch	JRxx	–	–	–	–	–	–	–
Interruption management	TRAP	WFI	HALT	IRET	–	–	–	–
Condition Code Flag modification	SIM	RIM	SCF	RCF	–	–	–	–

Using a prebyte

The instructions are described with 1 to 4 bytes.

In order to extend the number of available opcodes for an 8-bit CPU (256 opcodes), three different prebyte opcodes are defined. These prebytes modify the meaning of the instruction they precede.

The whole instruction becomes:

- PC-2: End of previous instruction
- PC-1: Prebyte
- PC: Opcode
- PC+1: Additional word (0 to 2) according to the number of bytes required to compute the effective address.

These prebytes enable instruction in Y as well as indirect addressing modes to be implemented.

They precede the opcode of the instruction in X or the instruction using direct addressing mode. The prebytes are:

- PDY 90: Replace an X based instruction using immediate, direct, indexed, or inherent addressing mode by a Y one.
- PIX 92: Replace an instruction using direct, direct bit or direct relative addressing mode to an instruction using the corresponding indirect addressing mode.
  It also changes an instruction using X indexed addressing mode to an instruction using indirect X indexed addressing mode.
- PIY 91: Replace an instruction using X indirect indexed addressing mode by a Y one.

12.2.1 Illegal opcode reset

In order to provide enhanced robustness to the device against unexpected behavior, a system of illegal opcode detection is implemented. If a code to be executed does not correspond to any opcode or prebyte value, a reset is generated. This, combined with the Watchdog, allows the detection and recovery from an unexpected fault or interference.

Note: A valid prebyte associated with a valid opcode forming an unauthorized combination does not generate a reset.

Table 56. Instruction set overview

Mnemo	Description	Function/example	Dst	Src	H	I	N	Z	C
ADC	Add with Carry	A = A + M + C	A	M	H	–	N	Z	C
ADD	Addition	A = A + M	A	M	H	–	N	Z	C
AND	Logical And	A = A . M	A	M	–	–	N	Z	–
BCP	Bit compare A, memory	tst (A . M)	A	M	–	–	N	Z	–
BRES	Bit reset	bres Byte, #3	M	–	–	–	–	–	–
BSET	Bit set	bset Byte, #3	M	–	–	–	–	–	–
BTJF	Jump if bit is false (0)	btjf Byte, #3, Jmp1	M	–	–	–	–	–	C
BTJT	Jump if bit is true (1)	btjt Byte, #3, Jmp1	M	–	–	–	–	–	C
CALL	Call sub-routine	–	–	–	–	–	–	–	–
CALLR	Call sub-routine relative	–	–	–	–	–	–	–	–
CLR	Clear	–	reg, M	–	–	–	0	1	–
CP	Arithmetic Compare	–	reg	M	–	–	N	Z	C
CPL	One Complement	A = FFH-A	reg, M	–	–	–	N	Z	1
DEC	Decrement	dec Y	reg, M	–	–	–	N	Z	–
HALT	HALT	–	–	–	–	0	–	–	–
IRET	Interrupt routine return	Pop CC, A, X, PC	–	–	H	I	N	Z	C
INC	Increment	inc X	reg, M	–	–	–	N	Z	–
JP	Absolute Jump	jp [TBL.w]	–	–	–	–	–	–	–
JRA	Jump relative always	–	–	–	–	–	–	–	–
JRT	Jump relative	–	–	–	–	–	–	–	–
JRF	Never jump	jrf *	–	–	–	–	–	–	–
JRIH	Jump if ext. interrupt = 1	–	–	–	–	–	–	–	–
JRIL	Jump if ext. interrupt = 0	–	–	–	–	–	–	–	–
JRH	Jump if H = 1	H = 1 ?	–	–	–	–	–	–	–
JRNH	Jump if H = 0	H = 0 ?	–	–	–	–	–	–	–
JRM	Jump if I1:0 = 11	I = 1 ?	–	–	–	–	–	–	–
JRNM	Jump if I1:0 <> 11	I = 0 ?	–	–	–	–	–	–	–
JRMI	Jump if N = 1 (minus)	N = 1 ?	–	–	–	–	–	–	–
JRPL	Jump if N = 0 (plus)	N = 0 ?	–	–	–	–	–	–	–
JREQ	Jump if Z = 1 (equal)	Z = 1 ?	–	–	–	–	–	–	–
JRNE	Jump if Z = 0 (not equal)	Z = 0 ?	–	–	–	–	–	–	–
JRC	Jump if C = 1	C = 1 ?	–	–	–	–	–	–	–
JRNC	Jump if C = 0	C = 0 ?	–	–	–	–	–	–	–
JRULT	Jump if C = 1	Unsigned <	–	–	–	–	–	–	–
JRUGE	Jump if C = 0	Jmp if unsigned ≥	–	–	–	–	–	–	–

1. Not tested in production.
2. Not tested in production. The V_{DD} rise time rate condition is needed to insure a correct device power-on and LVD reset. When the V_{DD} slope is outside these values, the LVD may not ensure a proper reset of the MCU.
   Use of LVD with capacitive power supply: with this type of power supply, if power cuts occur in the application, it is recommended to pull V_{DD} down to 0 V to ensure optimum restart conditions. Refer to circuit example in *Figure 84: RESET pin protection when LVD is enabled*

Table 70. Resonator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CrOSC}	Crystal Oscillator Frequency(1)	–	2	–	16	MHz
C_{L1} C_{L2}	Recommended load capacitance versus equivalent serial resistance of the crystal or ceramic resonator (R_S)	–	See *Table 72: Resonator performances*			pF

1. When PLL is used, please refer to the *Section 13.3.4: Internal RC oscillator and PLL* and *Section 7: Supply, reset and clock management* (f_{CrOSC} min. is 8 Mhz with PLL).

Table 71: Resonator performances

Supplier	f_{CrOSC} [MHz]	Typical ceramic resonators(1)		CL1(2) [pF]	CL2(2) [pF]	Rd [Ω]	Supply voltage range [V]	Temperature range [°C]
		Type (3)	Reference					
Murata	2	SMD	CSTCC2M00G56-R0	(47)	(47)	0	2.4V to 5.5V	-40 to 85
	4	SMD	CSTCR4M00G53-R0	(15)	(15)	0		
		LEAD	CSTLS4M00G53-B0	(15)	(15)	0		
	8	SMD	CSTCE8M00G52-R0	(10)	(10)	0		
		LEAD	CSTLS8M00G53-B0	(15)	(15)	0		
	16	SMD	CSTCE16M0V51-R0	(5)	(5)	0	3.3V to 5.5V	
		LEAD	CSTLS16M0X53-B0	(15)	(15)	0	4.5V to 5.5V	
		LEAD	CSALS16M0X55-B0	7	7	1.5k	3.8V to 5.5V	

1. Resonator characteristics given by the ceramic resonator manufacturer. For more information on these resonators, please consult www.murata.com
2. () means load capacitor built in resonator.
3. SMD = -R0: Plastic tape package (∅=180mm).
   LEAD = -B0: Bulk

Table 77. Emission test

Symbol	Parameter	Conditions	Monitored Frequency Band	Max vs. [f_{OSC}/f_{CPU}]		Unit
				8/4MHz	16/8MHz	–
S_{EMI}	Peak level	V_{DD}=5V, T_A=+25°C, SO20 package, conforming to SAE J 1752/3	0.1 MHz to 30 MHz	9	17	dBµV
			30 MHz to 130 MHz	31	36	
			130 MHz to 1 GHz	25	27	
			SAE EMI Level	3.5	4	–

Note: Data based on characterization results, not tested in production.

13.7.3 Absolute maximum ratings (Electrical sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

Note: For more details, refer to the application note AN1181.

Electro-Static Discharge (ESD)

Electro-Static Discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard.

Table 78. Absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human body model)	T_A=+25°C	4000	V

1. Data based on characterization results, not tested in production.

Static and dynamic latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard.
- **DLU**: Electro-Static Discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards.

Note: For more details, refer to the application note AN1181.

Table 90. Thermal characteristics

Symbol	Ratings		Value	Unit
R_{thJA}	Package thermal resistance (junction to ambient)	SO20 DIP20	125 63	°C/W
T_{Jmax}	Maximum junction temperature(1)		150	°C
P_{Dmax}	Power dissipation(2)		500	mW

1. The maximum chip-junction temperature is based on technology characteristics.
2. The maximum power dissipation is obtained from the formula $P_D = (T_J - T_A) / R_{thJA}$.
The power dissipation of an application can be defined by the user with the formula: $P_D=P_{INT}+P_{PORT}$ where P_{INT} is the chip internal power ($I_{DD}xV_{DD}$) and P_{PORT} is the port power dissipation depending on the ports used in the application.

14.2 Soldering information

In accordance with the RoHS European directive, all STMicroelectronics packages have been converted to lead-free technology, named ECOPACK™.

- ECOPACK™ packages are qualified according to the JEDEC STD-020C compliant soldering profile.
- Detailed information on the STMicroelectronics ECOPACK™ transition program is available on www.st.com/stonline/leadfree/, with specific technical Application notes covering the main technical aspects related to lead-free conversion (AN2033, AN2034, AN2035, AN2036).

Backward and forward compatibility

The main difference between Pb and Pb-free soldering process is the temperature range.

- ECOPACK™ TQFP, SDIP and SO packages are fully compatible with Lead (Pb) containing soldering process (see application note AN2034)
- TQFP, SDIP and SO Pb-packages are compatible with Lead-free soldering process, nevertheless it's the customer's duty to verify that the Pb packages maximum temperature (mentioned on the Inner box label) is compatible with their Leadfree soldering temperature.

Table 91. Soldering compatibility (wave and reflow soldering process)

Package	Plating material devices	Pb solder paste	Pb-free solder paste
SDIP & PDIP	Sn (pure Tin)	Yes	Yes(1)
TQFP and SO	NiPdAu (Nickel-palladium-Gold)	Yes	Yes(1)

1. Assemblers must verify that the Pb-package maximum temperature (mentioned on the Inner box label) is compatible with their Lead-free soldering process.

Table 100. ST7 application notes (continued)

Identification	Description
AN1151	Performance Comparison Between ST72254 & PC16F876
AN1278	LIN (Local Interconnect Network) Solutions
Product Migration	
AN1131	Migrating applications from ST72511/311/214/124 to ST72521/321/324
AN1322	Migrating an application from ST7263 Rev.B to ST7263B
AN1365	Guidelines for migrating ST72C254 applications to ST72F264
AN1604	How to use ST7MDT1-TRAIN with ST72F264
AN2200	guidelines for migrating st7lite1x applications to st7flite1xb
Product Optimization	
AN 982	Using ST7 with Ceramic Resonator
AN1014	How to Minimize the ST7 Power Consumption
AN1015	SOFTWARE TECHNIQUES FOR IMPROVING MICROCONTROLLER EMC PERFORMANCE
AN1040	Monitoring the Vbus Signal for USB Self-Powered Devices
AN1070	ST7 Checksum Self-Checking Capability
AN1181	Electrostatic Discharge Sensitive Measurement
AN1324	Calibrating the RC Oscillator of the ST7FLITE0 MCU using the MAINS
AN1502	Emulated Data EEPROM with ST7 HDFlash Memory
AN1529	Extending the current & voltage capability on the ST7265 VDDF Supply
AN1530	Accurate timebase for low-cost ST7 applications with internal RC oscillator
AN1605	Using an active RC to wakeup the ST7LITE0 from power saving mode
AN1636	UNDERSTANDING AND MINIMIZING ADC CONVERSION ERRORS
AN1828	PIR (Passive Infrared) Detector using the ST7FLITE05/09/SUPERLITE
AN1946	SENSORLESS BLDC MOTOR CONTROL AND BEMF SAMPLING METHODS WITH ST7MC
AN1953	PFC FOR ST7MC STARTER KIT
AN1971	ST7LITE0 MICROCONTROLLED BALLAST
Programming and Tools	
AN 978	ST7 Visual DeVELOP Software Key Debugging Features
AN 983	Key Features of the Cosmic ST7 C-Compiler Package
AN 985	Executing Code In ST7 RAM
AN 986	Using the Indirect Addressing Mode with ST7
AN 987	ST7 Serial Test Controller Programming
AN 988	Starting with ST7 Assembly Tool Chain
AN 989	Getting Started with the ST7 Hiware C Toolchain

16 Important notes

16.1 Execution of BTJX instruction

When testing the address $FF with the "BTJT" or "BTJF" instructions, the CPU may perform an incorrect operation when the relative jump is negative and performs an address page change.

To avoid this issue, including when using a C compiler, it is recommended to never use address $00FF as a variable (using the linker parameter for example).

16.2 ADC conversion spurious results

Spurious conversions occur with a rate lower than 50 per million. Such conversions happen when the measured voltage is just between 2 consecutive digital values.

Workaround

A software filter should be implemented to remove erratic conversion results whenever they may cause unwanted consequences.

16.3 A/D converter accuracy for first conversion

When the ADC is enabled after being powered down (for example when waking up from HALT, ACTIVE-HALT or setting the ADON bit in the ADCCSR register), the first conversion (8-bit or 10-bit) accuracy does not meet the accuracy specified in the datasheet.

Workaround

In order to have the accuracy specified in the datasheet, the first conversion after a ADC switch-on has to be ignored.

16.4 Negative injection impact on ADC accuracy

Injecting a negative current on an analog input pins significantly reduces the accuracy of the AD Converter. Whenever necessary, the negative injection should be prevented by the addition of a Schottky diode between the concerned I/Os and ground.

Injecting a negative current on digital input pins degrades ADC accuracy especially if performed on a pin close to ADC channel in use.

16.5 Clearing active interrupts outside interrupt routine

When an active interrupt request occurs at the same time as the related flag or interrupt mask is being cleared, the CC register may be corrupted.