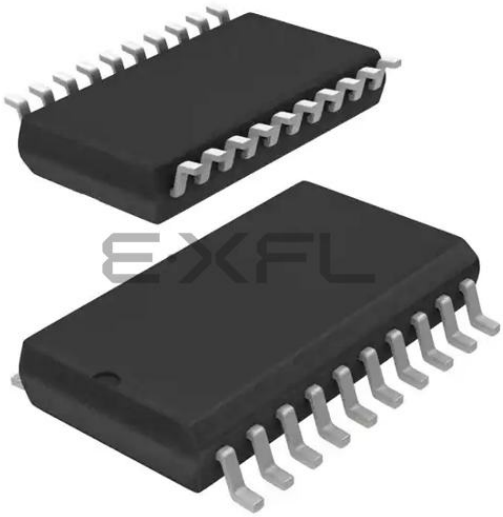

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	15
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SO
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7flite25m6tr

Port and control configuration:

- Input:
  - float = floating, wpu = weak pull-up, int = interrupt, ana = analog
- Output:
  - OD = open drain
  - PP = push-pull

The RESET configuration of each pin is shown in bold which is valid as long as the device is in reset state.

Table 2. Device pin description

Pin No.		Pin name	Type	Level		Port / Control						Main function (after reset)	Alternate function
						Input				Output			
SO20	DIP20			Input	Output	float	wpu	int	ana	OD	PP		
1	16	V_{SS}	S	-	-	-	-	-	-	-	-	Ground	
2	17	V_{DD}	S	-	-	-	-	-	-	-	-	Main power supply	
3	18	$\overline{RESET}$	I/O	C_T	-	-	X	-	-	X	-	Top priority non maskable interrupt (active low)	
4	19	PB0/AIN0/$\overline{SS}$	I/O	C_T		**X**	ei3		X	X	X	**Port B0**	ADC analog input 0 or SPI Slave Select (active low)(1)
5	20	PB1/AIN1/SCK	I/O	C_T		**X**			X	X	X	**Port B1**	ADC analog input 1 or SPI Serial Clock(1)
6	1	PB2/AIN2/MISO	I/O	C_T		**X**			X	X	X	**Port B2**	ADC analog input 2 or SPI Master in/ Slave out data
7	2	PB3/AIN3/MOSI	I/O	C_T		**X**	ei2		X	X	X	**Port B3**	ADC analog input 3 or SPI Master out / Slave in data
8	3	PB4/AIN4/CLKIN	I/O	C_T		**X**			X	X	X	**Port B4**	ADC analog input 4 or external clock input
9	4	PB5/AIN5	I/O	C_T		**X**			X	X	X	**Port B5**	ADC analog input 5
10	5	PB6/AIN6	I/O	C_T		**X**			X	X	X	**Port B6**	ADC analog input 6
11	6	PA7	I/O	C_T	HS	**X**	ei1		-	X	X	**Port A7**	-
12	7	PA6 /MCO/ ICCCLK/BREAK	I/O	C_T		X	ei1		-	X	X	**Port A6**	Main clock output or in circuit communication clock or external BREAK(2)
13	8	PA5 /ATPWM3/ ICCDATA	I/O	C_T	HS	**X**	ei1		-	X	X	**Port A5**	Auto-reload timer PWM3 or In circuit communication data
14	9	PA4/ATPWM2	I/O	C_T	HS	**X**			-	X	X	**Port A4**	Auto-reload timer PWM2

3 Register & memory map

As shown in *Figure 4*, the MCU is able of addressing 64K bytes of memories and I/O registers.

The available memory locations consist of 128 bytes of register locations, 384 bytes of RAM, 256 bytes of data EEPROM and 8 Kbytes of user program memory. The RAM space includes up to 128 bytes for the stack from 180h to 1FFh.

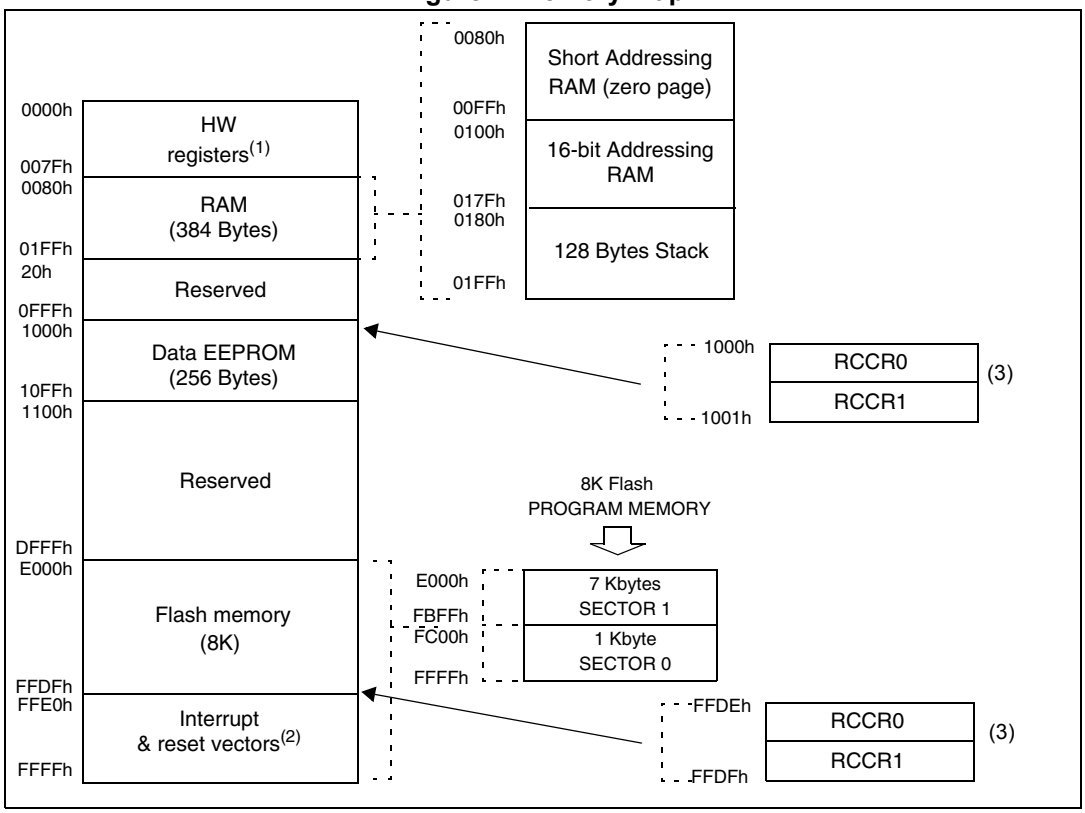
The highest address bytes contain the user reset and interrupt vectors.

The Flash memory contains two sectors (see *Figure 4*) mapped in the upper part of the ST7 addressing space so the reset and interrupt vectors are located in Sector 0 (F000h-FFFFh).

The size of Flash Sector 0 and other device options are configurable by Option byte (refer to *Section 15: Device configuration*).

Note: Memory locations marked as "Reserved" must never be accessed. Accessing a reserved area can have unpredictable effects on the device.

Figure 4. Memory map



1. See *Table 3: Hardware register map*
2. See *Table 12: Interrupt mapping*
3. See *Section 7.1: Internal RC oscillator adjustment*

Note: When the Multi-oscillator is not used, PB4 is selected by default as external clock.

Crystal/ceramic oscillators

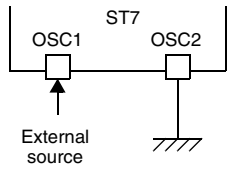
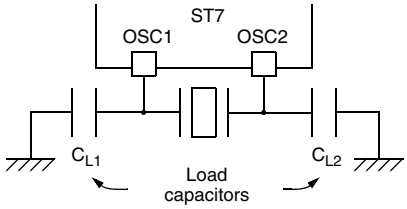
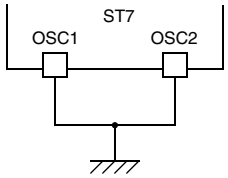
This family of oscillators has the advantage of producing a very accurate rate on the main clock of the ST7. The selection within a list of 4 oscillators with different frequency ranges has to be done by option byte in order to reduce consumption (refer to *Section 15.1: Option bytes* for more details on the frequency ranges). In this mode of the multi-oscillator, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The loading capacitance values must be adjusted according to the selected oscillator.

These oscillators are not stopped during the RESET phase to avoid losing time in the oscillator startup phase.

Internal RC oscillator

In this mode, the tunable 1% RC oscillator is used as main clock source. The two oscillator pins have to be tied to ground.

Table 7. ST7 clock sources

Clock source	Hardware configuration
External clock	
Crystal/ceramic resonators	
Internal RC oscillator or external clock on PB4	

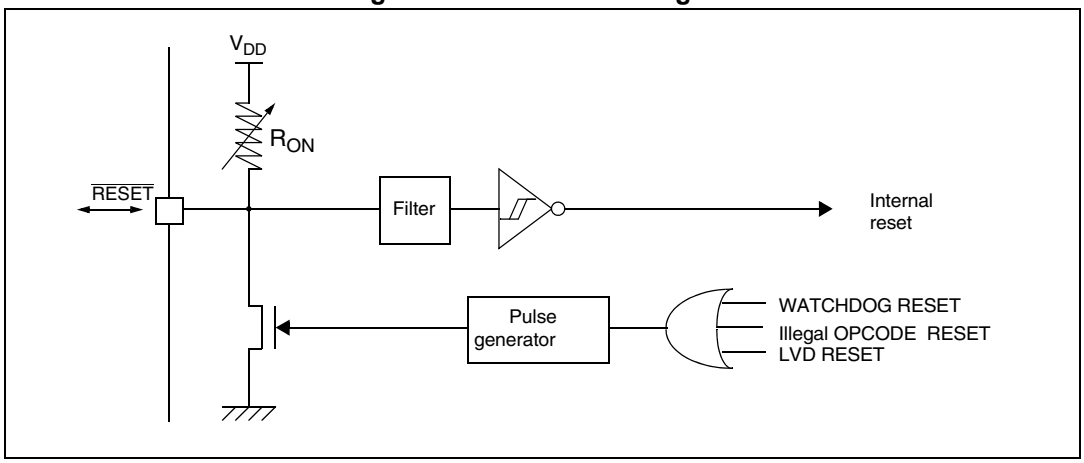
7.5.2 Asynchronous external $\overline{\text{RESET}}$ pin

The $\overline{\text{RESET}}$ pin is both an input and an open-drain output with integrated R_{ON} weak pull-up resistor. This pull-up has no fixed value but varies in accordance with the input voltage. It can be pulled low by external circuitry to reset the device.

Note: See Section 13: Electrical characteristics for more details.

A RESET signal originating from an external source must have a duration of at least $t_{h(RSTL)in}$ in order to be recognized (see *Figure 16: RESET sequences*). This detection is asynchronous and therefore the MCU can enter reset state even in HALT mode.

Figure 15. Reset block diagram



Note: See Section 12.2.1: Illegal opcode reset for more details on illegal opcode reset conditions.

The $\overline{\text{RESET}}$ pin is an asynchronous signal which plays a major role in EMS performance. In a noisy environment, it is recommended to follow the guidelines mentioned in *Section 13: Electrical characteristics*.

7.5.3 External power-on RESET

If the LVD is disabled by option byte, to start up the microcontroller correctly, the user must ensure by means of an external reset circuit that the reset signal is held low until V_{DD} is over the minimum level specified for the selected f_{OSC} frequency.

A proper reset signal for a slow rising V_{DD} supply can generally be provided by an external RC network connected to the $\overline{\text{RESET}}$ pin.

7.5.4 Internal low voltage detector (LVD) RESET

Two different RESET sequences caused by the internal LVD circuitry can be distinguished:

- Power-on RESET
- Voltage drop RESET.

The device $\overline{\text{RESET}}$ pin acts as an output that is pulled low when $V_{DD}<V_{IT+}$ (rising edge) or $V_{DD}<V_{IT-}$ (falling edge) as shown in *Figure 16: RESET sequences*.

The LVD filters spikes on V_{DD} larger than $t_{g(VDD)}$ to avoid parasitic resets.

Table 16. External interrupt I/O pin ei1[1:0] selection

ei11	ei10	I/O pin
0	0	PA4
0	1	PA5
1	0	PA6
1	1	PA7(1)

1. Reset state

- Bits 1:0 = **ei0[1:0]** *ei0 pin selection*
  These bits are written by software. They select the Port A I/O pin used for the ei0 external interrupt according to the table below.

Table 17. External interrupt I/O pin ei0[1:0] selection

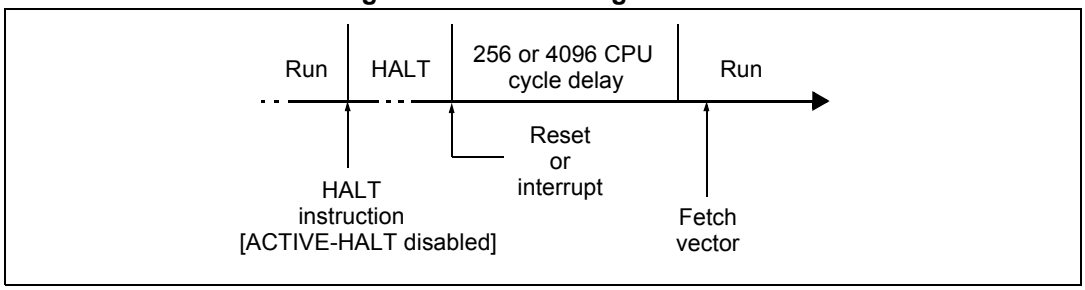
ei01	ei00	I/O pin
0	0	PA0 (1)
0	1	PA1
1	0	PA2
1	1	PA3

1. Reset state

ones which get their clock supply from another clock generator (such as an external or auxiliary oscillator).

The compatibility of Watchdog operation with HALT mode is configured by the “WDGHALT” option bit of the option byte. The HALT instruction when executed while the Watchdog system is enabled, can generate a Watchdog RESET (see *Section 15.1: Option bytes* for more details).

Figure 24. HALT timing overview



Spurious interrupts

When enabling/disabling an external interrupt by setting/resetting the related OR register bit, a spurious interrupt is generated if the pin level is low and its edge sensitivity includes falling/rising edge. This is due to the edge detector input which is switched to '1' when the external interrupt is disabled by the OR register.

To avoid this unwanted interrupt, a "safe" edge sensitivity (rising edge for enabling and falling edge for disabling) has to be selected before changing the OR register bit and configuring the appropriate sensitivity again.

Caution: In case a pin level change occurs during these operations (asynchronous signal input), as interrupts are generated according to the current sensitivity, it is advised to disable all interrupts before and to reenable them after the complete previous sequence in order to avoid an external interrupt occurring on the unwanted edge.

This corresponds to the following steps:

1. To enable an external interrupt:
   - set the interrupt mask with the SIM instruction (in cases where a pin level change could occur)
   - select rising edge
   - enable the external interrupt through the OR register
   - select the desired sensitivity if different from rising edge
   - reset the interrupt mask with the RIM instruction (in cases where a pin level change could occur).
2. To disable an external interrupt:
   - set the interrupt mask with the SIM instruction SIM (in cases where a pin level change could occur)
   - select falling edge
   - disable the external interrupt through the OR register
   - select rising edge
   - reset the interrupt mask with the RIM instruction (in cases where a pin level change could occur).

10.2.2 Output modes

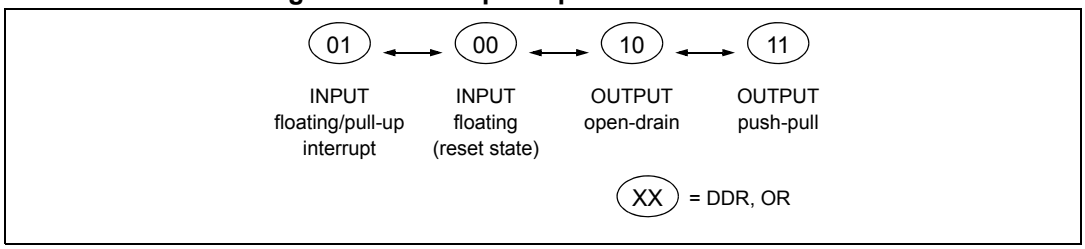
Setting the DDRx bit selects output mode. Writing to the DR bits applies a digital value to the I/O through the latch. Reading the DR bits returns the previously stored value.

If an OR bit is available, different output modes can be selected by software: push-pull or opendrain. Refer to I/O Port Implementation section for configuration.

Table 21. DR value and output pin status

DR	Push-pull	Open-drain
0	V_{OL}	V_{OL}
1	V_{OH}	Floating

Figure 32. Interrupt I/O port state transitions



10.4 Unused I/O pins

Unused I/O pins must be connected to fixed voltage levels. Refer to *Section 13.8: I/O port pin characteristics*.

10.5 Low power modes

Table 24. Effect of low power modes on I/O ports

Mode	Description
WAIT	No effect on I/O ports. External interrupts cause the device to exit from WAIT mode.
HALT	No effect on I/O ports. External interrupts cause the device to exit from HALT mode.

10.6 Interrupts

The external interrupt event generates an interrupt if the corresponding configuration is selected with DDR and OR registers and if the I bit in the CC register is cleared (RIM instruction).

Table 25. I/O port interrupt control/wake-up capability

Interrupt event	Event flag	Enable control bit	Exit from WAIT	Exit from HALT
External interrupt on selected external event	-	DDRx ORx	Yes	Yes

10.7 Device-specific I/O port configuration

The I/O port register configurations are summarized as follows:

Standard ports

Table 26. Ports PA7:0, PB6:0

Mode	DDR	OR
Floating input	0	0
Pull-up input	0	1

The application program must write in the CR register at regular intervals during normal operation to prevent an MCU reset. This downcounter is freerunning: it counts down even if the watchdog is disabled. The value to be stored in the CR register must be between FFh and C0h (see *Table 31: Watchdog timing*):

- The WDGA bit is set (watchdog enabled)
- The T6 bit is set to prevent generating an immediate reset
- The T[5:0] bits contain the number of increments which represents the time delay before the watchdog produces a reset.

Following a reset, the watchdog is disabled. Once activated it cannot be disabled, except by a reset.

The T6 bit can be used to generate a software reset (the WDGA bit is set and the T6 bit is cleared).

If the watchdog is activated, the HALT instruction will generate a Reset.

Table 31. Watchdog timing(1)

f_{CPU} = 8 MHz		
WDG counter code	**min [ms]**	**max [ms]**
C0h	1	2
FFh	127	128

1. The timing variation is due to the unknown status of the prescaler when writing to the CR register.

Note: The number of CPU clock cycles applied during the reset phase (256 or 4096) must be taken into account in addition to these timings.

11.1.4 Hardware watchdog option

If Hardware Watchdog is selected by option byte, the watchdog is always active and the WDGA bit in the CR is not used.

Refer to the Option Byte description in *Section 15: Device configuration*.

Using HALT mode or ACTIVE-HALT mode with the WDG (WDGHALT option)

If Halt mode with Watchdog is enabled by option byte (No watchdog reset on HALT instruction), it is recommended before executing the HALT instruction to refresh the WDG counter, to avoid an unexpected WDG reset immediately after waking up the microcontroller. Same behavior in active-halt mode.

11.1.5 Interrupts

None.

0: CMPF interrupt disabled.
1: CMPF interrupt enabled.

Counter register high (CNTRH)

Read only

Reset value: 0000 0000 (000h)

15							8
0	0	0	0	CNTR11	CNTR10	CNTR9	CNTR8

Counter register low (CNTRL)

Read only

Reset value: 0000 0000 (000h)

7							0
CNTR7	CNTR6	CNTR5	CNTR4	CNTR3	CNTR2	CNTR1	CNTR0

- Bits 15:12 = Reserved
- Bits 11:0 = **CNTR[11:0]** *Counter value*
  This 12-bit register is read by software and cleared by hardware after a reset. The counter is incremented continuously as soon as a counter clock is selected. To obtain the 12-bit value, software should read the counter value in two consecutive read operations, LSB first. When a counter overflow occurs, the counter restarts from the value specified in the ATR register.

Autoreload register (ATRH)

Read / Write

Reset Value: 0000 0000 (00h)

15							8
0	0	0	0	ATR11	ATR10	ATR9	ATR8

- Bits 15:12 = Reserved
- Bits 11:0 = **ATR[11:0]** *Counter value*
  This 12-bit register is read by software and cleared by hardware after a reset. The counter is incremented continuously as soon as a counter clock is selected. To obtain the 12-bit value, software should read the counter value in two consecutive read operations, LSB first. When a counter overflow occurs, the counter restarts from the value specified in the ATR register.

11.3 Lite timer 2 (LT2)

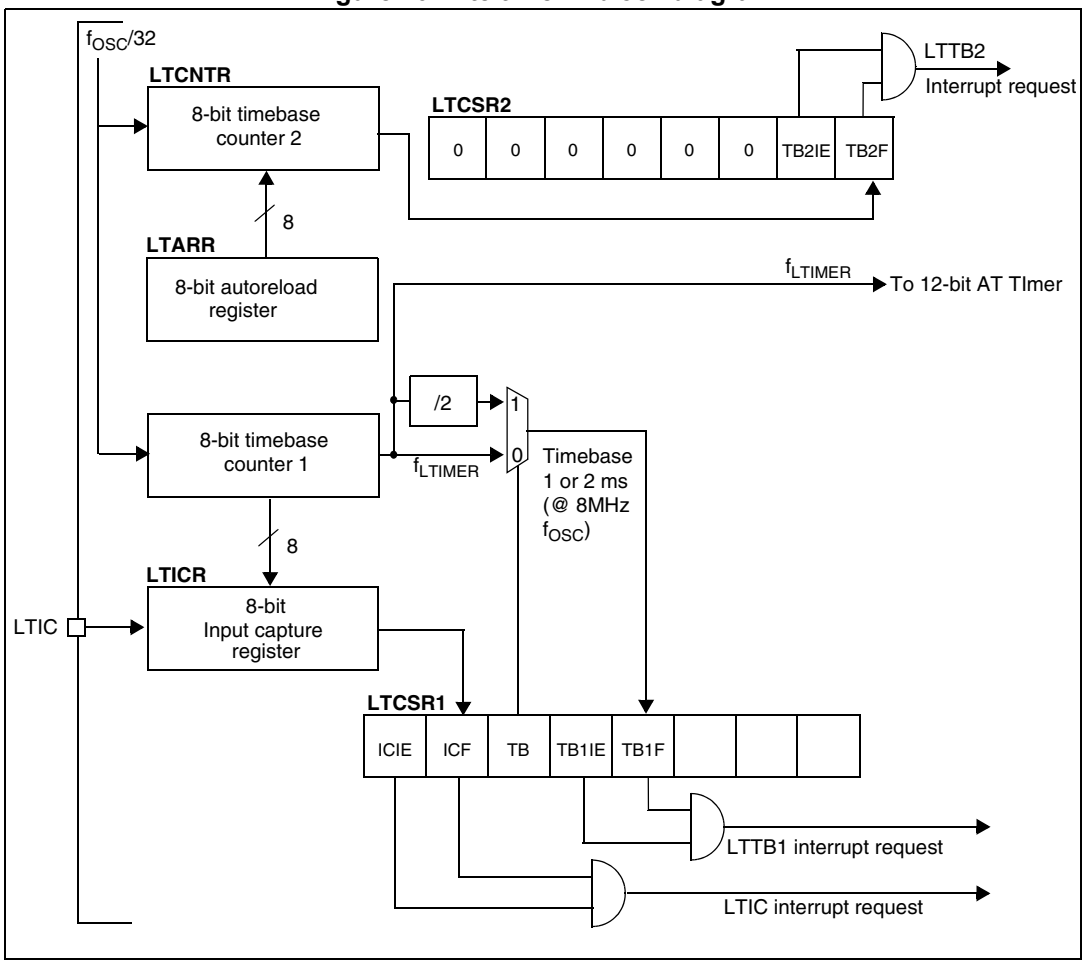
11.3.1 Introduction

The Lite timer can be used for general-purpose timing functions. It is based on two free-running 8-bit upcounters, an 8-bit input capture register.

11.3.2 Main features

- Real-time clock
  - One 8-bit upcounter 1 ms or 2 ms timebase period (@ 8 MHz f_{OSC})
  - One 8-bit upcounter with autoreload and programmable timebase period from 4µs to 1.024 ms in 4 µs increments (@ 8 MHz f_{OSC})
  - 2 Maskable timebase interrupts.
- Input capture
  - 8-bit input capture register (LTICR)
  - Maskable interrupt with wakeup from HALT mode capability.

Figure 40. Lite timer 2 block diagram



1: A Counter 2 overflow has occurred.

Lite timer autoreload register (LTARR)

Read / Write

Reset Value: 0000 0000 (00h)

7							0
AR7	AR7	AR7	AR7	AR3	AR2	AR1	AR0

- Bits 7:0 = **AR[7:0]** *Counter 2 Reload Value*
  These bits register is read/write by software. The LTARR value is automatically loaded into Counter 2 (LTCNTR) when an overflow occurs.

Lite timer counter 2 (LTCNTR)

Read only

Reset Value: 0000 0000 (00h)

7							0
CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0

- Bits 7:0 = **CNT[7:0]** *Counter 2 Reload Value*
  This register is read by software. The LTARR value is automatically loaded into Counter 2 (LTCNTR) when an overflow occurs.

Lite timer control/status register (LTCSR1)

Read / Write

Reset Value: 0x00 0000 (x0h)

7							0
ICIE	ICF	TB	TB1IE	TB1F	–	–	–

- Bit 7 = **ICIE** *Interrupt Enable*
  This bit is set and cleared by software.
  0: Input Capture (IC) interrupt disabled
  1: Input Capture (IC) interrupt enabled
- Bit 6 = **ICF** *Input Capture Flag*
  This bit is set by hardware and cleared by software by reading the LTICR register. Writing to this bit does not change the bit value.
  0: No input capture
  1: An input capture has occurred

Note: After an MCU reset, software must initialise the ICF bit by reading the LTICR register

- Bit 5 = **TB** *Timebase period selection*
  This bit is set and cleared by software.

1. All power (V_{DD}) and ground (V_{SS}) lines must always be connected to the external supply.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected.
3. Negative injection disturbs the analog performance of the device. In particular, it induces leakage currents throughout the device including the analog inputs. To avoid undesirable effects on the analog functions, care must be taken:
   - Analog input pins must have a negative injection less than 0.8 mA (assuming that the impedance of the analog voltage is lower than the specified limits)
   - Pure digital pins must have a negative injection less than 1.6mA. In addition, it is recommended to inject the current as far as possible from the analog input pins.
4. No negative current injection allowed on PB0 and PB1 pins.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 59. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature(1)	–	–

1. (see *Table 90: Thermal characteristics*)

13.3 Operating conditions

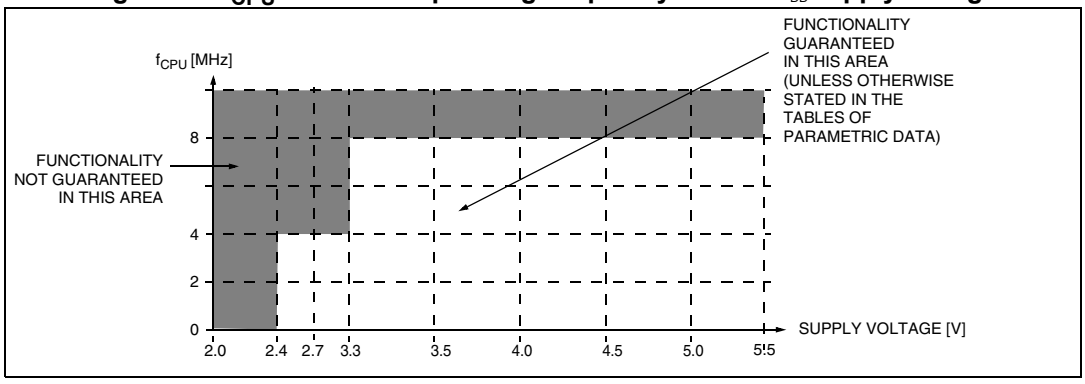
13.3.1 General operating conditions

T_A = -40 to +85 °C unless otherwise specified.

Table 60. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage	f_{CPU} = 4 MHz. max.	2.4	5.5	V
		f_{CPU} = 8 MHz. max.	3.3	5.5	
f_{CPU}	CPU clock frequency	3.3 V≤V_{DD}≤5.5 V	up to 8		MHz
		2.4 V≤V_{DD}<3.3 V	up to 4		

Figure 52. f_{CPU} maximum operating frequency versus V_{DD} supply voltage



13.3.2 Operating conditions with low voltage detector (LVD)

T_A = -40 to 85°C, unless otherwise specified

Table 61. Power on/power down operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IT+(LVD)}$	Reset release threshold (V_{DD} rise)	High Threshold Med. Threshold Low Threshold	4.00(1) 3.40(1) 2.65(1)	4.25 3.60 2.90	4.50 3.80 3.15	V
$V_{IT-(LVD)}$	Reset generation threshold (V_{DD} fall)	High Threshold Med. Threshold Low Threshold	3.80 3.20 2.40	4.05 3.40 2.70	4.30(1) 3.65(1) 2.90(1)	
V_{hys}	LVD voltage threshold hysteresis	$V_{IT+(LVD)}$-$V_{IT-(LVD)}$	–	200	–	mV
Vt_{POR}	V_{DD} rise time rate (2)	–	20		20000	µs/V
$t_{g(VDD)}$	Filtered glitch delay on V_{DD}	Not detected by the LVD	–	–	150	ns
$I_{DD(LVD)}$	LVD/AVD current consumption	–	–	220	–	µA

Figure 54. RC Osc Freq vs V_{DD} (calibrated with RCCR0: 5V@ 25°C)

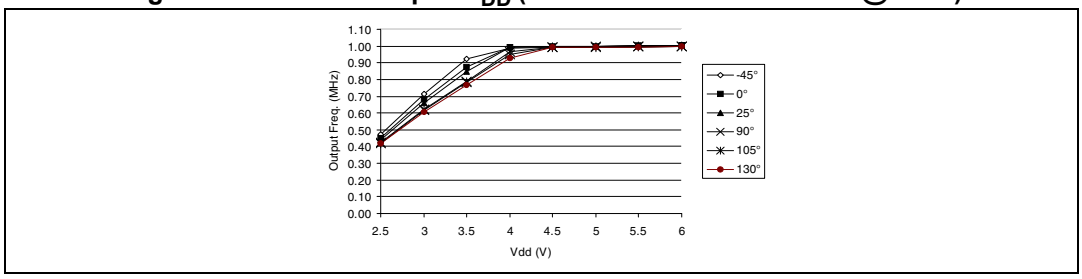


Figure 55. Typical RC oscillator Accuracy vs temperature @ V_{DD}=5V (calibrated with RCCR0: 5V @ 25°C)

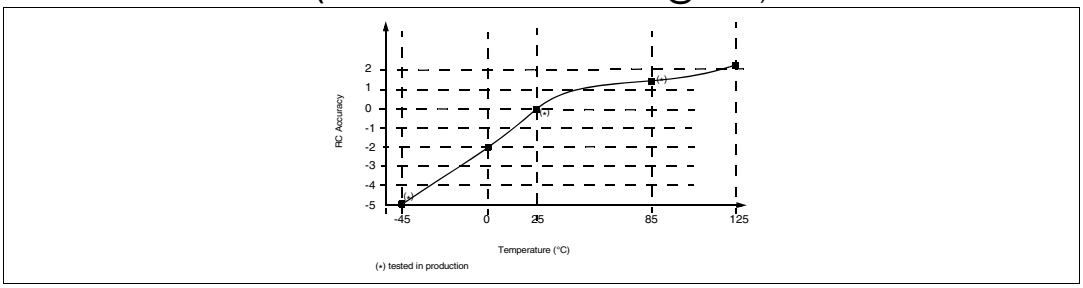


Figure 56. RC Osc Freq vs V_{DD} and RCCR Value

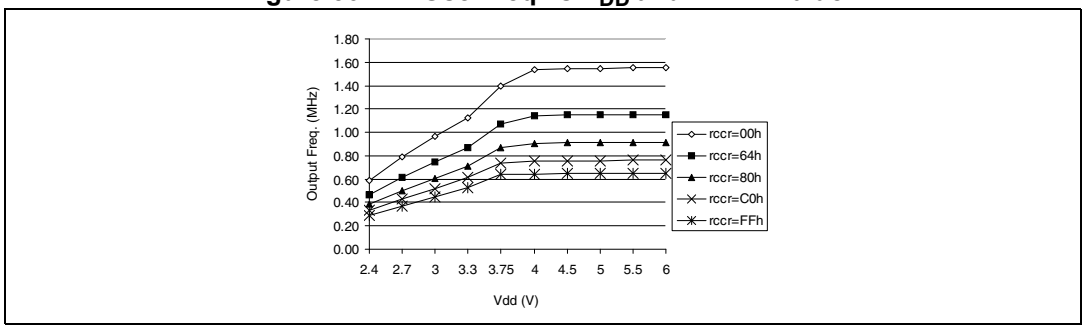


Figure 57. PLL $\Delta f_{CPU}/f_{CPU}$ versus time

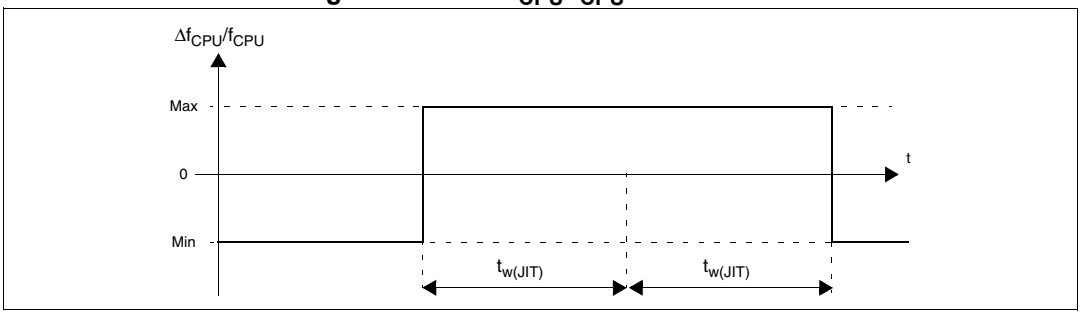


Table 77. Emission test

Symbol	Parameter	Conditions	Monitored Frequency Band	Max vs. [f_{OSC}/f_{CPU}]		Unit
				8/4MHz	16/8MHz	–
S_{EMI}	Peak level	V_{DD}=5V, T_A=+25°C, SO20 package, conforming to SAE J 1752/3	0.1 MHz to 30 MHz	9	17	dBµV
			30 MHz to 130 MHz	31	36	
			130 MHz to 1 GHz	25	27	
			SAE EMI Level	3.5	4	–

Note: Data based on characterization results, not tested in production.

13.7.3 Absolute maximum ratings (Electrical sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

Note: For more details, refer to the application note AN1181.

Electro-Static Discharge (ESD)

Electro-Static Discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard.

Table 78. Absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human body model)	T_A=+25°C	4000	V

1. Data based on characterization results, not tested in production.

Static and dynamic latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard.
- **DLU**: Electro-Static Discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards.

Note: For more details, refer to the application note AN1181.

5. The stabilization time of the AD converter is masked by the first t_{LOAD}. The first conversion after the enable is then always valid.

Figure 89. Typical application with ADC

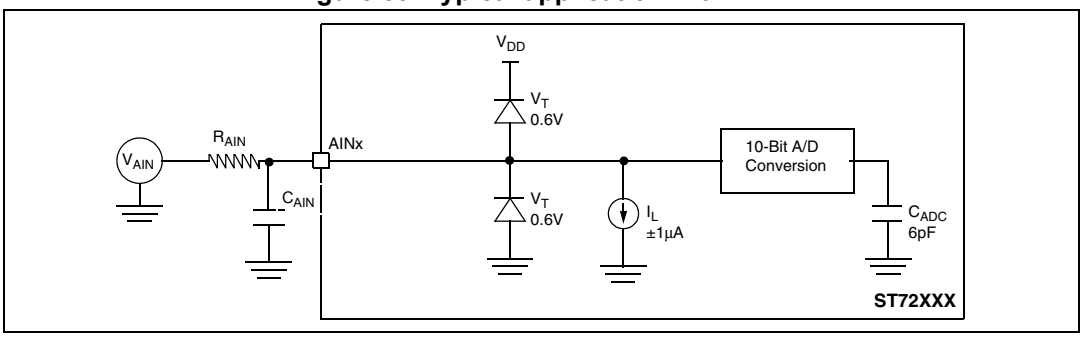


Table 85. ADC accuracy with V_{DD} = 5.0V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error(2)	f_{CPU}=8MHz, f_{ADC}=4MHz(1), VDD=5.0V	3	6	LSB
$\|E_O\|$	Offset error (2)		1.5	5	
$\|E_G\|$	Gain Error (2)		2	4.5	
$\|E_D\|$	Differential linearity error(2)		2.5	4.5	
$\|E_L\|$	Integral linearity error(2)		2.5	4.5	

1. Data based on characterization results over the whole temperature range, not tested in production.
2. Injecting negative current on any of the analog input pins significantly reduces the accuracy of any conversion being performed on any analog input.
Analog pins can be protected against negative injection by adding a Schottky diode (pin to ground).
Injecting negative current on digital input pins degrades ADC accuracy especially if performed on a pin close to the analog input pins.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma_{IINJ(PIN)}$ in *Section 13.8: I/O port pin characteristics* does not affect the ADC accuracy.

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