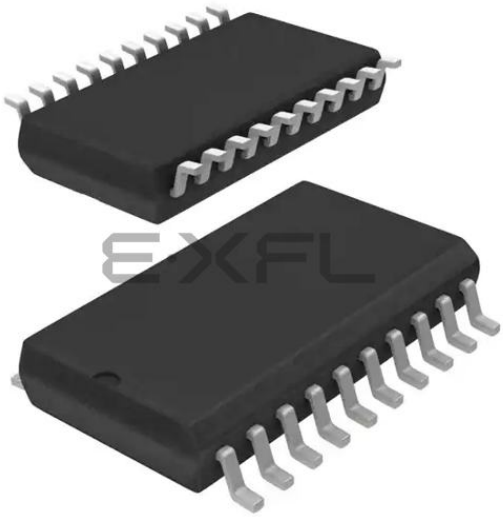

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	15
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SO
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7flite29f2m6

Table 5. DATA EEPROM register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0030h	**EECSR** Reset Value	0	0	0	0	0	0	E2LAT 0	E2PGM 0

for TA = -40 to +85°C) @ VDD = 4.5 to 5.5 V).

Refer to *Section 7.6.4: Register description* for a description of the LOCKED bit in the SICSR register.

7.3 Register description

Main clock control/status register (MCCSR)

Read / Write

Reset value: 0000 0000 (00h)

7							0
0	0	0	0	0	0	MCO	SMS

- Bits 7:2 = Reserved, must be kept cleared
- Bit 1 = **MCO** *Main Clock Out enable*
  This bit is read/write by software and cleared by hardware after a reset. This bit allows to enable the MCO output clock.
  0: MCO clock disabled, I/O port free for general purpose I/O.
  1: MCO clock enabled.
- Bit 0 = **SMS** *Slow Mode select*
  This bit is read/write by software and cleared by hardware after a reset. This bit selects the input clock f_{OSC2} or $f_{OSC2}/32$.
  0: Normal mode ($f_{CPU} = f_{OSC2}$
  1: Slow mode ($f_{CPU} = f_{OSC2}/32$)

RC control register (RCCR)

Read / Write

Reset value: 1111 1111 (FFh)

7							0
CR70	CR60	CR50	CR40	CR30	CR20	CR10	CR0

- Bits 7:0 = **CR[7:0]** *RC oscillator frequency adjustment bits*
  These bits must be written immediately after reset to adjust the RC oscillator frequency and to obtain an accuracy of 1%. The application can store the correct value for each voltage range in EEPROM and write it to this register at startup.
  00h = maximum available frequency
  FFh = lowest available frequency

Note: To tune the oscillator, write a serie of different values in the register until the correct frequency is reached. The fastest method is to use a dichotomy starting with 80h.

Note: When the Multi-oscillator is not used, PB4 is selected by default as external clock.

Crystal/ceramic oscillators

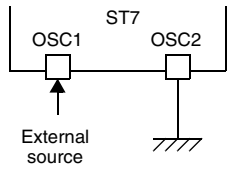
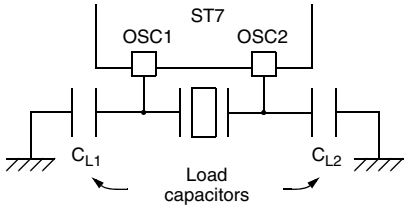
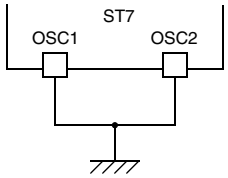
This family of oscillators has the advantage of producing a very accurate rate on the main clock of the ST7. The selection within a list of 4 oscillators with different frequency ranges has to be done by option byte in order to reduce consumption (refer to *Section 15.1: Option bytes* for more details on the frequency ranges). In this mode of the multi-oscillator, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The loading capacitance values must be adjusted according to the selected oscillator.

These oscillators are not stopped during the RESET phase to avoid losing time in the oscillator startup phase.

Internal RC oscillator

In this mode, the tunable 1% RC oscillator is used as main clock source. The two oscillator pins have to be tied to ground.

Table 7. ST7 clock sources

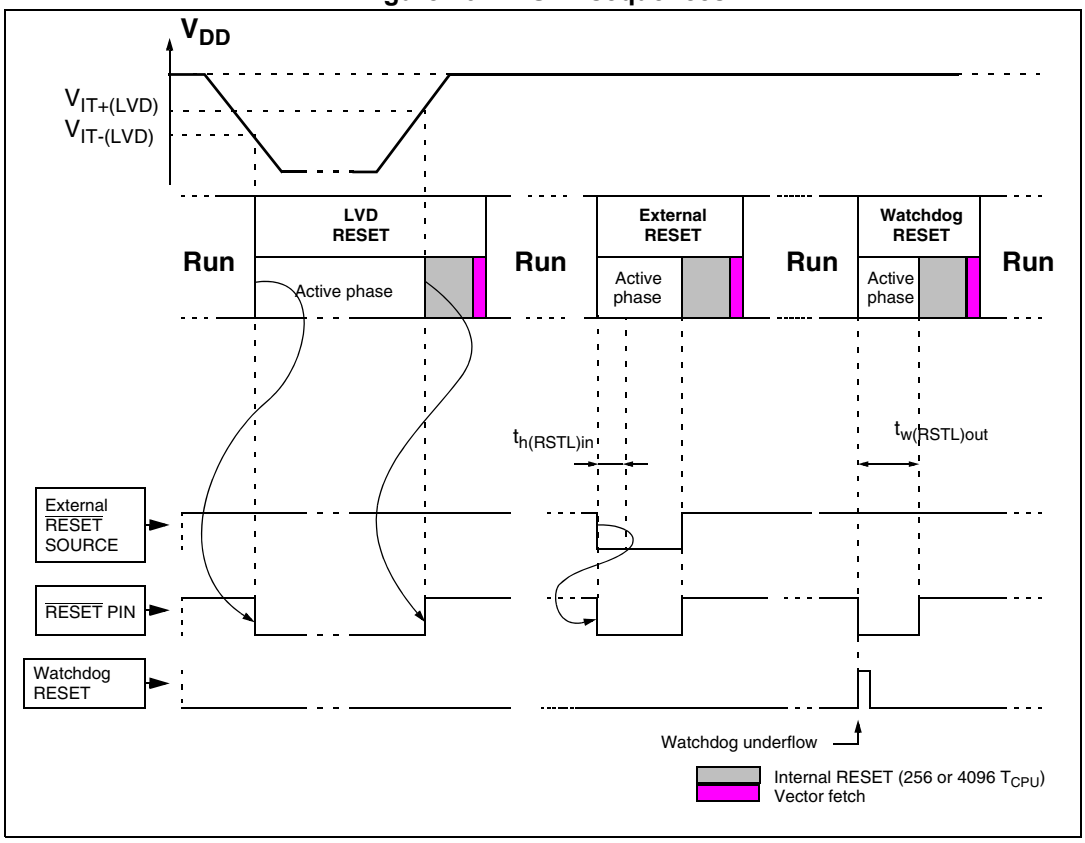
Clock source	Hardware configuration
External clock	
Crystal/ceramic resonators	
Internal RC oscillator or external clock on PB4	

7.5.5 Internal watchdog RESET

The RESET sequence generated by a internal Watchdog counter overflow is shown in *Figure 16*.

Starting from the Watchdog counter underflow, the device $\overline{\text{RESET}}$ pin acts as an output that is pulled low during at least $t_{w(RSTL)out}$.

Figure 16. RESET sequences



7.6 System integrity management (SI)

The system integrity management block contains the low voltage detector (LVD) and auxiliary voltage detector (AVD) functions. It is managed by the SICSR register.

Note: A reset can also be triggered following the detection of an illegal opcode or prebyte code. Refer to Section 12.2.1: Illegal opcode reset for further details.

7.6.1 Low voltage detector (LVD)

The low voltage detector function (LVD) generates a static reset when the V_{DD} supply voltage is below a $V_{IT-(LVD)}$ reference value. This means that it secures the power-up as well as the power-down keeping the ST7 in reset.

The $V_{IT-(LVD)}$ reference value for a voltage drop is lower than the $V_{IT+(LVD)}$ reference value for power-on in order to avoid a parasitic reset when the MCU starts running and sinks current on the supply (hysteresis).

The LVD Reset circuitry generates a reset when VDD is below:

- $V_{IT+(LVD)}$when V_{DD} is rising
- $V_{IT-(LVD)}$ when V_{DD} is falling.

The LVD function is illustrated in *Figure 17*.

The voltage threshold can be configured by option byte to be low, medium or high.

Provided the minimum V_{DD} value (guaranteed for the oscillator frequency) is above $V_{IT-(LVD)}$, the MCU can only be in two modes:

- under full software control
- in static safe reset.

In these conditions, secure operation is always ensured for the application without the need for external reset hardware.

During a Low Voltage Detector Reset, the $\overline{\text{RESET}}$ pin is held low, thus permitting the MCU to reset other devices.

Note: The LVD allows the device to be used without any external RESET circuitry.

The LVD is an optional function which can be selected by option byte.

Use of LVD with capacitive power supply: with this type of power supply, if power cuts occur in the application, it is recommended to pull V_{DD} down to 0V to ensure optimum restart conditions. Refer to circuit example in Figure 84: RESET pin protection when LVD is enabled

It is recommended to make sure that the V_{DD} supply voltage rises monotonously when the device is exiting from Reset, to ensure the application functions properly.

Figure 17. Low voltage detector vs. Reset

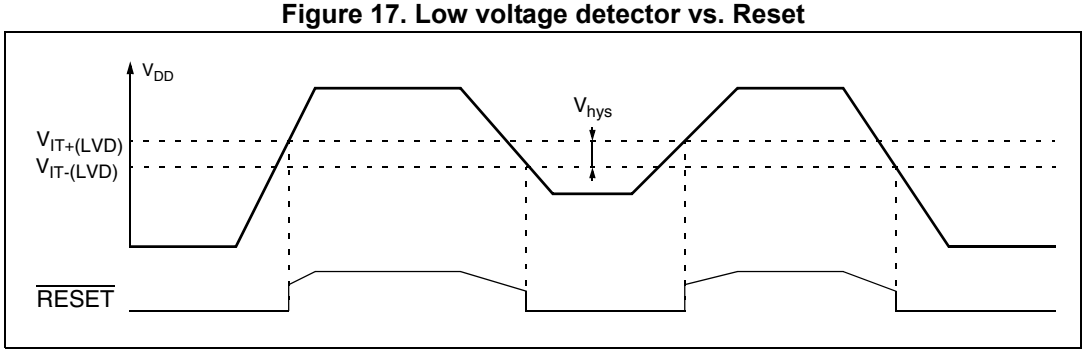
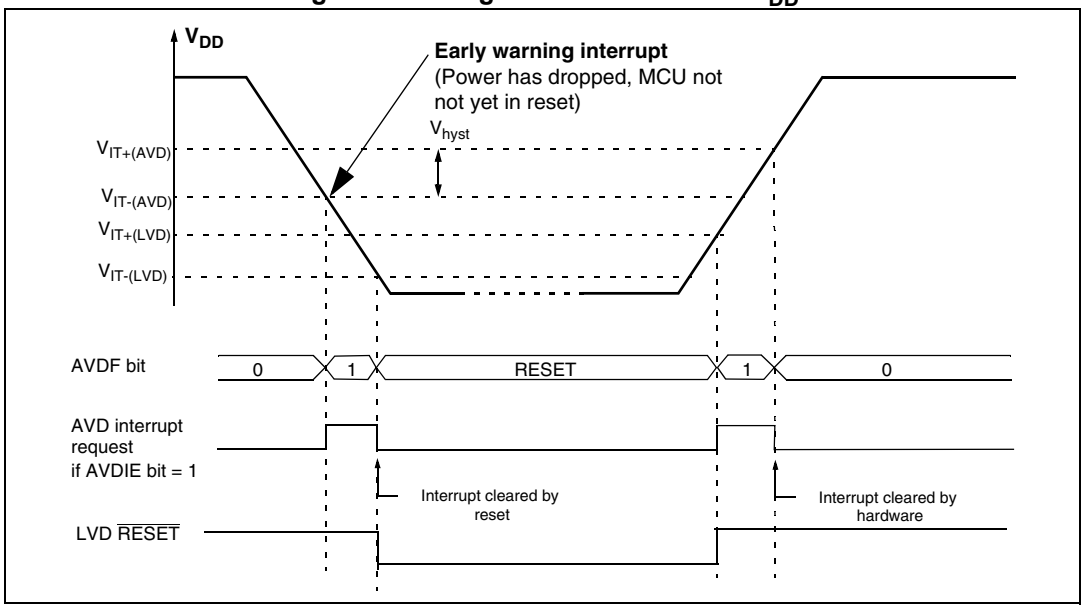


Figure 19. Using the AVD to monitor V_{DD}



7.6.3 Low power modes

Table 9. Effect of low power modes on SI

Mode	Description
WAIT	No effect on SI. AVD interrupts cause the device to exit from WAIT mode.
HALT	The SICSR register is frozen. The AVD remains active.

Interrupts

The AVD interrupt event generates an interrupt if the corresponding enable control bit (AVDIE) is set and the interrupt mask in the CC register is reset (RIM instruction).

Table 10. Interrupt control bits

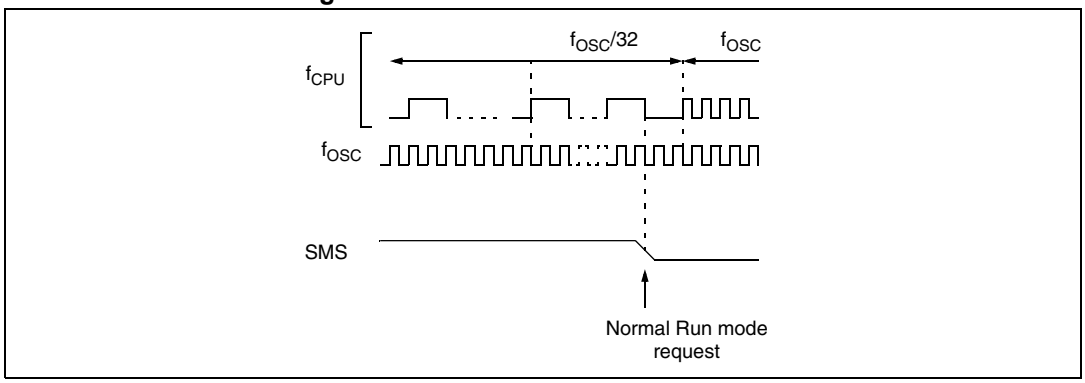
Interrupt event	Event flag	Enable control bit	Exit from Wait	Exit from Halt
AVD event	AVDF	AVDIE	Yes	No

SLOW mode is controlled by the SMS bit in the MCCSR register which enables or disables SLOW mode.

In this mode, the oscillator frequency is divided by 32. The CPU and peripherals are clocked at this lower frequency.

Note: SLOW-WAIT mode is activated when entering WAIT mode while the device is already in SLOW mode.

Figure 22. SLOW mode clock transition



9.3 WAIT mode

WAIT mode places the MCU in a low power consumption mode by stopping the CPU.

This power saving mode is selected by calling the “WFI” instruction.

All peripherals remain active. During WAIT mode, the I bit of the CC register is cleared, to enable all interrupts. All other registers and memory remain unchanged. The MCU remains in WAIT mode until an interrupt or RESET occurs, whereupon the Program Counter branches to the starting address of the interrupt or Reset service routine.
The MCU will remain in WAIT mode until a RESET or an Interrupt occurs, causing it to wake up.

Refer to *Figure 23*.

interrupt). Refer to *Table 12: Interrupt mapping* for more details.

4. Before servicing an interrupt, the CC register is pushed on the stack. The I[1:0] bits of the CC register are set to the current software priority level of the interrupt routine and recovered when the CC register is popped.
5. If the PLL is enabled by option byte, it outputs the clock after an additional delay of $t_{STARTUP}$ (see *Figure 12: PLL output frequency timing diagram*).

9.6.1 Register description

AWUF control/status register (CR)

Read/Write

Reset value: 0000 0000 (0Ch)

7							0
0	0	0	0	0	AWUF	AWUM	AWUEN

- Bits 7:3 = Reserved
- Bit 2 = **AWUF** *Auto-Wakeup Flag*
  This bit is set by hardware when the AWU module generates an interrupt and cleared by software on reading AWUCSR. Writing to this bit does not change its value.
  0: No AWU interrupt occurred
  1: AWU interrupt occurred
- Bit 1= **AWUM** *Auto-Wakeup Measurement*
  This bit enables the AWU RC oscillator and connects its output to the input capture of the 12-bit Auto-Reload timer. This allows the timer to be used to measure the AWU RC oscillator dispersion and then compensate this dispersion by providing the right value in the AWUPRE register.
  0: Measurement disabled
  1: Measurement enabled
- Bit 0 = **AWUEN** *Auto Wake Up From Halt Enabled*
  This bit enables the Auto Wake Up From Halt feature:
  once HALT mode is entered, the AWUF wakes up the microcontroller after a time delay dependent on the AWU prescaler value. It is set and cleared by software.
  0: AWUF (Auto Wake Up From Halt) mode disabled
  1: AWUF (Auto Wake Up From Halt) mode enabled

Table 26. Ports PA7:0, PB6:0 (continued)

Mode	DDR	OR
Open drain output	1	0
Push-pull output	1	1

Table 27. Port configuration (standard ports)

Port	Pin name	Input		Output	
		OR = 0	OR = 1	OR = 0	OR = 1
Port A	PA7:0	Floating	Pull-up	Open drain	Push-pull
Port B	PB6:0	Floating	Pull-up	Open drain	Push-pull

Note: On ports where the external interrupt capability is selected using the EISR register, the configuration will be as follows:

Table 28. Port configuration (Interrupt ports)

Port	Pin name	Input		Output	
		OR = 0	OR = 1	OR = 0	OR = 1
Port A	PA7:0	Floating	Pull-up interrupt	Open drain	Push-pull
Port B	PB6:0	Floating	Pull-up interrupt	Open drain	Push-pull

Interrupt ports

Table 29. Ports where the external interrupt capability selected using the EISR register

Mode	DDR	OR
Floating input	0	0
Pull-up interrupt input	0	1
Open drain output	1	0
Push-pull output	1	1

Table 30. I/O port register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0000h	**PADR** Reset value	MSB 1	1	1	1	1	1	1	LSB 1
0001h	**PADDR** Reset value	MSB 0	0	0	0	0	0	0	LSB 0
0002h	**PAOR** Reset value	MSB 0	1	0	0	0	0	0	LSB 0

11 On-chip peripherals

11.1 Watchdog timer (WDG)

11.1.1 Introduction

The Watchdog timer is used to detect the occurrence of a software fault, usually generated by external interference or by unforeseen logical conditions, which causes the application program to abandon its normal sequence. The Watchdog circuit generates an MCU reset on expiry of a programmed time period, unless the program refreshes the counter's contents before the T6 bit becomes cleared.

11.1.2 Main features

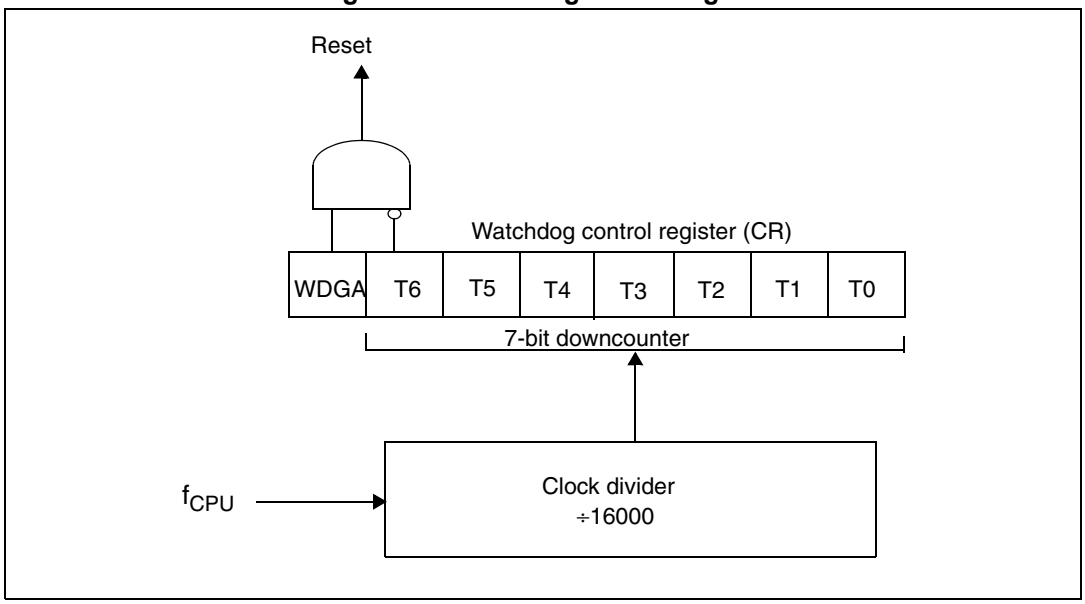
- Programmable free-running downcounter (64 increments of 16000 CPU cycles)
- Programmable reset
- Reset (if watchdog activated) when the T6 bit reaches zero
- Optional reset on HALT instruction (configurable by option byte)
- Hardware Watchdog selectable by option byte.

11.1.3 Functional description

The counter value stored in the CR register (bits T[6:0]), is decremented every 16000 machine cycles, and the length of the time-out period can be programmed by the user in 64 increments.

If the watchdog is activated (the WDGA bit is set) and when the 7-bit timer (bits T[6:0]) rolls over from 40h to 3Fh (T6 becomes cleared), it initiates a reset cycle pulling low the reset pin for typically 30µs.

Figure 33. Watchdog block diagram



Input capture register high (ATICRH)

Read only

Reset Value: 0000 0000 (00h)

15							8
0	0	0	0	ICR11	ICR10	ICR9	ICR8

Input capture register low (ATICRL)

Read only

Reset Value: 0000 0000 (00h)

7							0
ICR7	ICR6	ICR5	ICR4	ICR3	ICR2	ICR1	ICR0

- Bits 15:12 = Reserved.
- Bits 11:0 = **ICR[11:0]** *Input capture data*.
  This is a 12-bit register which is readable by software and cleared by hardware after a reset. The ATICR register contains captured the value of the 12-bit CNTR register when a rising or falling edge occurs on the ATIC pin. Capture will only be performed when the ICF flag is cleared.

Transfer control register (TRANCR)

Read/Write

Reset Value: 0000 0001 (01h)

7							0
0	0	0	0	0	0	0	TRAN

- Bits 7:1 Reserved. Forced by hardware to 0.
- Bit 0 = **TRAN** *Transfer enable*
  This bit is read/write by software, cleared by hardware after each completed transfer and set by hardware after reset.
  It allows the value of the DCRx registers to be transferred to the DCRx shadow registers after the next overflow event.
  The OPx bits are transferred to the shadow OPx bits in the same way.

Table 36. Register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0D	**ATCSR** Reset value	0	ICF 0	ICIE 0	CK1 0	CK0 0	OVF 0	OVFIE 0	CMPIE 0
0E	**CNTRH** Reset value	0	0	0	0	CNTR11 0	CNTR10 0	CNTR9 0	CNTR8 0

11.3 Lite timer 2 (LT2)

11.3.1 Introduction

The Lite timer can be used for general-purpose timing functions. It is based on two free-running 8-bit upcounters, an 8-bit input capture register.

11.3.2 Main features

- Real-time clock
  - One 8-bit upcounter 1 ms or 2 ms timebase period (@ 8 MHz f_{OSC})
  - One 8-bit upcounter with autoreload and programmable timebase period from 4µs to 1.024 ms in 4 µs increments (@ 8 MHz f_{OSC})
  - 2 Maskable timebase interrupts.
- Input capture
  - 8-bit input capture register (LTICR)
  - Maskable interrupt with wakeup from HALT mode capability.

Figure 40. Lite timer 2 block diagram

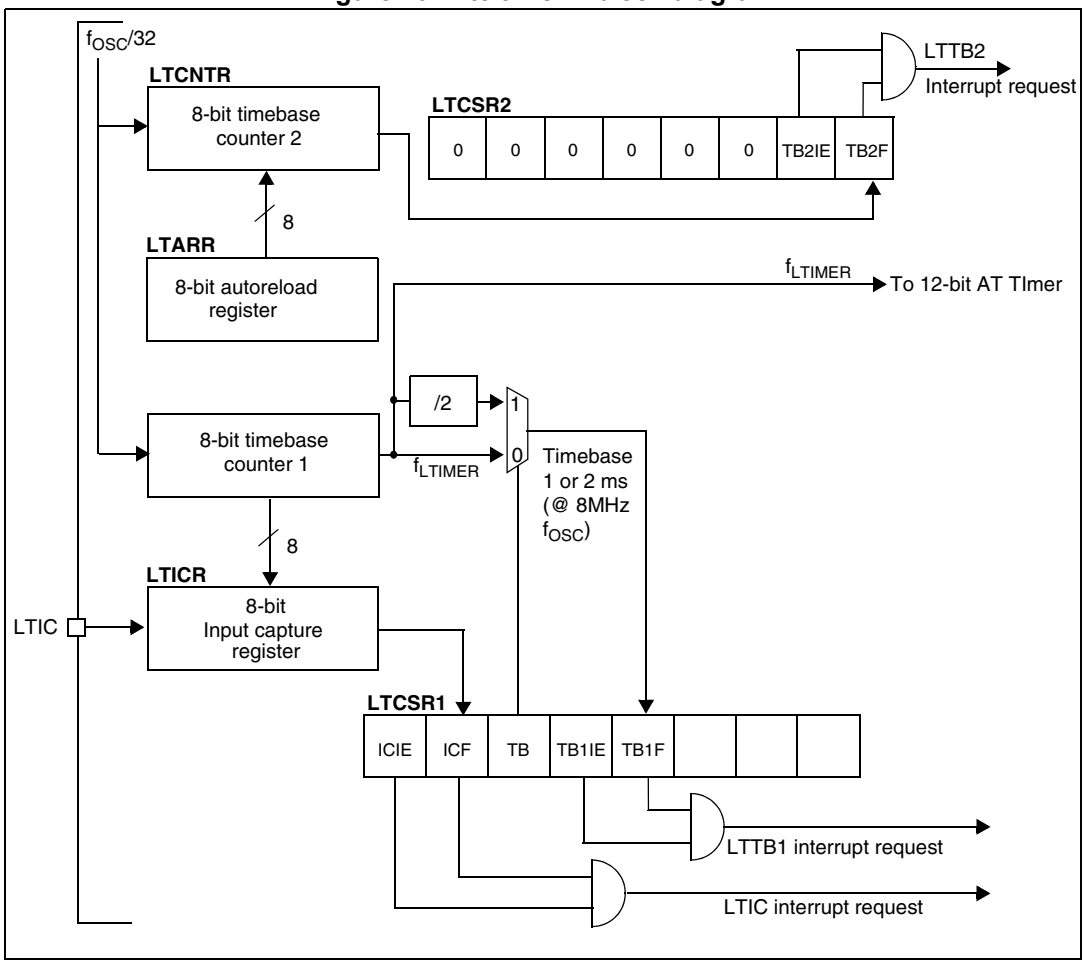
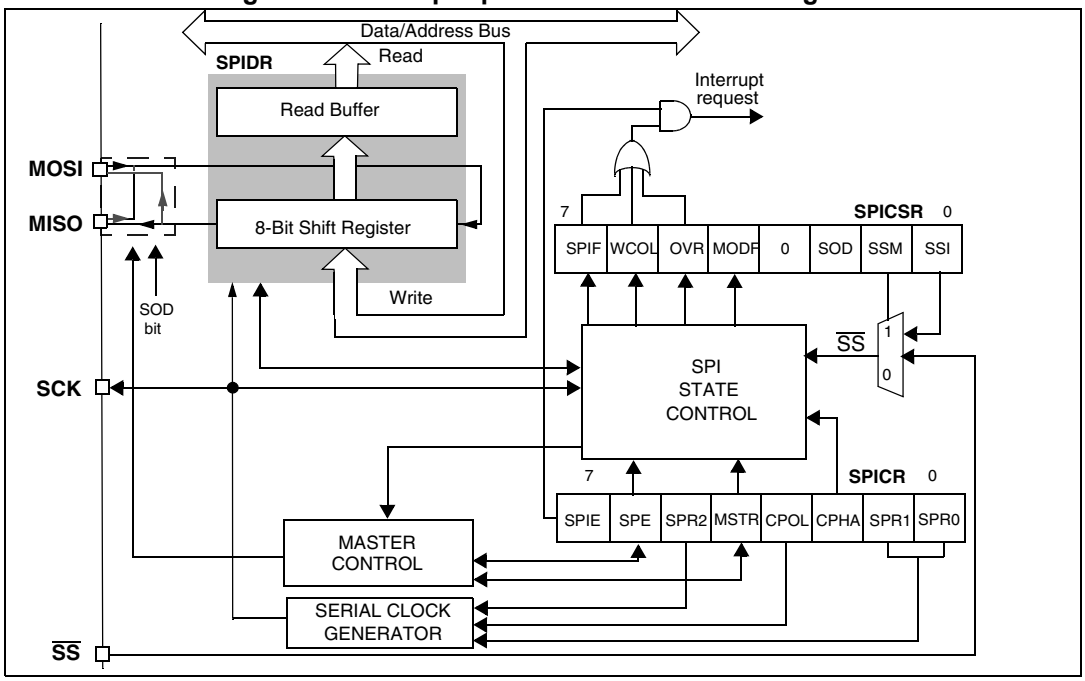


Figure 42. Serial peripheral interface block diagram



Functional description

A basic example of interconnections between a single master and a single slave is illustrated in *Figure 43: Single master/ single slave application*.

The MOSI pins are connected together and the MISO pins are connected together. In this way data is transferred serially between master and slave (most significant bit first).

The communication is always initiated by the master. When the master device transmits data to a slave device via MOSI pin, the slave device responds by sending data to the master device via the MISO pin. This implies full duplex communication with both data out and data in synchronized with the same clock signal (which is provided by the master device via the SCK pin).

To use a single data line, the MISO and MOSI pins must be connected at each node (in this case only simplex communication is possible).

Four possible data/clock timing relationships may be chosen (see *Figure 46: Data clock timing diagram*) but master and slave must be programmed with the same timing mode.

For example, if V_{DD} = 5 V, then the ADC can convert voltages in the range 0 V to 430 mV with an ideal resolution of 0.6 mV (equivalent to 13-bit resolution with reference to a V_{SS} to V_{DD} range).

Note: For more details, refer to Section 13: Electrical characteristics.
The amplifier is switched on by the ADON bit in the ADCCSR register, so no additional startup time is required when the amplifier is selected by the AMPSEL bit.

Digital A/D conversion result

The conversion is monotonic, meaning that the result never decreases if the analog input does not and never increases if the analog input does not.

If the input voltage (V_{AIN}) is greater than V_{DDA} (high-level voltage reference) then the conversion result is FFh in the ADCDRH register and 03h in the ADCDRL register (without overflow indication).

If the input voltage (V_{AIN}) is lower than V_{SSA} (low-level voltage reference) then the conversion result in the ADCDRH and ADCDRL registers is 00 00h.

The A/D converter is linear and the digital result of the conversion is stored in the ADCDRH and ADCDRL registers. The accuracy of the conversion is described in *Section 13: Electrical characteristics*.

R_{AIN} is the maximum recommended impedance for an analog input signal. If the impedance is too high, this will result in a loss of accuracy due to leakage and sampling not being completed in the allowed time.

A/D Conversion

The analog input ports must be configured as input, no pull-up, no interrupt. *Section 10: I/O ports*. Using these pins as analog inputs does not affect the ability of the port to be read as a logic input.

In the ADCCSR register, select the CS[2:0] bits to assign the analog channel to convert.

ADC Conversion mode

- In the ADCCSR register:
  - set the ADON bit to enable the A/D converter and to start the conversion. From this time on, the ADC performs a continuous conversion of the selected channel.
- When a conversion is complete:
  - the EOC bit is set by hardware.
  - the result is in the ADCDR registers.

A read to the ADCDRH resets the EOC bit.

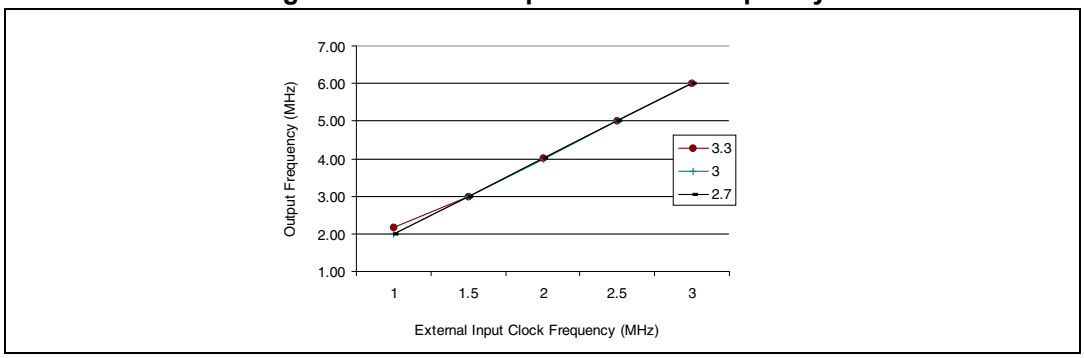
To read the 10 bits, perform the following steps:

1. Poll EOC bit
2. Read ADCDRL
3. Read ADCDRH. This clears EOC automatically.

To read only 8 bits, perform the following steps:

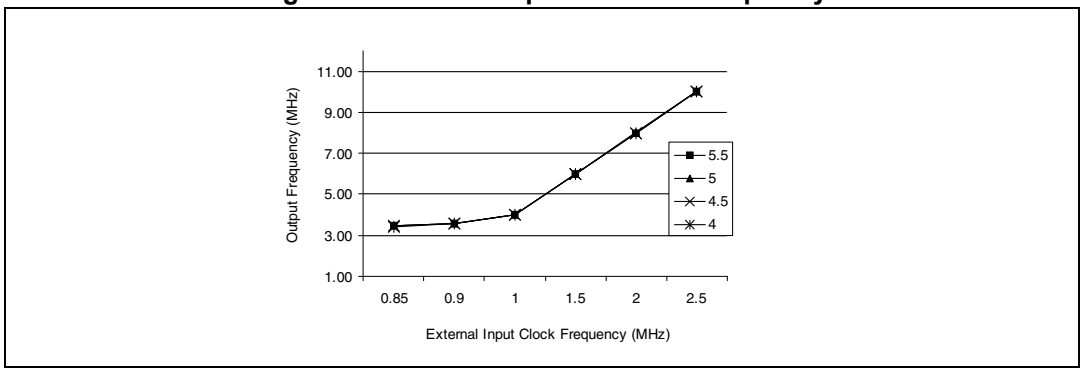
1. Poll EOC bit
2. Read ADCDRH. This clears EOC automatically.

Figure 58. PLLx4 Output vs CLKIN frequency



1. $f_{OSC} = f_{CLKIN}/2*PLL4$

Figure 59. PLLx8 Output vs CLKIN frequency



1. $f_{OSC} = f_{CLKIN}/2*PLL8$

Table 65. 32 MHz PLL

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Voltage (1)	4.5	5	5.5	V
f_{PLL32}	Frequency (1)	–	32	–	MHz
f_{INPUT}	Input Frequency	7	8	9	MHz

1. 32 MHz is guaranteed within this voltage range.

Note: T_A = -40 to 85°C, unless otherwise specified.

13.4 Supply current characteristics

The following current consumption specified for the ST7 functional operating modes over temperature range does not take into account the clock source current consumption. To get the total device consumption, the two current values must be added (except for HALT mode for which the clock is stopped).

Table 66. Supply current

Symbol	Parameter	Conditions	Typ	Max	Unit
I_{DD}	Supply current in Run mode	External Clock, f_{CPU} = 1MHz(1)	1	–	mA
		Internal RC, f_{CPU}=1MHz	2.2	–	
		f_{CPU}=8MHz(1)	7.5	12	
	Supply current in WAIT mode	External Clock, f_{CPU}=1MHz(2)	0.8	–	
		Internal RC, f_{CPU}=1MHz	1.8	–	
		f_{CPU} = 8MHz(2)	3.7	6	
	Supply current in SLOW mode	f_{CPU} = 250kHz(3)	1.6	2.5	
	Supply current in SLOW-wait mode	f_{CPU} = 250kHz(4)	1.6	2.5	
	Supply current in HALT mode(5)	-40°C≤T_A≤+85°C	1	10	µA
		T_A = +125°C	15	50	
	Supply current in AWUF mode(6)	T_A = +25°C	20	30	

1. CPU running with memory access, all I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load), all peripherals in reset state; clock input (CLKIN) driven by external square wave, LVD disabled.
2. All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load), all peripherals in reset state; clock input (CLKIN) driven by external square wave, LVD disabled.
3. SLOW mode selected with f_{CPU} based on f_{OSC} divided by 32. All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load), all peripherals in reset state; clock input (CLKIN) driven by external square wave, LVD disabled.
4. SLOW-WAIT mode selected with f_{CPU} based on f_{OSC} divided by 32. All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load), all peripherals in reset state; clock input (CLKIN) driven by external square wave, LVD disabled.
5. All I/O pins in output mode with a static value at V_{SS} (no load), LVD disabled. Data based on characterization results, tested in production at V_{DD} max and fCPU max.
6. All I/O pins in input mode with a static value at VDD or VSS (no load). Data tested in production at VDD max. and f_{CPU} max.
   This consumption refers to the Halt period only and not the associated run period which is software dependent.

Note: TA = -40 to +85°C unless otherwise specified, V_{DD}=5.5V.

Figure 60. Tipical I_{DD} in RUN vs. f_{CPU}

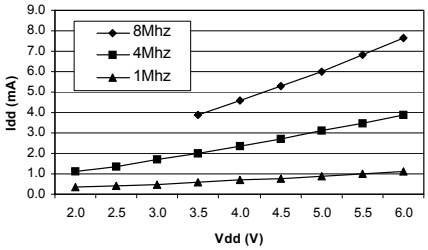


Figure 92. Amplifier noise vs voltage

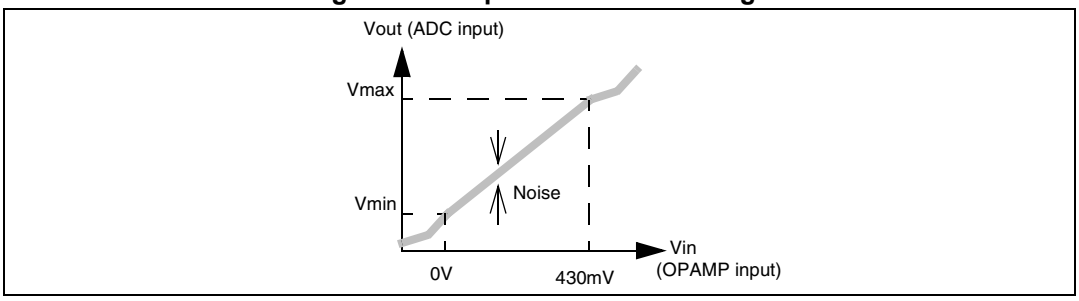


Table 86. ADC characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(AMP)}$	Amplifier operating voltage	–	3.6	–	5.5	V
V_{IN}	Amplifier input voltage(2)	V_{DD}=3.6V	0	–	350	mV
		V_{DD}=5V	0	–	500	
V_{OFFSET}	Amplifier output offset voltage(3)	V_{DD}=5V	–	200	–	mV
V_{STEP}	Step size for monotonicity(4)	V_{DD}=3.6V	3.5	–	–	mV
		V_{DD}=5V	4.89	–	–	
Linearity	Output voltage response	–	Linear			
Gain factor	Amplified analog input gain(5)	–	–	8	–	–
Vmax	Output linearity max voltage	V_{INmax} = 430mV, V_{DD}=5V	–	3.65	3.94	V
Vmin	Output linearity min voltage		–	200	–	mV

1. Data based on characterization results over the whole temperature range, not tested in production.
2. Please refer to the application note AN1830 for details of TE% vs V_{in}.
3. Refer to the offset variation in temperature below.
4. Monotonicity guaranteed if V_{IN} increases or decreases in steps of min. 5mV.
5. For precise conversion results, it is recommended to calibrate the amplifier at the following two points:
–offset at V_{INmin} = 0V
–gain at full scale (for example V_{IN}=430mV).

13.11.1 Amplifier output offset variation

The offset is quite sensitive to temperature variations. In order to ensure a good reliability in measurements, the offset must be recalibrated periodically i.e. during power on or whenever the device is reset depending on the customer application and during temperature variation. *Table 87* gives the typical offset variation over temperature.

Table 87. Typical offset variation over temperature

Typical offset variation (LSB)				Unit
-45	-20	+25	+90	°C
-12	-7	–	+13	LSB

Figure 94. 20-pin plastic dual in-line package, 300-mil width

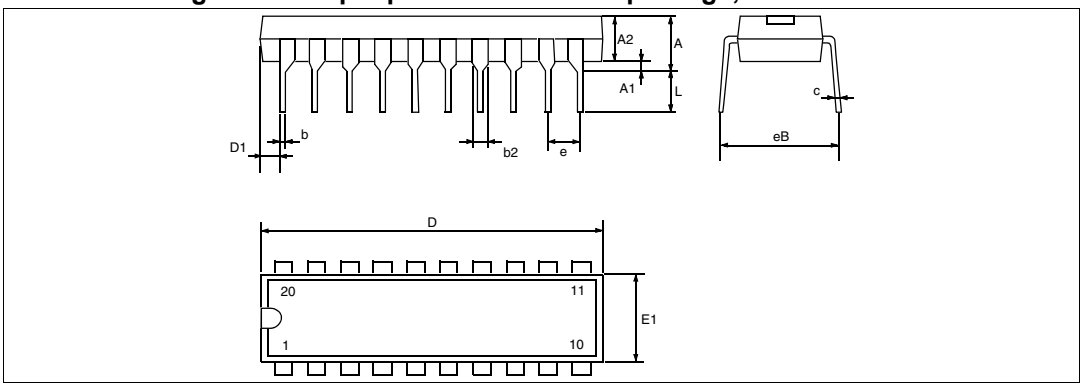


Table 89. Dual in-line package characteristics

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	–	–	5.33	–	–	0.210
A1	0.38	–	–	0.015	–	–
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	24.89	26.16	26.92	0.980	1.030	1.060
D1	0.13	–	–	0.005	–	–
e	–	2.54	–	–	0.100	–
eB	–	–	10.92	–	–	0.430
E1	6.10	6.35	7.11	0.240	0.250	0.280
L	2.92	3.30	3.81	0.115	0.130	0.150
	Number of Pins					
N	20					

Table 97. Supported part numbers

Part number	Program memory (Bytes)	RAM (Bytes)	Data EEPROM (Bytes)	Temp. range	Package
ST7FLITE20F2B6	8K Flash	384	–	-40 °C to +85 °C	DIP20
ST7FLITE20F2M6					SO20
ST7FLITE25F2B6			–		DIP20
ST7FLITE25F2M6					SO20
ST7FLITE29F2B6			256		DIP20
ST7FLITE29F2M6					SO20
ST7FLITE29F2M7				-40 °C to +105 °C	SO20
ST7PLITE20F2B6	8K FASTROM	384	–	-40 °C to +85 °C	DIP20
ST7PLITE20F2M6					SO20
ST7PLITE25F2B6			–		DIP20
ST7PLITE25F2M6					SO20
ST7PLITE29F2B6			256		DIP20
ST7PLITE29F2M6					SO20

Note: Contact ST sales office for product availability.

Table 98. ST7LITE2 FASTROM microcontroller option list

Customer
Address

Contact
Phone N°
Reference/FASTROM code (assigned by STMicroelectronics)
FASTROM code must be sent in .S19 format. .Hex extension cannot be processed.

Device Type/Memory Size/Package (check only one option):

FASTROM device	8K
SO20:	[ ] ST7PLITE20F2M6
	[ ] ST7PLITE25F2M6
	[ ] ST7PLITE29F2M6
	[ ] ST7FLITE29F2M7
DIP20:	[ ] ST7PLITE20F2B6
	[ ] ST7PLITE25F2B6
	[ ] ST7PLITE29F2B6

Note: Addresses 1000h, 1001h, FFDEh and FFDFh are reserved areas for ST to program RCCR0 and RCCR1 (see Section 7.1: Internal RC oscillator adjustment).

Conditioning (do not specify for DIP package)

[ ] Tape & Reel[ ] Tube
Special marking: [ ] No [ ] Yes "_ _ _ _ _ _ _ _ "
Authorized characters are letters, digits, '.', '-', '/' and spaces only.
Maximum character count:
DIP20/S020 (8 char. max) : _ _ _ _ _ _ _ _
Watchdog Selection:[ ] Software Activation[ ] Hardware Activation
Watchdog Reset on HALT:[ ] Reset[ ] No Reset
LVD Reset[ ] Disabled[ ] Enabled
[ ] Highest threshold
[ ] Medium threshold
[ ] Lowest threshold
Sector 0 size:[ ] 0.5K[ ] 1K [ ] 2K[ ] 4K
Read-out Protection:[ ] Disabled[ ] Enabled
FLASH write Protection:[ ] Disabled[ ] Enabled
Clock Source Selection:[ ] Resonator:
[ ] VLP: Very Low power resonator (32 to 100 kHz)
[ ] LP: Low power resonator (1 to 2 MHz)
[ ] MP: Medium power resonator (2 to 4 MHz)
[ ] MS: Medium speed resonator (4 to 8 MHz)
[ ] HS: High speed resonator (8 to 16 MHz)
[ ] External Clock:
[ ] On OSC1

Note: Not all configurations are available. See Table 96 for authorized option byte combinations.