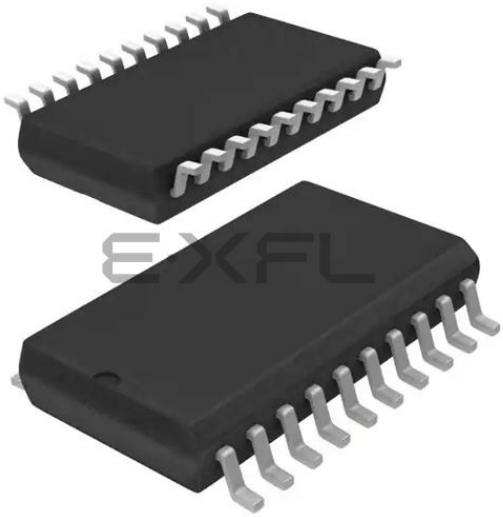


Welcome to E-XFL.COM

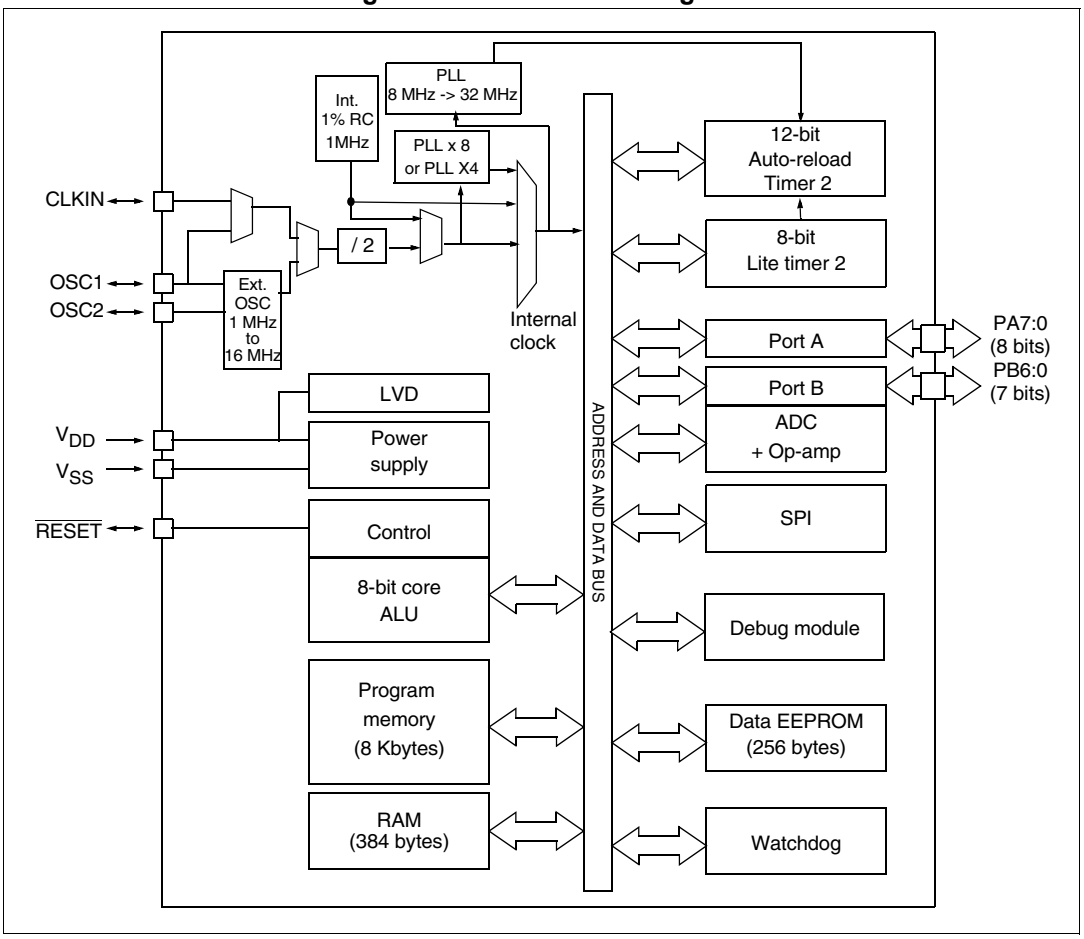
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	15
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SO
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7flite29f2m6tr

Figure 1. General block diagram



Port and control configuration:

- Input:
  - float = floating, wpu = weak pull-up, int = interrupt, ana = analog
- Output:
  - OD = open drain
  - PP = push-pull

The RESET configuration of each pin is shown in bold which is valid as long as the device is in reset state.

Table 2. Device pin description

Pin No.		Pin name	Type	Level		Port / Control						Main function (after reset)	Alternate function
						Input				Output			
SO20	DIP20			Input	Output	float	wpu	int	ana	OD	PP		
1	16	V_{SS}	S	-	-	-	-	-	-	-	-	Ground	
2	17	V_{DD}	S	-	-	-	-	-	-	-	-	Main power supply	
3	18	$\overline{RESET}$	I/O	C_T	-	-	X	-	-	X	-	Top priority non maskable interrupt (active low)	
4	19	PB0/AIN0/$\overline{SS}$	I/O	C_T		**X**	ei3		X	X	X	**Port B0**	ADC analog input 0 or SPI Slave Select (active low)(1)
5	20	PB1/AIN1/SCK	I/O	C_T		**X**			X	X	X	**Port B1**	ADC analog input 1 or SPI Serial Clock(1)
6	1	PB2/AIN2/MISO	I/O	C_T		**X**			X	X	X	**Port B2**	ADC analog input 2 or SPI Master in/ Slave out data
7	2	PB3/AIN3/MOSI	I/O	C_T		**X**	ei2		X	X	X	**Port B3**	ADC analog input 3 or SPI Master out / Slave in data
8	3	PB4/AIN4/CLKIN	I/O	C_T		**X**			X	X	X	**Port B4**	ADC analog input 4 or external clock input
9	4	PB5/AIN5	I/O	C_T		**X**			X	X	X	**Port B5**	ADC analog input 5
10	5	PB6/AIN6	I/O	C_T		**X**			X	X	X	**Port B6**	ADC analog input 6
11	6	PA7	I/O	C_T	HS	**X**	ei1		-	X	X	**Port A7**	-
12	7	PA6 /MCO/ ICCCLK/BREAK	I/O	C_T		X	ei1		-	X	X	**Port A6**	Main clock output or in circuit communication clock or external BREAK(2)
13	8	PA5 /ATPWM3/ ICCDATA	I/O	C_T	HS	**X**	ei1		-	X	X	**Port A5**	Auto-reload timer PWM3 or In circuit communication data
14	9	PA4/ATPWM2	I/O	C_T	HS	**X**			-	X	X	**Port A4**	Auto-reload timer PWM2

4 Flash program memory

4.1 Introduction

The ST7 single voltage extended Flash (XFlash) is a non-volatile memory that can be electrically erased and programmed either on a byte-by-byte basis or up to 32 bytes in parallel.

The XFlash devices can be programmed off-board (plugged in a programming tool) or on-board using in-circuit programming or in-application programming.

The array matrix organization allows each sector to be erased and reprogrammed without affecting other sectors.

4.2 Main features

- ICP (in-circuit programming)
- IAP (in-application programming)
- ICT (in-circuit testing) for downloading and executing user application test patterns in RAM
- Sector 0 size configurable by option byte
- Read-out and write protection

4.3 Programming modes

The ST7 can be programmed in three different ways:

- Insertion in a programming tool. In this mode, Flash sectors 0 and 1, option byte row and data EEPROM (if present) can be programmed or erased.
- In-circuit programming. In this mode, Flash sectors 0 and 1, option byte row and data EEPROM (if present) can be programmed or erased without removing the device from the application board.
- In-application programming. In this mode, sector 1 and data EEPROM (if present) can be programmed or erased without removing the device from the application board and while the application is running.

4.3.1 In-circuit programming (ICP)

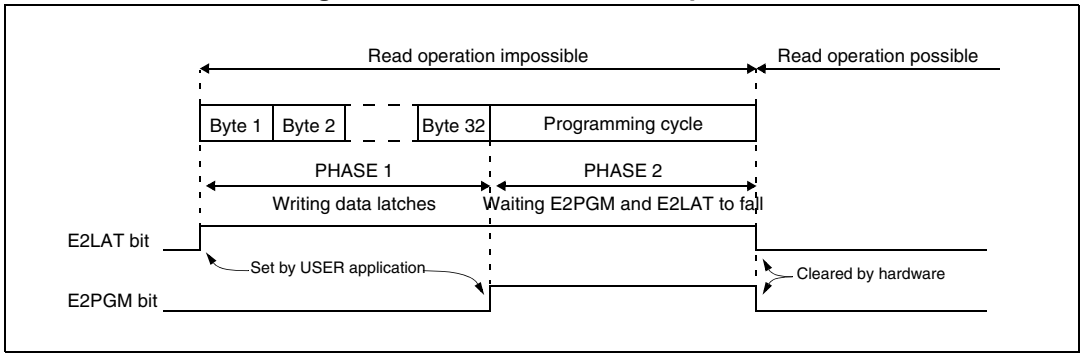
ICP uses a protocol called ICC (in-circuit communication) which allows an ST7 plugged on a printed circuit board (PCB) to communicate with an external programming device connected via cable. ICP is performed in three steps:

1. Switch the ST7 to ICC mode (in-circuit communications). This is done by driving a specific signal sequence on the ICCCLK/DATA pins while the RESET pin is pulled low. When the ST7 enters ICC mode, it fetches a specific RESET vector which points to the ST7 System Memory containing the ICC protocol routine. This routine enables the ST7 to receive bytes from the ICC interface.
2. Download ICP driver code in RAM from the ICCDATA pin.
3. Execute ICP driver code in RAM to program the Flash memory.

Table 4. Row definition

⇓ Row / Byte ⇒	0	1	2	3	...	30	31	Physical address
0								00h...1Fh
1								20h...3Fh
...								
N								Nx20h...Nx20h+1Fh

Figure 8. Data EEPROM Write operation



Note: If a programming cycle is interrupted (by a reset action), the integrity of the data in memory is not guaranteed.

5.4 Power saving modes

WAIT mode

The DATA EEPROM can enter WAIT mode on execution of the WFI instruction of the microcontroller or when the microcontroller enters ACTIVE-HALT mode.The DATA EEPROM will immediately enter this mode if there is no programming in progress, otherwise the DATA EEPROM will finish the cycle and then enter WAIT mode.

ACTIVE-HALT mode

Refer to WAIT mode.

HALT mode

The DATA EEPROM immediately enters HALT mode if the microcontroller executes the HALT instruction. Therefore the EEPROM will stop the function in progress, and data may be corrupted.

5.5 Access error handling

If a read access occurs while E2LAT=1, then the data bus will not be driven.

If a write access occurs while E2LAT=0, then the data on the bus will not be latched.

If a programming cycle is interrupted (by a RESET action), the memory data will not be guaranteed.

by software in the interrupt routine, pending interrupts are serviced regardless of the priority level of the current interrupt routine.

- Bit 2 = **N** *Negative*

  This bit is set and cleared by hardware. It is representative of the result sign of the last arithmetic, logical or data manipulation. It is a copy of the 7th bit of the result.
  0: The result of the last operation is positive or null
  1: The result of the last operation is negative
  (i.e. the most significant bit is a logic 1)

  This bit is accessed by the JRMI and JRPL instructions.

- Bit 1 = **Z** *Zero*

  This bit is set and cleared by hardware. This bit indicates that the result of the last arithmetic, logical or data manipulation is zero.
  0: The result of the last operation is different from zero
  1: The result of the last operation is zero

  This bit is accessed by the JREQ and JRNE test instructions.

- Bit 0 = **C** *Carry/borrow*

  This bit is set and cleared by hardware and software. It indicates an overflow or an underflow has occurred during the last arithmetic operation.
  0: No overflow or underflow has occurred
  1: An overflow or underflow has occurred

  This bit is driven by the SCF and RCF instructions and tested by the JRC and JRNC instructions. It is also affected by the “bit test and branch”, shift and rotate instructions.

Stack pointer register (SP)

Read/Write

Reset value: 01FFh

15							**8**
0	0	0	0	0	0	0	1
7							**0**
1	SP6	SP5	SP4	SP3	SP2	SP1	SP0

The Stack Pointer is a 16-bit register which is always pointing to the next free location in the stack. It is then decremented after data has been pushed onto the stack and incremented before data is popped from the stack (see *Figure 11*).

Since the stack is 128 bytes deep, the 9 most significant bits are forced by hardware. Following an MCU Reset, or after a Reset Stack Pointer instruction (RSP), the Stack Pointer contains its reset value (the SP6 to SP0 bits are set) which is the stack higher address.

The least significant byte of the Stack Pointer (called S) can be directly accessed by a LD instruction.

Note: When the lower limit is exceeded, the Stack Pointer wraps around to the stack upper limit, without indicating the stack overflow. The previously stored information is then overwritten and therefore lost. The stack also wraps in case of an underflow.

The stack is used to save the return address during a subroutine call and the CPU context during an interrupt. The user may also directly manipulate the stack by means of the PUSH and POP instructions. In the case of an interrupt, the PCL is stored at the first location

Note: See Section 13: Electrical characteristics for more information on the frequency and accuracy of the RC oscillator.

To improve clock stability and frequency accuracy, it is recommended to place a decoupling capacitor, typically 100nF, between the V_{DD} and V_{SS} pins as close as possible to the ST7 device.

These two bytes are systematically programmed by ST, including on FASTROM devices. Consequently, customers intending to use FASTROM service must not use these two bytes.

RCCR0 and RCCR1 calibration values will be erased if the Read-out protection bit is reset after it has been set. See *Section 4.5.1: Read-out protection*.

Caution: If the voltage or temperature conditions change in the application, the frequency may need to be recalibrated.
Refer to application note AN1324 for information on how to calibrate the RC frequency using an external reference signal.

7.2 Phase locked loop (PLL)

The PLL can be used to multiply a 1 MHz frequency from the RC oscillator or the external clock by 4 or 8 to obtain f_{OSC} of 4 or 8 MHz. The PLL is enabled and the multiplication factor of 4 or 8 is selected by 2 option bits.

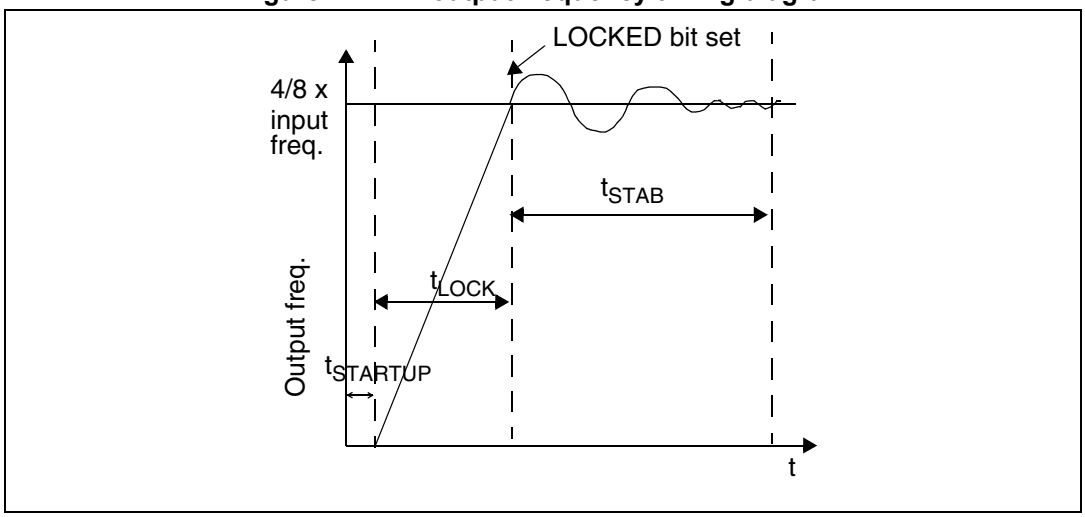
- The x4 PLL is intended for operation with V_{DD} in the 2.4 V to 3.3 V range
- The x8 PLL is intended for operation with V_{DD} in the 3.3 V to 5.5 V range

Note: Refer to Section 15.1: Option bytes for the option byte description.

If the PLL is disabled and the RC oscillator is enabled, then f_{OSC} = 1 MHz.

If both the RC oscillator and the PLL are disabled, f_{OSC} is driven by the external clock.

Figure 12. PLL output frequency timing diagram



When the PLL is started, after reset or wakeup from HALT mode or AWUF mode, it outputs the clock after a delay of $t_{STARTUP}$.

When the PLL output signal reaches the operating frequency, the LOCKED bit in the SICSCR register is set. Full PLL accuracy (ACC_{PLL}) is reached after a stabilization time of t_{STAB} (see *Figure 12* below and *Figure 64: RC oscillator and PLL characteristics (tested*

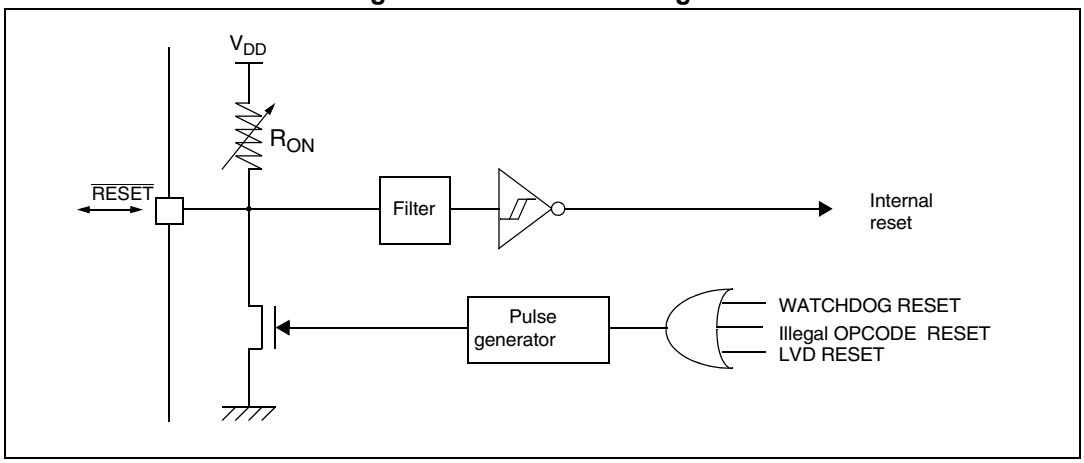
7.5.2 Asynchronous external $\overline{\text{RESET}}$ pin

The $\overline{\text{RESET}}$ pin is both an input and an open-drain output with integrated R_{ON} weak pull-up resistor. This pull-up has no fixed value but varies in accordance with the input voltage. It can be pulled low by external circuitry to reset the device.

Note: See Section 13: Electrical characteristics for more details.

A RESET signal originating from an external source must have a duration of at least $t_{h(RSTL)in}$ in order to be recognized (see *Figure 16: RESET sequences*). This detection is asynchronous and therefore the MCU can enter reset state even in HALT mode.

Figure 15. Reset block diagram



Note: See Section 12.2.1: Illegal opcode reset for more details on illegal opcode reset conditions.

The $\overline{\text{RESET}}$ pin is an asynchronous signal which plays a major role in EMS performance. In a noisy environment, it is recommended to follow the guidelines mentioned in *Section 13: Electrical characteristics*.

7.5.3 External power-on RESET

If the LVD is disabled by option byte, to start up the microcontroller correctly, the user must ensure by means of an external reset circuit that the reset signal is held low until V_{DD} is over the minimum level specified for the selected f_{OSC} frequency.

A proper reset signal for a slow rising V_{DD} supply can generally be provided by an external RC network connected to the $\overline{\text{RESET}}$ pin.

7.5.4 Internal low voltage detector (LVD) RESET

Two different RESET sequences caused by the internal LVD circuitry can be distinguished:

- Power-on RESET
- Voltage drop RESET.

The device $\overline{\text{RESET}}$ pin acts as an output that is pulled low when $V_{DD}<V_{IT+}$ (rising edge) or $V_{DD}<V_{IT-}$ (falling edge) as shown in *Figure 16: RESET sequences*.

The LVD filters spikes on V_{DD} larger than $t_{g(VDD)}$ to avoid parasitic resets.

Note: The LVDRF flag is not cleared when another RESET type occurs (external or watchdog), the LVDRF flag remains set to keep trace of the original failure.
In this case, a watchdog reset can be detected by software while an external reset can not.

Note: Refer to the Section 10.7: Device-specific I/O port configuration for device specific information.

Table 22. I/O port mode options(1)

Configuration mode		Pull-up	P-buffer	Diodes	
				to V_{DD}	to V_{SS}
Input	Floating with/without interrupt	Off	Off	On	On
	Pull-up with/without interrupt	On			
Output	Push-pull	Off	On		
	Open drain (logic level)		Off		
	True open drain	NI	NI	NI(2)	

1. Legend:
NI - not implemented
Off - implemented not activated
On - implemented and activated.

2. The diode to V_{DD} is not implemented in the true open drain pads. A local protection between the pad and V_{OL} is implemented to protect the device against positive stress.

Table 23. I/O configurations

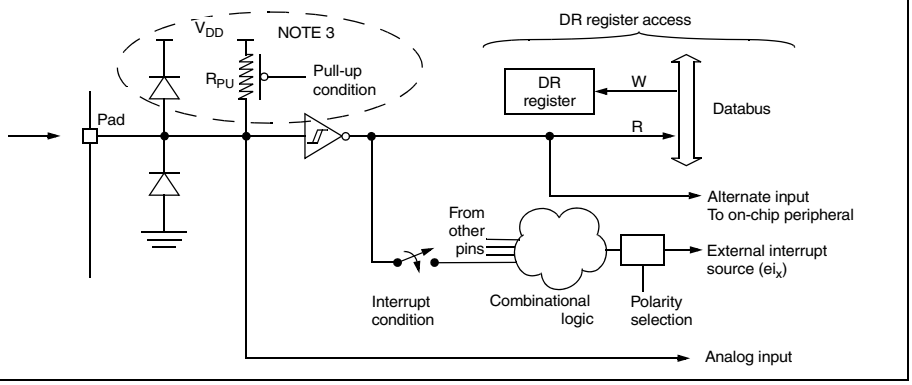
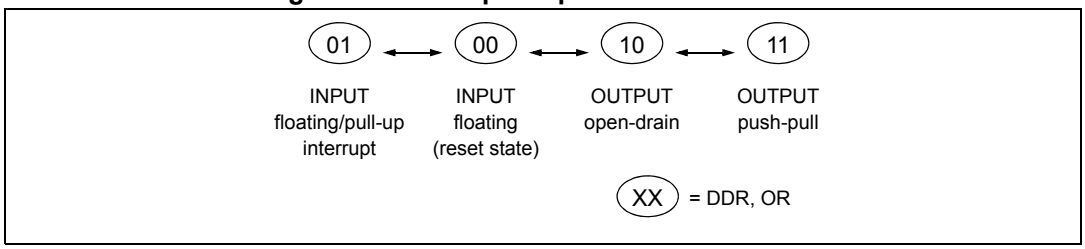
I/O port	Hardware configuration
Input(1)	

Figure 32. Interrupt I/O port state transitions



10.4 Unused I/O pins

Unused I/O pins must be connected to fixed voltage levels. Refer to *Section 13.8: I/O port pin characteristics*.

10.5 Low power modes

Table 24. Effect of low power modes on I/O ports

Mode	Description
WAIT	No effect on I/O ports. External interrupts cause the device to exit from WAIT mode.
HALT	No effect on I/O ports. External interrupts cause the device to exit from HALT mode.

10.6 Interrupts

The external interrupt event generates an interrupt if the corresponding configuration is selected with DDR and OR registers and if the I bit in the CC register is cleared (RIM instruction).

Table 25. I/O port interrupt control/wake-up capability

Interrupt event	Event flag	Enable control bit	Exit from WAIT	Exit from HALT
External interrupt on selected external event	-	DDRx ORx	Yes	Yes

10.7 Device-specific I/O port configuration

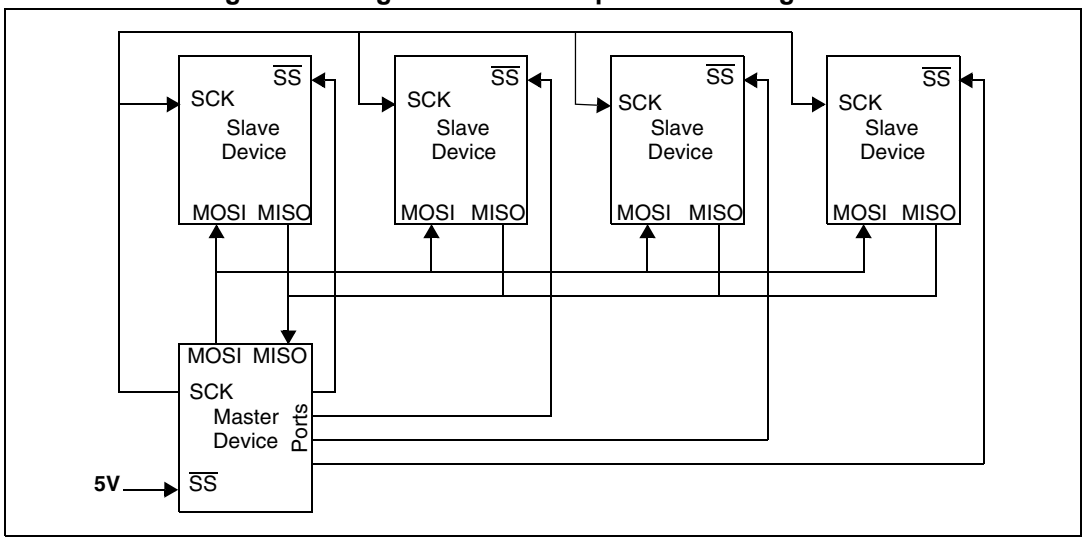
The I/O port register configurations are summarized as follows:

Standard ports

Table 26. Ports PA7:0, PB6:0

Mode	DDR	OR
Floating input	0	0
Pull-up input	0	1

Figure 48. Single master / multiple slave configuration



11.4.6 Low power modes

Table 40. WAIT and HALT mode description

Mode	Description
WAIT	No effect on SPI. SPI interrupt events cause the device to exit from WAIT mode.
HALT	SPI registers are frozen. In HALT mode, the SPI is inactive. SPI operation resumes when the Device is woken up by an interrupt with “exit from HALT mode” capability. The data received is subsequently read from the SPIDR register when the software is running (interrupt vector fetching). If several data are received before the wakeup event, then an overrun error is generated. This error can be detected after the fetch of the interrupt routine that woke up the Device.

Using the SPI to wake up the device from HALT mode

In slave configuration, the SPI is able to wake up the Device from HALT mode through a SPIF interrupt. The data received is subsequently read from the SPIDR register when the software is running (interrupt vector fetch). If multiple data transfers have been performed before software clears the SPIF bit, then the OVR bit is set by hardware.

Note: When waking up from HALT mode, if the SPI remains in Slave mode, it is recommended to perform an extra communications cycle to bring the SPI from HALT mode state to normal state. If the SPI exits from Slave mode, it returns to normal state immediately.

Caution: The SPI can wake up the Device from HALT mode only if the Slave Select signal (external SS pin or the SSI bit in the SPICSR register) is low when the Device enters HALT mode. So if Slave selection is configured as external (see *Slave select management on page 93*), make sure the master drives a low level on the SS pin when the slave enters HALT mode.

11.4.7 Interrupts

Table 41. Interrupt events

Interrupt Event	Event flag	Enable control bit	Exit from WAIT	Exit from HALT
SPI end of transfer event	SPIF	SPIE	Yes	Yes
Master mode fault event	MODF		Yes	No
Overrun error	OVR		Yes	No

Note: The SPI interrupt events are connected to the same interrupt vector (see Section 8: Interrupts). They generate an interrupt if the corresponding Enable Control bit is set and the interrupt mask in the CC register is reset (RIM instruction).

11.4.8 Register description

Control register (SPICR)

Read/Write

Reset Value: 0000 xxxx (0xh)

7							0
SPIE	SPE	SPR2	MSTR	CPOL	CPHA	SPR1	SPR0

- Bit 7 = **SPIE** *Serial peripheral interrupt enable*
  This bit is set and cleared by software.
  0: Interrupt is inhibited
  1: An SPI interrupt is generated whenever an End of Transfer event, Master mode Fault or Overrun error occurs (SPIF=1, MODF=1 or OVR=1 in the SPICSR register).
- Bit 6 = **SPE** *Serial Peripheral Output Enable*
  This bit is set and cleared by software. It is also cleared by hardware when, in master mode, $\overline{SS}$=0 (see *Master mode fault (MODF) on page 96*). The SPE bit is cleared by reset, so the SPI peripheral is not initially connected to the external pins.
  0: I/O pins free for general purpose I/O
  1: SPI I/O pin alternate functions enabled.
- Bit 5 = **SPR2** *Divider enable*
  This bit is set and cleared by software and is cleared by reset. It is used with the SPR[1:0] bits to set the baud rate. Refer to *Table 42: SPI master mode SCK frequency*.
  0: Divider by 2 enabled
  1: Divider by 2 disabled

Note: This bit has no effect in slave mode.

- Bit 4 = **MSTR** *Master mode*
  This bit is set and cleared by software. It is also cleared by hardware when, in master mode, $\overline{SS}$=0 (see *Master mode fault (MODF) on page 96*).
  0: Slave mode

Table 45. Channel selection bits (continued)

Channel pin(1)	CH2	CH1	CH0
AIN3	0	1	1
AIN4	1	0	0
AIN5	1	0	1
AIN6	1	1	0

1. The number of channels is device dependent. Refer to *Table 2: Device pin description*.

Figure 54. RC Osc Freq vs V_{DD} (calibrated with RCCR0: 5V@ 25°C)

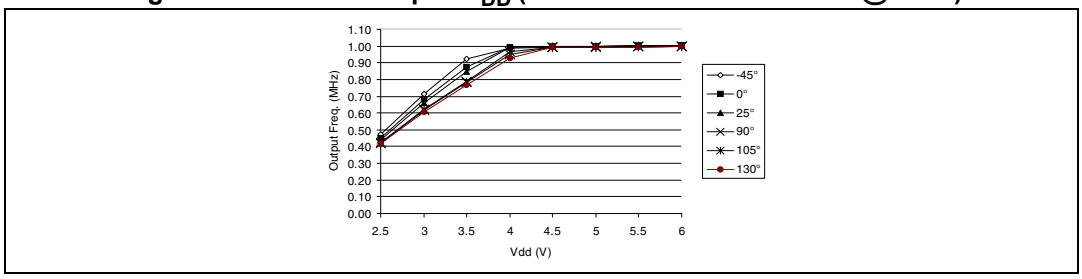


Figure 55. Typical RC oscillator Accuracy vs temperature @ V_{DD}=5V (calibrated with RCCR0: 5V @ 25°C)

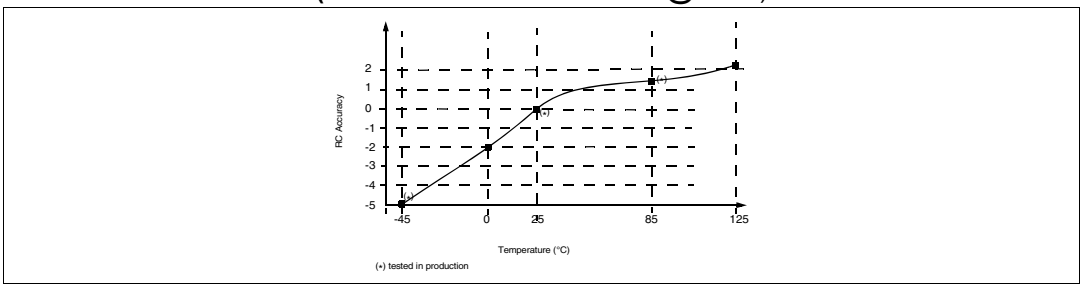


Figure 56. RC Osc Freq vs V_{DD} and RCCR Value

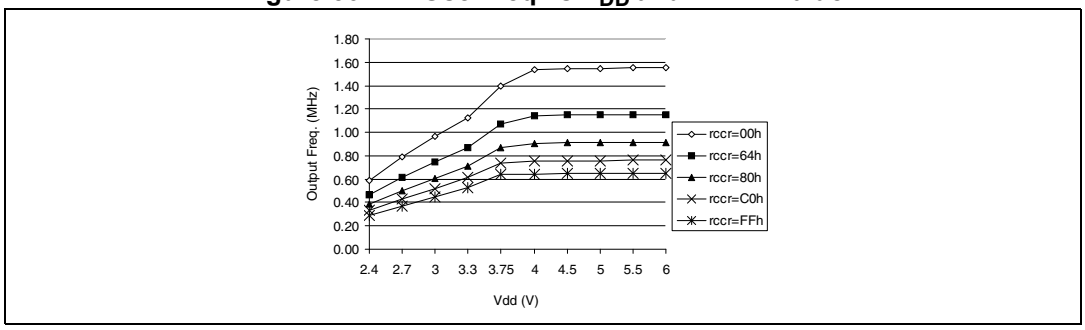


Figure 57. PLL $\Delta f_{CPU}/f_{CPU}$ versus time

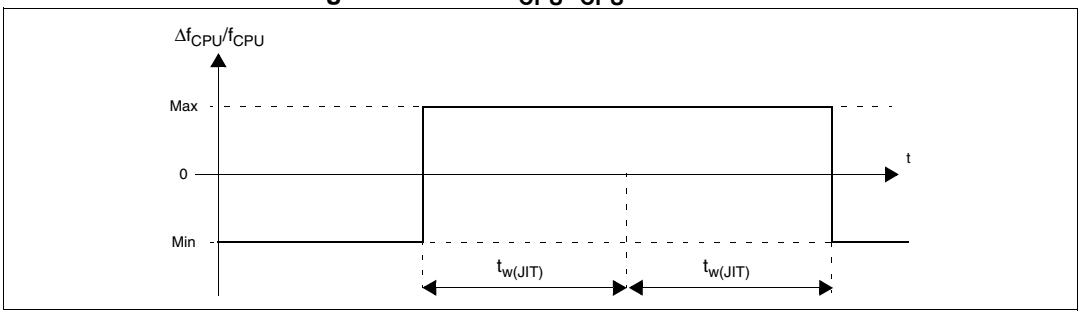
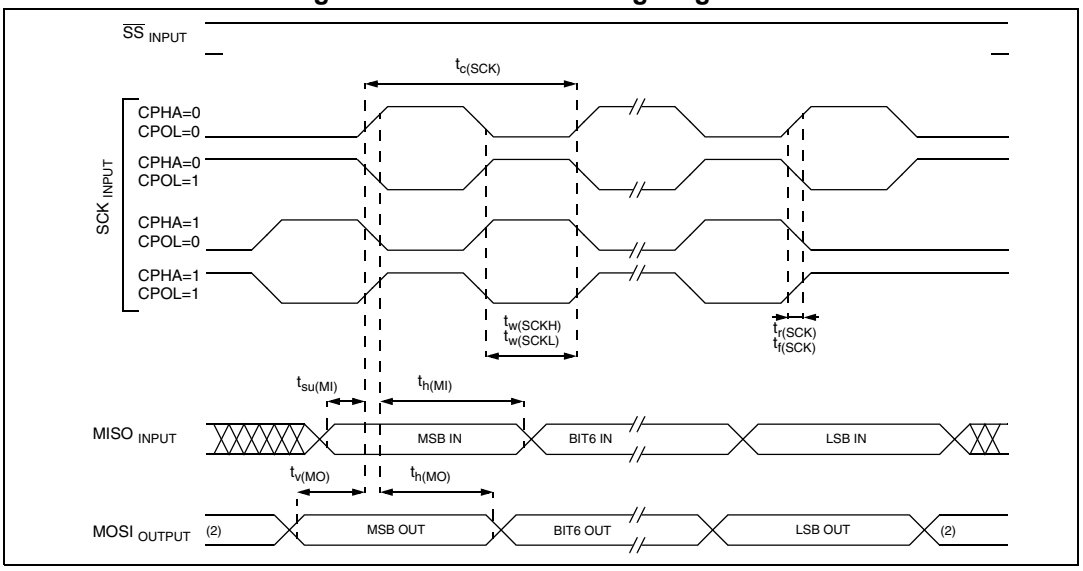


Figure 88. SPI master timing diagram(1)



1. Measurement points are done at CMOS levels: $0.3xV_{DD}$ and $0.7xV_{DD}$.
2. When no communication is on-going the data output line of the SPI (MOSI in master mode, MISO in slave mode) has its alternate function capability released. In this case, the pin status depends on the I/O port configuration.

13.11 10-Bit ADC characteristics

Table 84. 10-bit ADC characteristics(1)

Symbol	Parameter	Conditions	Min	Typ(2)	Max	Unit
f_{ADC}	ADC clock frequency	–	–	–	4	MHz
V_{AIN}	Conversion voltage range(3)	–	V_{SSA}	–	V_{DDA}	V
R_{AIN}	External input resistor	–	–	–	10(4)	kΩ
C_{ADC}	Internal sample and hold capacitor	–	–	6	–	pF
t_{STAB}	Stabilization time after ADC enable	f_{CPU}=8MHz, f_{ADC}=4MHz	0(5)			µs
t_{ADC}	Conversion time (Sample+Hold)		3.5			
	- Sample capacitor loading time - Hold conversion time		4 10			$1/f_{ADC}$
I_{ADC}	Analog Part	–	–	–	1	mA
	Digital Part	–	–	–	0.2	

1. Subject to general operating condition for V_{DD}, f_{OSC}, and T_A unless otherwise specified.
2. Unless otherwise specified, typical data are based on T_A=25°C and V_{DD}-V_{SS}=5V. They are given only as design guidelines and are not tested.
3. When V_{DDA} and V_{SSA} pins are not available on the pinout, the ADC refers to V_{DD} and V_{SS}.
4. Any added external serial resistor will downgrade the ADC accuracy (especially for resistance greater than 10kΩ). Data based on characterization results, not tested in production.

Figure 92. Amplifier noise vs voltage

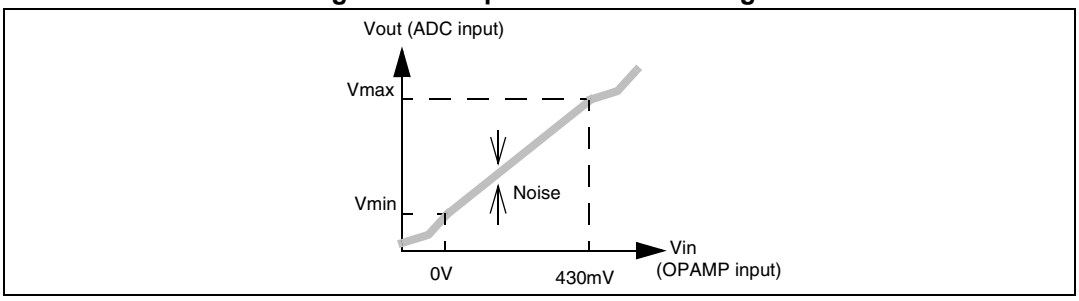


Table 86. ADC characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(AMP)}$	Amplifier operating voltage	–	3.6	–	5.5	V
V_{IN}	Amplifier input voltage(2)	V_{DD}=3.6V	0	–	350	mV
		V_{DD}=5V	0	–	500	
V_{OFFSET}	Amplifier output offset voltage(3)	V_{DD}=5V	–	200	–	mV
V_{STEP}	Step size for monotonicity(4)	V_{DD}=3.6V	3.5	–	–	mV
		V_{DD}=5V	4.89	–	–	
Linearity	Output voltage response	–	Linear			
Gain factor	Amplified analog input gain(5)	–	–	8	–	–
Vmax	Output linearity max voltage	V_{INmax} = 430mV, V_{DD}=5V	–	3.65	3.94	V
Vmin	Output linearity min voltage		–	200	–	mV

1. Data based on characterization results over the whole temperature range, not tested in production.
2. Please refer to the application note AN1830 for details of TE% vs V_{in}.
3. Refer to the offset variation in temperature below.
4. Monotonicity guaranteed if V_{IN} increases or decreases in steps of min. 5mV.
5. For precise conversion results, it is recommended to calibrate the amplifier at the following two points:
–offset at V_{INmin} = 0V
–gain at full scale (for example V_{IN}=430mV).

13.11.1 Amplifier output offset variation

The offset is quite sensitive to temperature variations. In order to ensure a good reliability in measurements, the offset must be recalibrated periodically i.e. during power on or whenever the device is reset depending on the customer application and during temperature variation. *Table 87* gives the typical offset variation over temperature.

Table 87. Typical offset variation over temperature

Typical offset variation (LSB)				Unit
-45	-20	+25	+90	°C
-12	-7	–	+13	LSB

Figure 94. 20-pin plastic dual in-line package, 300-mil width

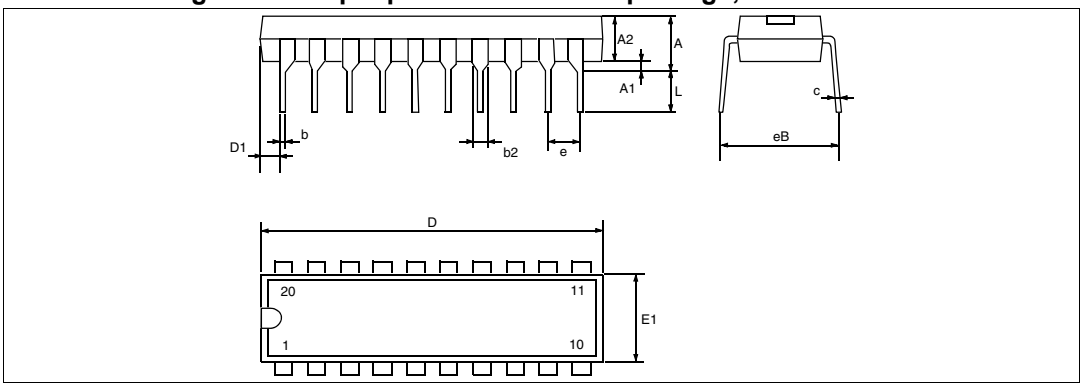


Table 89. Dual in-line package characteristics

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	–	–	5.33	–	–	0.210
A1	0.38	–	–	0.015	–	–
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	24.89	26.16	26.92	0.980	1.030	1.060
D1	0.13	–	–	0.005	–	–
e	–	2.54	–	–	0.100	–
eB	–	–	10.92	–	–	0.430
E1	6.10	6.35	7.11	0.240	0.250	0.280
L	2.92	3.30	3.81	0.115	0.130	0.150
	Number of Pins					
N	20					

Table 101. Revision history (continued)

Date	Revision	Description of changes
25-Jun-2013	5	Added Temperature range in *Features*. Added ST7FLITE29F2M to*Table 97: Supported part numbers* and *Table 98: ST7LITE2 FASTROM microcontroller option list*.
31-Jul-2013	6	Added a second Temperature range in *Features*. Updated the Operating temperature row in *Table 1: Device summary*. Updated the Temp. range column in front of ST7FLITE29F2M in *Table 97: Supported part numbers*.
07-Jan-2014	7	Added note (1) on *Table 88: Small outline package characteristics*