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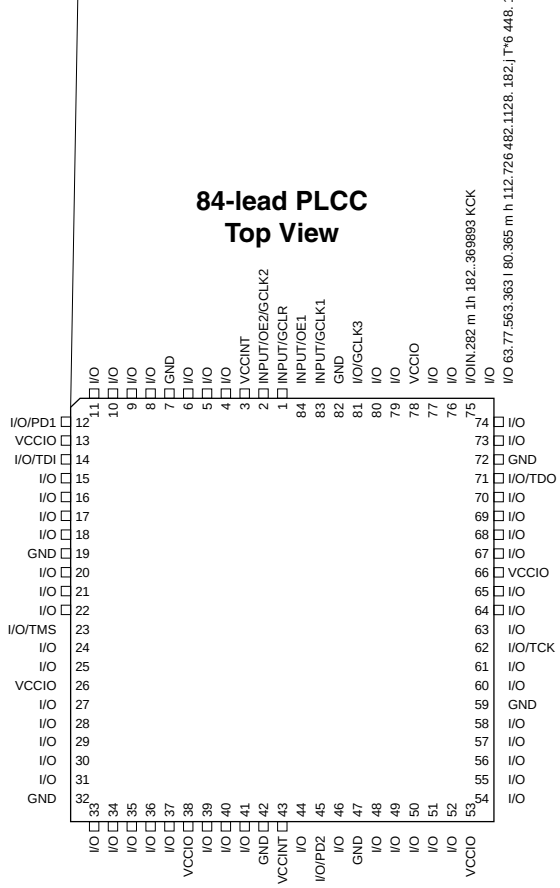
## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

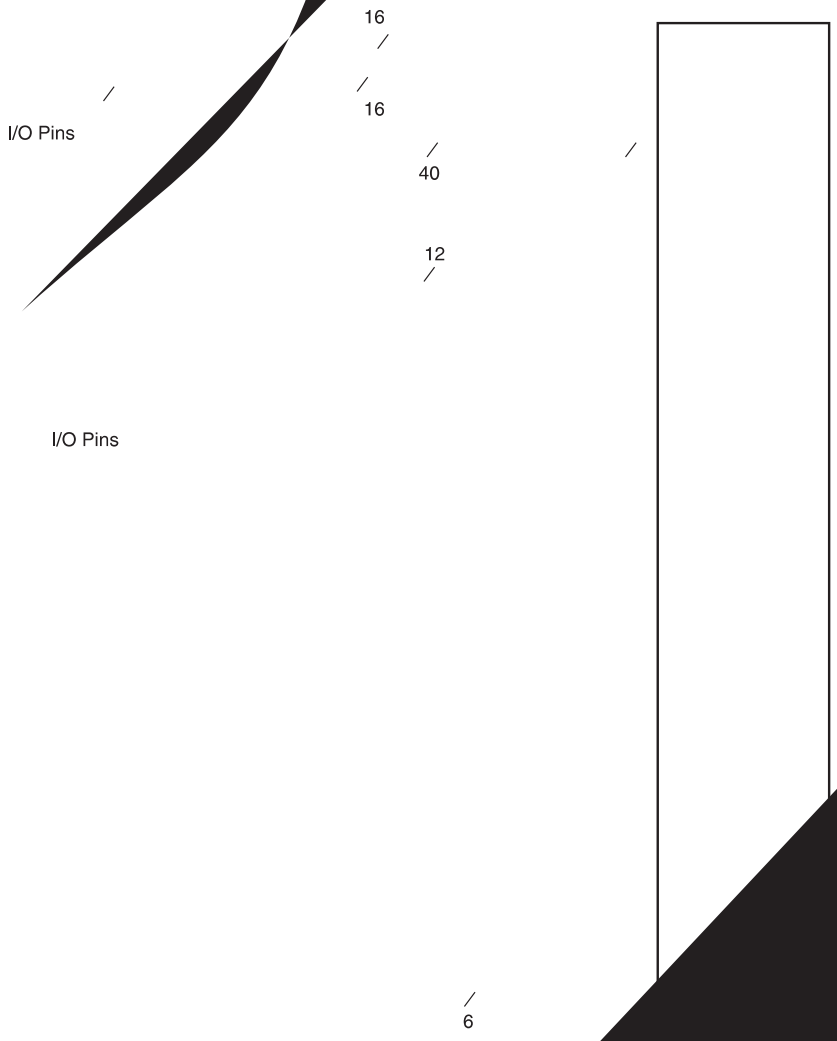
| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable (min 10K program/erase cycles) |
| Delay Time tpd(1) Max | 10 ns |
| Voltage Supply - Internal | 4.5V ~ 5.5V |
| Number of Logic Elements/Blocks | - |
| Number of Macrocells | 128 |
| Number of Gates | - |
| Number of I/O | 80 |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atf1508as-10ai100 |

## 84-lead PLCC
## Top View




## 100-lead TQFP
## Top View

## Block Diagram



## Description

The ATF1508AS is a high-performance, high-density complex programmable logic device (CPLD) that utilizes Atmel's proven electrically-erasable technology. With 128 logic macrocells and up to 100 inputs, it easily integrates logic from several TTL, SSI, MSI, LSI and classic PLDs. The ATF1508AS's enhanced routing switch matrices increase usable gate count and increase odds of successful pin-locked design modifications.

The ATF1508AS has up to 96 bi-directional I/O pins and four dedicated input pins, depending on the type of device package selected. Each dedicated pin can also serve as a global control signal, register clock, register reset or output enable. Each of these control signals can be selected for use individually within each macrocell.

Each of the 128 macrocells generates a buried feedback that goes to the global bus. Each input and I/O pin also feeds into the global bus. The switch matrix in each logic block then selects 40 individual signals from the global bus. Each macrocell also generates a foldback logic term that goes to a regional bus. Cascade logic between macrocells in the ATF1508AS allows fast, efficient generation of complex logic functions. The ATF1508AS contains eight such logic chains, each capable of creating sum term logic with a fan-in of up to 40 product terms.

The ATF1508AS macrocell, shown in Figure 1, is flexible enough to support highly-complex logic functions operating at high speed. The macrocell consists of five sections: product terms and product term select multiplexer; OR/XOR/CASCADE logic, a flip-flop, output select and enable, and logic array inputs.

Unused macrocells are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the contents of the ATF1508AS. Two bytes (16 bits) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the security fuse.

The ATF1508AS device is an in-system programmable (ISP) device. It uses the industry-standard 4-pin JTAG interface (IEEE Std. 1149.1), and is fully compliant with JTAG's Boundary-scan Description Language (BSDL). ISP allows the device to be programmed without removing it from the printed circuit board. In addition to simplifying the manufacturing flow, ISP also allows design modifications to be made in the field via software.

### Product Terms and Select Mux

Each ATF1508AS macrocell has five product terms. Each product term receives as its inputs all signals from both the global bus and regional bus.

The product term select multiplexer (PTMUX) allocates the five product terms as needed to the macrocell logic gates and control signals. The PTMUX programming is determined by the design compiler, which selects the optimum macrocell configuration.

### OR/XOR/ CASCADE Logic

The ATF1508AS's logic structure is designed to efficiently support all types of logic. Within a single macrocell, all the product terms can be routed to the OR gate, creating a 5-input
e opeme(e6c-)e.4.e9hd.6cagicrLogic1.3(o5.)(6cagigic1.3ic1.3.n6c4)n6a0uLu9y3(.3mDEsi2ih.1eiy)1-5

## ATF1508AS I/O Pinouts

| MC | PLB | 84-lead J-lead | 100-lead PQFP | 100-lead TQFP | 160-lead PQFP | MC | PLB | 84-lead J-lead | 100-lead PQFP | 100-lead TQFP | 160-lead PQFP |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | A | – | 4 | 2 | 160 | 33 | C | – | 27 | 25 | 41 |
| 2 | A | – | – | – | – | 34 | C | – | – | – | – |
| 3 | A/ **PD1** | 12 | 3 | 1 | 159 | 35 | C | 31 | 26 | 24 | 33 |
| 4 | A | – | – | – | 158 | 36 | C | – | – | – | 32 |
| 5 | A | 11 | 2 | 100 | 153 | 37 | C | 30 | 25 | 23 | 31 |
| 6 | A | 10 | 1 | 99 | 152 | 38 | C | 29 | 24 | 22 | 30 |
| 7 | A | – | – | – | – | 39 | C | – | – | – | – |
| 8 | A | 9 | 100 | 98 | 151 | 40 | C | 28 | 23 | 21 | 29 |
| 9 | A | – | 99 | 97 | 150 | 41 | C | – | 22 | 20 | 28 |
| 10 | A | – | – | – | – | 42 | C | – | – | – | – |
| 11 | A | 8 | 98 | 96 | 149 | 43 | C | 27 | 21 | 19 | 27 |
| 12 | A | – | – | – | 147 | 44 | C | – | – | – | 25 |
| 13 | A | 6 | 96 | 94 | 146 | 45 | C | 25 | 19 | 17 | 24 |
| 14 | A | 5 | 95 | 93 | 145 | 46 | C | 24 | 18 | 16 | 23 |
| 15 | A | – | – | – | – | 47 | C | – | – | – | – |
| 16 | A | 4 | 94 | 92 | 144 | 48 | C/ **TMS** | 23 | 17 | 15 | 22 |
| 17 | B | 22 | 16 | 14 | 21 | 49 | D | 41 | 39 | 37 | 59 |
| 18 | B | – | – | – | – | 50 | D | – | – | – | – |
| 19 | B | 21 | 15 | 13 | 20 | 51 | D | 40 | 38 | 36 | 58 |
| 20 | B | – | – | – | 19 | 52 | D | – | – | – | 57 |
| 21 | B | 20 | 14 | 12 | 18 | 53 | D | 39 | 37 | 35 | 56 |
| 22 | B | – | 12 | 10 | 16 | 54 | D | – | 35 | 33 | 54 |
| 23 | B | – | – | – | – | 55 | D | – | – | – | – |
| 24 | B | 18 | 11 | 9 | 15 | 56 | D | 37 | 34 | 32 | 53 |
| 25 | B | 17 | 10 | 8 | 14 | 57 | D | 36 | 33 | 31 | 52 |
| 26 | B | – | – | – | – | 58 | D | – | – | – | – |
| 27 | B | 16 | 9 | 7 | 13 | 59 | D | 35 | 32 | 30 | 51 |
| 28 | B | – | – | – | 12 | 60 | D | – | – | – | 50 |
| 29 | B | 15 | 8 | 6 | 11 | 61 | D | 34 | 31 | 29 | 49 |
| 30 | B | – | 7 | 5 | 10 | 62 | D | – | 30 | 28 | 48 |
| 31 | B | – | – | – | – | 63 | D | – | – | – | – |
| 32 | B/ **TDI** | 14 | 6 | 4 | 9 | 64 | D | 33 | 29 | 27 | 43 |
| 65 | E | 44 | 42 | 40 | 62 | 97 | G | 63 | 65 | 63 | 100 |

## ATF1508ASL Standard Package Options

| $t_{PD}$ (ns) | $t_{CO1}$ (ns) | $f_{MAX}$ (MHz) | Ordering Code | Package | Operation Range |
|---|---|---|---|---|---|
| 20 | 12 | 83.3 | ATF1508ASL-20 JC84 | 84J | Commercial (0°C to 70°C) |
| | | | ATF1508ASL-20 QC100 | 100Q1 | |
| | | | ATF1508ASL-20 AC100 | 100A | |
| | | | ATF1508ASL-20 QC160 | 160Q1 | |
| 25 | 15 | 70 | ATF1508ASL-25 JI84 | 84J | Industrial (-40°C to +85°C) |
| | | | ATF1508ASL-25 QI100 | 100Q1 | |
| | | | ATF1508ASL-25 AI100 | 100A | |
| | | | ATF1508ASL-25 QI160 | 160Q1 | |

Note: 1. The last time buy is Sept. 30, 2005 for shaded parts.

## Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

## ATF1508ASL Green Package Options (Pb/Halide-free/RoHS Compliant)

| $t_{PD}$ (ns) | $t_{CO1}$ (ns) | $f_{MAX}$ (MHz) | Ordering Code | Package | Operation Range |
|---|---|---|---|---|---|
| 25 | 15 | 70 | ATF1508ASL-25 JU84 | 84J | Industrial (-40°C to +85°C) |
| | | | ATF1508ASL-25 AU100 | 100A | |

| Package Type | |
|---|---|
| **84J** | 84-lead, Plastic J-leaded Chip Carrier (PLCC) |
| **100Q1** | 100-lead, Plastic Quad Pin Flat Package (PQFP) |
| **100A** | 100-lead, Very Thin Plastic Gull Wing Quad Flat Package (TQFP) |
| **160Q1** | 160-lead, Plastic Quad Pin Flat Package (PQFP) |