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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.
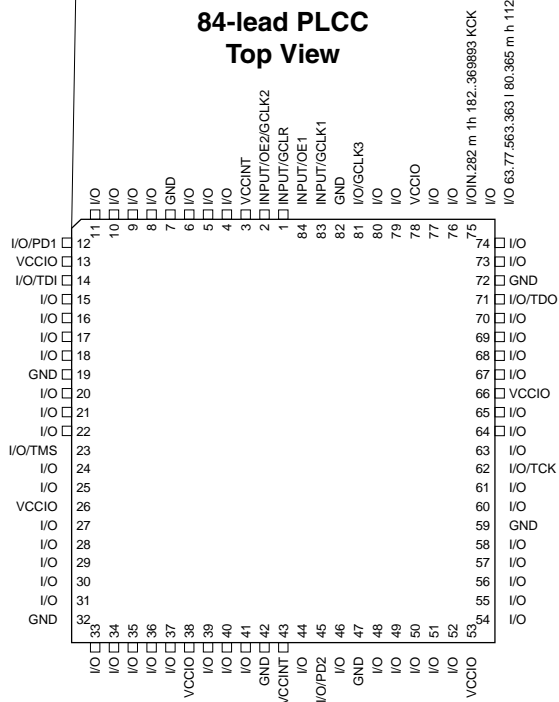
Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable (min 10K program/erase cycles)
Delay Time tpd(1) Max	15 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	64
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atf1508as-15ji84

84-lead PLCC
Top View

Left side (top to bottom):
I/O/PD1 12
VCCIO 13
I/O/TDI 14
I/O 15
I/O 16
I/O 17
I/O 18
GND 19
I/O 20
I/O 21
I/O 22
I/O/TMS 23
I/O 24
I/O 25
VCCIO 26
I/O 27
I/O 28
I/O 29
I/O 30
I/O 31
GND 32

Top side (pins 11 down to 75):
I/O 11
I/O 10
I/O 9
I/O 8
GND 7
I/O 6
I/O 5
I/O 4
VCCINT 3
INPUT/OE2/GCLK2 2
INPUT/GCLR 1
INPUT/OE1 84
INPUT/GCLK1 83
GND 82
I/O/GCLK3 81
I/O 80
I/O 79
VCCIO 78
I/O 77
I/O 76
I/O 75

Right side (top to bottom):
74 I/O
73 I/O
72 GND
71 I/O/TDO
70 I/O
69 I/O
68 I/O
67 I/O
66 VCCIO
65 I/O
64 I/O
63 I/O
62 I/O/TCK
61 I/O
60 I/O
59 GND
58 I/O
57 I/O
56 I/O
55 I/O
54 I/O

Bottom side (pins 33 through 53):
I/O 33
I/O 34
I/O 35
I/O 36
I/O 37
VCCIO 38
I/O 39
I/O 40
I/O 41
GND 42
VCCINT 43
I/O/PD2 44
I/O 45
I/O 46
GND 47
I/O 48
I/O 49
I/O 50
I/O 51
I/O 52
VCCIO 53

100-lead TQFP
Top View

Description

The ATF1508AS is a high-performance, high-density complex programmable logic device (CPLD) that utilizes Atmel's proven electrically-erasable technology. With 128 logic macrocells and up to 100 inputs, it easily integrates logic from several TTL, SSI, MSI, LSI and classic PLDs. The ATF1508AS's enhanced routing switch matrices increase usable gate count and increase odds of successful pin-locked design modifications.

The ATF1508AS has up to 96 bi-directional I/O pins and four dedicated input pins, depending on the type of device package selected. Each dedicated pin can also serve as a global control signal, register clock, register reset or output enable. Each of these control signals can be selected for use individually within each macrocell.

Each of the 128 macrocells generates a buried feedback that goes to the global bus. Each input and I/O pin also feeds into the global bus. The switch matrix in each logic block then selects 40 individual signals from the global bus. Each macrocell also generates a foldback logic term that goes to a regional bus. Cascade logic between macrocells in the ATF1508AS allows fast, efficient generation of complex logic functions. The ATF1508AS contains eight such logic chains, each capable of creating sum term logic with a fan-in of up to 40 product terms.

The ATF1508AS macrocell, shown in Figure 1, is flexible enough to support highly-complex logic functions operating at high speed. The macrocell consists of five sections: product terms and product term select multiplexer; OR/XOR/CASCADE logic, a flip-flop, output select and enable, and logic array inputs.

Unused macrocells are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the contents of the ATF1508AS. Two bytes (16 bits) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the security fuse.

The ATF1508AS device is an in-system programmable (ISP) device. It uses the industry-standard 4-pin JTAG interface (IEEE Std. 1149.1), and is fully compliant with JTAG's Boundary-scan Description Language (BSDL). ISP allows the device to be programmed without removing it from the printed circuit board. In addition to simplifying the manufacturing flow, ISP also allows design modifications to be made in the field via software.

Product Terms and Select Mux

Each ATF1508AS macrocell has five product terms. Each product term receives as its inputs all signals from both the global bus and regional bus.

The product term select multiplexer (PTMUX) allocates the five product terms as needed to the macrocell logic gates and control signals. The PTMUX programming is determined by the design compiler, which selects the optimum macrocell configuration.
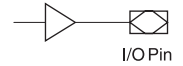
OR/XOR/ CASCADE Logic

The ATF1508AS's logic structure is designed to efficiently support all types of logic. Within a single macrocell, all the product terms can be routed to the OR gate, creating a 5-input
e opeme(e6c-)e.4.e9hd.6cagicrLogic1.3(o5.)(6cagigic1.3ic1.3.n6c4)n6a0uLu9y3(.3mDEsi2ih.1eiy)1-5

Figure 1. ATF1508AS Macrocell

SWITCH REGIONAL
F

D/T/L

I/O Pin

SLEW
RATE

OPEN COLLECTOR
OPTION

MACROCELL REDUCED POWER BIT

Programmable Pin-keeper Option for Inputs and I/Os

The ATF1508AS offers the option of programming all input and I/O pins so that "pin-keeper" circuits can be utilized. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high- or low-level. This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

Input Diagram

Speed/Power Management

The ATF1508AS has several built-in speed and power management features. The ATF1508AS contains circuitry that automatically puts the device into a low-power stand-by mode when no logic transitions are occurring. This not only reduces power consumption during inactive periods, but also provides proportional power-savings for most applications running at system speeds below 5 MHz.

To further reduce power, each ATF1508AS macrocell has a Reduced-power bit feature. This feature allows individual macrocells to be configured for maximum power savings. This feature may be selected as a design option.

I/O Diagram
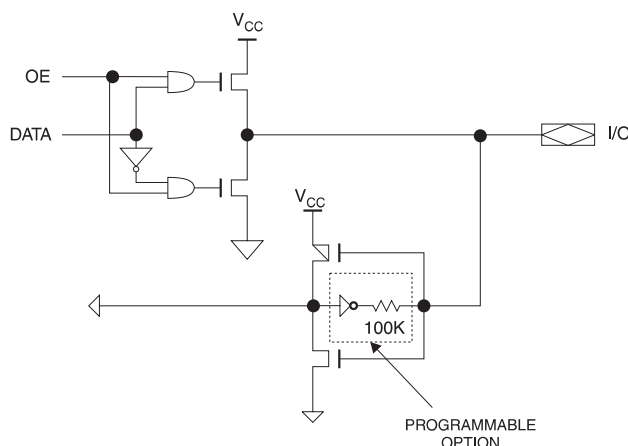
All ATF1508 also have an optional power-down mode. In this mode, current drops to below 10 mA. When the power-down option is selected, either PD1 or PD2 pins (or both) can be used to power down the part. The power-down option is selected in the design source file. When enabled, the device goes into power-down when either PD1 or PD2 is high. In the power-down mode, all internal logic signals are latched and held, as are any enabled outputs.

All pin transitions are ignored until the PD pin is brought low. When the power-down feature is enabled, the PD1 or PD2 pin cannot be used as a logic input or output. However, the pin's macrocell may still be used to generate buried foldback and cascade logic signals.

All power-down AC characteristic parameters are computed from external input or I/O pins, with Reduced-power Bit turned on. For macrocells in reduced-power mode (Reduced-power bit turned on), the reduced-power adder, tRPA, must be added to the AC parameters, which include the data paths t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{ACH} and t_{SEXP}.

Each output also has individual slew rate control. This may be used to reduce system noise by slowing down outputs that do not need to operate at maximum speed. Outputs default to slow switching, and may be specified as fast switching in the design file.

ISP Programming Protection

The ATF1508AS has a special feature that locks the device and prevents the inputs and I/O from driving if the programming process is interrupted for any reason. The inputs and I/O default to high-Z state during such a condition. In addition the pin-keeper option preserves the former state during device programming.

All ATF1508AS devices are initially shipped in the erased state thereby making them ready to use for ISP.

Note: For more information refer to the "Designing for In-System Programmability with Atmel CPLDs" application note.

JTAG-BST Overview

The JTAG boundary-scan testing is controlled by the Test Access Port (TAP) controller in the ATF1508AS. The boundary-scan technique involves the inclusion of a shift-register stage (contained in a boundary-scan cell) adjacent to each component so that signals at component boundaries can be controlled and observed using scan testing principles. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary-scan testing. The ATF1508AS does not currently include a Test Reset (TRST) input pin because the TAP controller is automatically reset at power-up. The six JTAG BST modes supported include: SAMPLE/PRELOAD, EXTEST, BYPASS and IDCODE. BST on the ATF1508AS is implemented using the Boundary-scan Definition Language (BSDL) described in the JTAG specification (IEEE Standard 1149.1). Any third-party tool that supports the BSDL format can be used to perform BST on the ATF1508AS.

The ATF1508AS also has the option of using four JTAG-standard I/O pins for In-System programming (ISP). The ATF1508AS is programmable through the four JTAG pins using programming compatible with the IEEE JTAG Standard 1149.1. Programming is performed by using 5V TTL-level programming signals from the JTAG ISP interface. The JTAG feature is a programmable option. If JTAG (BST or ISP) is not needed, then the four JTAG control pins are available as I/O pins.

JTAG Boundary-scan Cell (BSC) Testing

The ATF1508AS contains up to 96 I/O pins and four input pins, depending on the device type and package type selected. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary-scan testing as described in detail by IEEE Standard 1149.1. A typical BSC consists of three capture registers or scan registers and up to two update registers. There are two types of BSCs, one for input or I/O pin, and one for the macrocells. The BSCs in the device are chained together through the (BST) capture registers. Input to the capture register chain is fed in from the TDI pin while the output is directed to the TDO pin. Capture registers are used to capture active device data signals, to shift data in and out of the device and to load data into the update registers. Control signals are generated internally by the JTAG TAP controller. The BSC configuration for the input and I/O pins and macrocells are shown below.

BSC Configuration Pins and Macrocells (Except JTAG TAP Pins)

Dedic

To Internal

D   TDO

TDI
(From Next Register)

Note: The ATF1508AS has a pull-up option on TMS and TDI pins. This feature is selected as a design option.

## BSC Configuration for Macrocell

Boundary Scan Definition Language (BSDL) Models for the ATF1508

These are now available in all package types via the Atmel Web Site. These models can be used for Boundary-scan Test Operation in the ATF1508AS and have been scheduled to conform to the IEEE 1149.1 standard.

PCI Compliance   The ATF1508AS also supports the growing need in the industry to support the new Peripheral
Component Interconnect (PCI) interface standard in PCI-based designs and specifications.
The PCI interface calls for high current drivers, which are much larger than the traditional TTL
drivers.

PCI Voltage-to-current Curves for +5V Signaling in Pull-up Mode
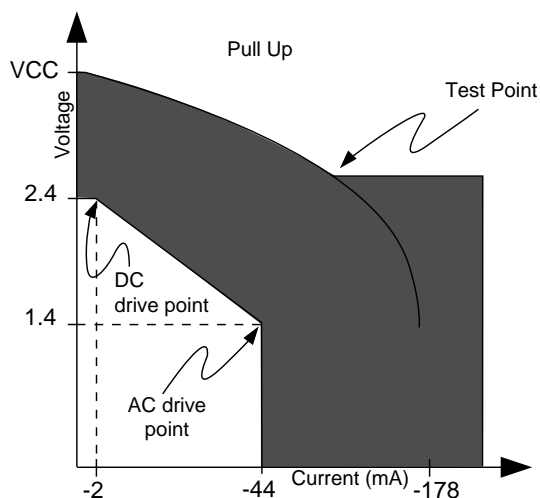
PCI Voltage-to-current Curves for +5V Signaling in Pull-down Mode
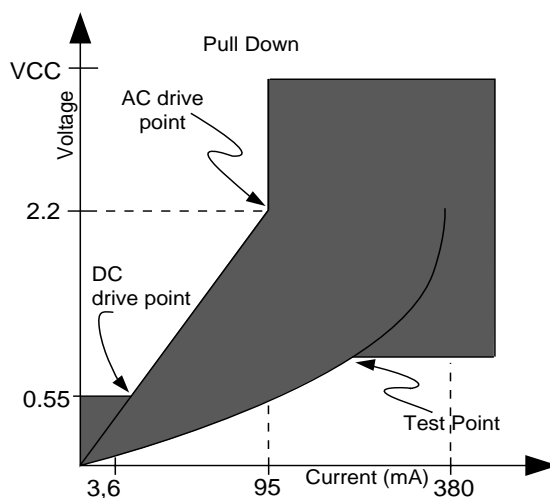
PCI DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Supply Voltage		4.75	5.25	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage		-0.5	0.8	V
I_{IH}	Input High Leakage Current[1]	V_{IN} = 2.7V		70	µA
I_{IL}	Input Low Leakage Current[1]	V_{IN} = 0.5V		-70	µA
V_{OH}	Output High Voltage	I_{OUT} = -2 mA	2.4		V
V_{OL}	Output Low Voltage	I_{OUT} = 3 mA, 6 mA		0.55	V
C_{IN}	Input Pin Capacitance			10	pF
C_{CLK}	CLK Pin Capacitance			12	pF
C_{IDSEL}	IDSEL Pin Capacitance			8	pF
L_{PIN}	Pin Inductance			20	nH

Note: 1. Leakage current is without pin-keeper off.

PCI AC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
$I_{OH(AC)}$	Switching	$0 < V_{OUT} \leq 1.4$	-44		mA
	Current High	$1.4 < V_{OUT} < 2.4$	$-44 + (V_{OUT} - 1.4)/0.024$		mA
		$3.1 < V_{OUT} < V_{CC}$		Equation A[1]	mA

Notes: 1. Equation A: I_{OH} = 11.9 (V_{OUT} - 5.25) * (V_{OUT} + 2.45) for $V_{CC} > V_{OUT} > 3.1V$.
          2. Equation B: I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT}) for $0V < V_{OUT} < 0.71V$.

Power-down Mode

The ATF1508AS includes two pins for optional pin-controlled power-down feature. When this mode is enabled, the PD pin acts as the power-down pin. When the PD1 and PD2 pin is high, the device supply current is reduced to less than 10 mA. During power-down, all output data and internal logic states are latched and held. Therefore, all registered and combinatorial output data remain valid. Any outputs that were in a high-Z state at the onset will remain at high-Z. During power-down, all input signals except the power-down pin are blocked. Input and I/O hold latches remain active to ensure that pins do not float to indeterminate levels, further reducing system power. The power-down pin feature is enabled in the logic design file. Designs using either power-down pin may not use the PD pin logic array input. However, buried logic resources in this macrocell may still be used.

Power-down AC Characteristics[1][2]

Symbol	Parameter	-7 Min	-7 Max	-10 Min	-10 Max	-15 Min	-15 Max	-20 Min	-20 Max	-25 Min	-25 Max	Units
t_{IVDH}	Valid I, I/O before PD High	7		10		15		20		25		ns
t_{GVDH}	Valid OE[2] before PD High	7		10		15		20		25		ns
t_{CVDH}	Valid Clock[2] before PD High	7		10		15		20		25		ns
t_{DHIX}	I, I/O Don't Care after PD High		12		15		25		30		35	ns
t_{DHGX}	OE[2] Don't Care after PD High		12		15		25		30		35	ns
t_{DHCX}	Clock[2] Don't Care after PD High		12		15		25		30		35	ns
t_{DLIV}	PD Low to Valid I, I/O		1		1		1		1		1	µs
t_{DLGV}	PD Low to Valid OE (Pin or Term)		1		1		1		1		1	µs
t_{DLCV}	PD Low to Valid Clock (Pin or Term)		1		1		1		1		1	µs
t_{DLOV}	PD Low to Valid Output		1		1		1		1		1	µs

Notes: 1. For slow slew outputs, add t_{SSO}.
2. Pin or product term.

Absolute Maximum Ratings*

Temperature Under Bias .... -40°C to +85°C

Storage Temperature .... -65°C to +150°C

Voltage on Any Pin with
Respect to Ground ....-2.0V to +7.0V[1]

Voltage on Input Pins
with Respect to Ground
During Programming.....................................-2.0V to +14.0V[1]

Programming Voltage with
Respect to Ground ....-2.0V to +14.0V[1]

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to 7.0V for pulses of less than 20 ns.

DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Ambient)	0°C - 70°C	-40°C - 85°C
V_{CCINT} or V_{CCIO} (5V) Power Supply	5V ± 5%	5V ± 10%
V_{CCIO} (3.3V) Power Supply	2.7V - 3.6V	2.7V - 3.6V

DC Characteristics[1]

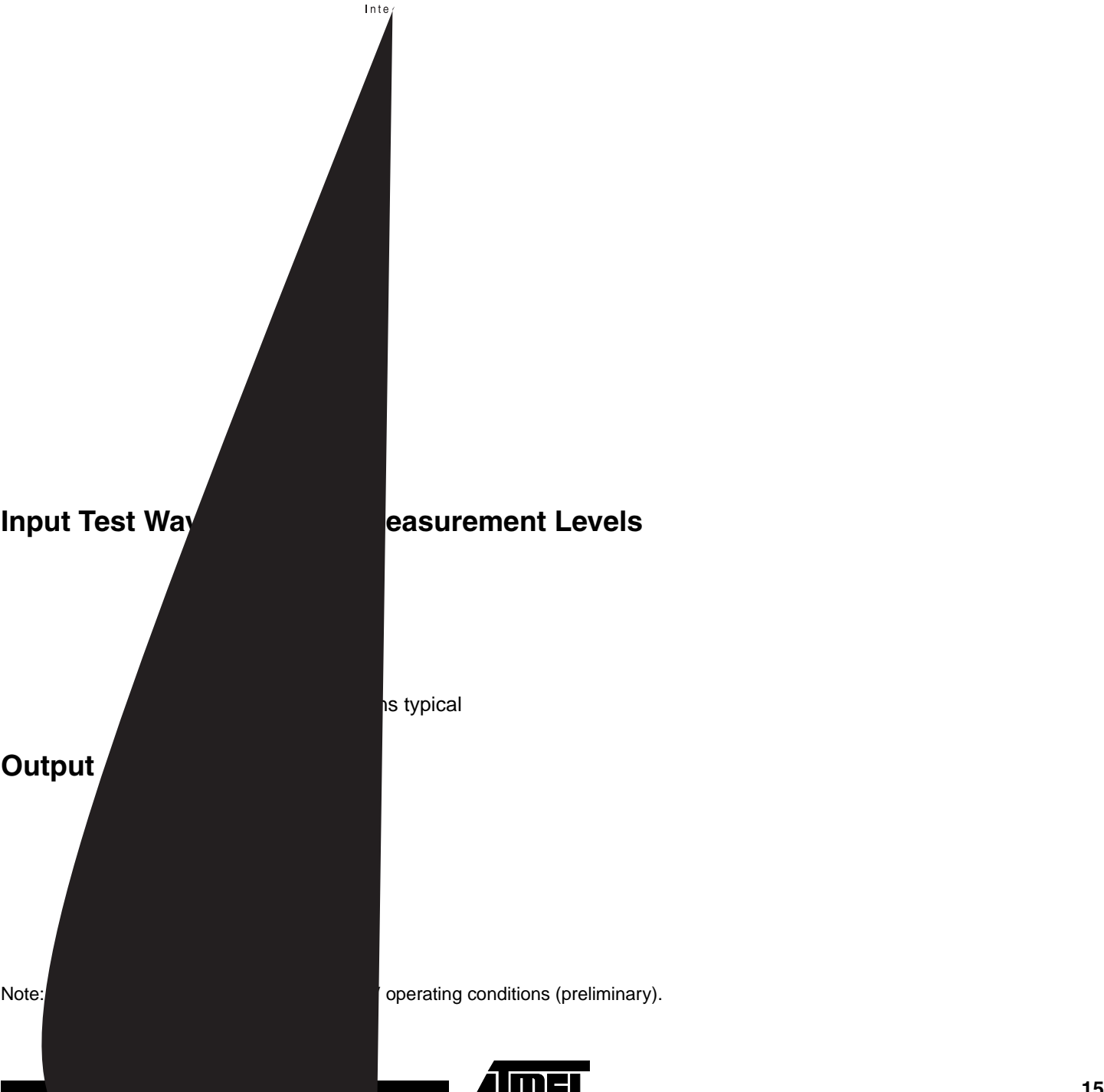| Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$V_{IN} = V_{CC}$				-2	-10	µA
I_{IH}	Input or I/O High Leakage Current					2	10	µA
I_{OZ}	Tri-state Output Off-state Current	$V_O = V_{CC}$ or GND			-40		40	µA
I_{CC1}	Power Supply Current, Standby	$V_{CC} = Max$ $V_{IN} = 0, V_{CC}$	Std Mode	Com.		160		mA
				Ind.		180		mA
			"L" Mode	Com.		10		µA
				Ind.		10		µA
I_{CC2}	Power Supply Current, Power-down Mode	$V_{CC} = Max$ $V_{IN} = 0, V_{CC}$	"PD" Mode			1	10	mA
I_{CC3}[2]	Reduced-power Mode Supply Current	$V_{CC} = Max$ $V_{IN} = 0, V_{CC}$	Std Mode	Com.		65		mA
				Ind.		85		mA
V_{CCIO}	Supply Voltage	5.0V Device Output		Com.	4.75		5.25	V
				Ind.	4.5		5.5	V
V_{CCIO}	Supply Voltage	3.3V Device Output			3.0		3.6	V
V_{IL}	Input Low Voltage				-0.3		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CCIO} + 0.3	V
V_{OL}	Output Low Voltage (TTL)	$V_{IN} = V_{IH}$ or V_{IL} $V_{CCIO} = MIN, I_{OL} = 12$ mA		Com.			0.45	V
				Ind.			0.45	V
	Output Low Voltage (CMOS)	$V_{IN} = V_{IH}$ or V_{IL} $V_{CC} = MIN, I_{OL} = 0.1$ mA		Com.			0.2	V
				Ind.			0.2	V
V_{OH}	Output High Voltage (TTL)	$V_{IN} = V_{IH}$ or V_{IL} $V_{CCIO} = MIN, I_{OH} = -4.0$ mA			2.4			V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. I_{CC3} refers to the current in the reduced-power mode when macrocell reduced-power is turned ON.
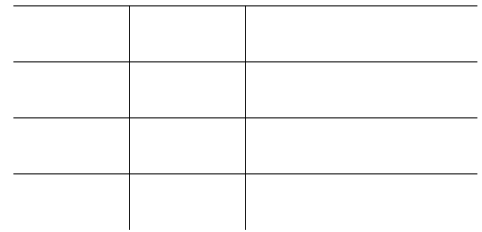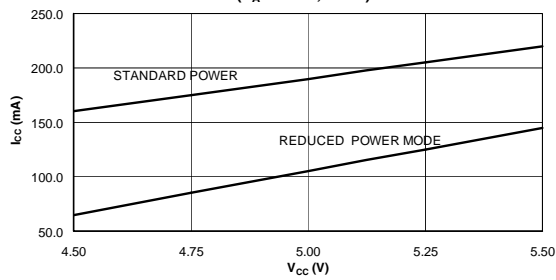
Pin Capacitance[1]

	Typ	Max	Units	Conditions
C_{IN}	8	10	pF	$V_{IN} = 0V; f = 1.0$ MHz
$C_{I/O}$	8	10	pF	$V_{OUT} = 0V; f = 1.0$ MHz

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested. The OGI pin (high-voltage pin during programming) has a maximum capacitance of 12 pF.

Timing Model

Inte

Input Test Wav   easurement Levels

ns typical

Output

Note: operating conditions (preliminary).

SUPPLY CURRENT VS. SUPPLY VOLTAGE
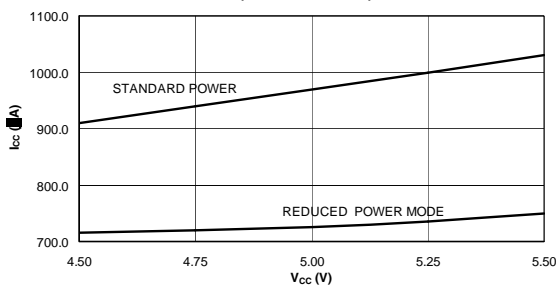**($T_A = 25°C$, F = 0)**

SUPPLY CURRENT VS. SUPPLY VOLTAGE
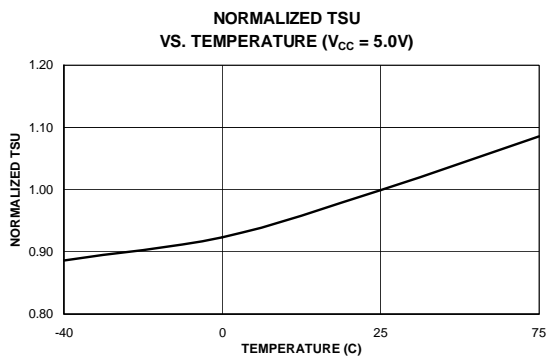**LOW-POWER ("L") VERSION**
($T_A = 25°C$, F = 0)
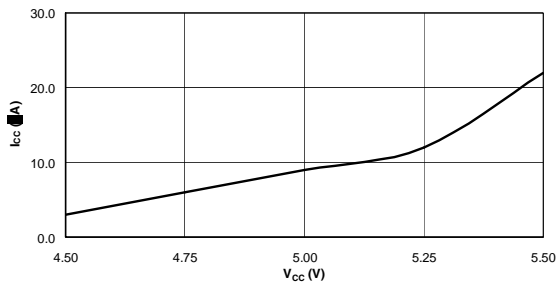
SUPPLY CURRENT VS. FREQUENCY
STANDARD POWER
($T_A = 25°C$, F = 0)
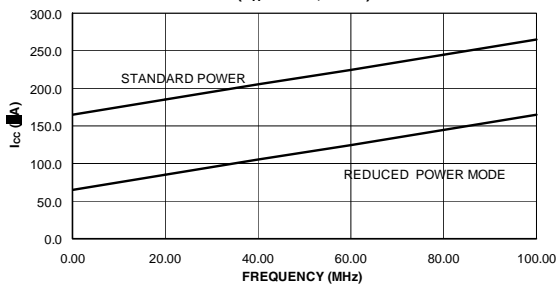
SUPPLY CURRENT VS. SUPPLY VOLTAGE
PIN-CONTROLLED POWER-DOWN MODE
($T_A = 25°C$, F = 0)

**NORMALIZED TSU
VS. TEMPERATURE (V$_{CC}$ = 5.0V)**

AC Characteristics [1]

Symbol	Parameter	-7 Min	-7 Max	-10 Min	-10 Max	-15 Min	-15 Max	-20 Min	-20 Max	-25 Min	-25 Max	Units
t_{PD1}	Input or Feedback to Non-registered Output		7.5		10	3	15		20		25	ns
t_{PD2}	I/O Input or Feedback to Non-registered Feedback		7		9	3	12		16		20	ns
t_{SU}	Global Clock Setup Time	6		7		11		16		20		ns
t_H	Global Clock Hold Time	0		0		0		0		0		ns
t_{FSU}	Global Clock Setup Time of Fast Input	3		3		3		3		3		ns
t_{FH}	Global Clock Hold Time of Fast Input	0.5		0.5		1.0		1.5		2		MHz
t_{COP}	Global Clock to Output Delay		4.5		5		8		10		13	ns
t_{CH}	Global Clock High Time	3		4		5		6		7		ns
t_{CL}	Global Clock Low Time	3		4		5		6		7		ns
t_{ASU}	Array Clock Setup Time	3		3		4		4		5		ns
t_{AH}	Array Clock Hold Time	2		3		4		5		6		ns
t_{ACOP}	Array Clock Output Delay		7.5		10		15		20		25	ns
t_{ACH}	Array Clock High Time	3		4		6		8		10		ns
t_{ACL}	Array Clock Low Time	3		4		6		8		10		ns
t_{CNT}	Minimum Clock Global Period		8		10		13		17		22	ns
f_{CNT}	Maximum Internal Global Clock Frequency	125		100		76.9		66		50		MHz
t_{ACNT}	Minimum Array Clock Period		8		10		13		17		22	ns
f_{ACNT}	Maximum Internal Array Clock Frequency	125		100		76.9		66		50		MHz
f_{MAX}	Maximum Clock Frequency	166.7		125		100		41.7		33.3		MHz
t_{IN}	Input Pad and Buffer Delay		0.5		0.5		2		2		2	ns
t_{IO}	I/O Input Pad and Buffer Delay		0.5		0.5		2		2		2	ns
t_{FIN}	Fast Input Delay		1		1		2		2		2	ns
t_{SEXP}	Foldback Term Delay		4		5		8		10		12	ns
t_{PEXP}	Cascade Logic Delay		0.8		0.8		1		1		1.2	ns
t_{LAD}	Logic Array Delay		3		5		6		7		8	ns
t_{LAC}	Logic Control Delay		3		5		6		7		8	ns
t_{IOE}	Internal Output Enable Delay		2		2		3		3		4	ns
t_{OD1}	Output Buffer and Pad Delay											

ATF1508AS Dedicated Pinouts

Dedicated Pin	84-lead J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP
INPUT/OE2/GCLK2	2	92	90	142
INPUT/GCLR	1	91	89	141
INPUT/OE1	84	90	88	140
INPUT/GCLK1	83	89	87	139
I/O /GCLK3	81	87	85	137
I/O / PD (1, 2)	12,45	3,43	1,41	63,159
I/O / TDI(JTAG)	14	6	4	9
I/O / TMS(JTAG)	23	17	15	22
I/O / TCK(JTAG)	62	64	62	99
I/O / TDO(JTAG)	71	75	73	112
GND	7,19,32,42, 47,59,72,82	13,28,40,45, 61,76,88,97	11,26,38,43, 59,74,86,95	17,42,60,66,95, 113,138,148
VCCINT	3,43	41,93	39,91	61,143
VCCIO	13,26,38, 53,66,78	5,20,36,53,68,84	3,18,34,51,66,82	8,26,55,79,104,133
N/C	–	–	–	1,2,3,4,5,6,7,34,35,36, 37,38,39,40,44,45,46, 47,74,75,76,77,81,82, 83,84,85,86,87,114, 115,116,117,118,119, 120,124,125,126,127, 154,155,156,157
# of SIGNAL PINS	68	84	84	100
# USER I/O PINS	64	80	80	96

OE (1, 2)	Global OE Pins
GCLR	Global Clear Pin
GCLK (1, 2, 3)	Global Clock Pins
PD (1, 2)	Power-down pins
TDI, TMS, TCK, TDO	JTAG pins used for boundary scan testing or in-system programming
GND	Ground Pins
VCCINT	VCC pins for the device (+5V - Internal)
VCCIO	VCC pins for output drivers (for I/O pins) (+5V or 3.3V - I/Os)

ATF1508AS I/O Pinouts (Continued)

MC	PLB	84-lead J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP	MC	PLB	84-lead J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP
66	E	–	–	–	–	98	G	–	–	–	–
67	E/ PD2	45	43	41	63	99	G	64	66	64	101
68	E	–	–	–	64	100	G	–	–	–	102
69	E	46	44	42	65	101	G	65	67	65	103
70	E	–	46	44	67	102	G	–	69	67	105
71	E	–	–	–	–	103	G	–	–	–	–
72	E	48	47	45	68	104	G	67	70	68	106
73	E	49	48	46	69	105	G	68	71	69	107
74	E	–	–	–	–	106	G	–	–	–	–
75	E	50	49	47	70	107	G	69	72	70	108
76	E	–	–	–	71	108	G	–	–	–	109
77	E	51	50	48	72	109	G	70	73	71	110
78	E	–	51	49	73	110	G	–	74	72	111
79	E	–	–	–	–	111	G	–	–	–	–
80	E	52	52	50	78	112	G/ TDO	71	75	73	112
81	F	–	54	52	80	113	H	–	77	75	121
82	F	–	–	–	–	114	H	–	–	–	–
83	F	54	55	53	88	115	H	73	78	76	122
84	F	–	–	–	89	116	H	–	–	–	123
85	F	55	56	54	90	117	H	74	79	77	128
86	F	56	57	55	91	118	H	75	80	78	129
87	F	–	–	–	–	119	H	–	–	–	–
88	F	57	58	56	92	120	H	76	81	79	130
89	F	–	59	57	93	121	H	–	82	80	131
90	F	–	–	–	–	122	H	–	–	–	–
91	F	58	60	58	94	123	H	77	83	81	132
92	F	–	–	–	96	124	H	–	–	–	134
93	F	60	62	60	97	125	H	79	85	83	135
94	F	61	63	61	98	126	H	80	86	84	136
95	F	–	–	–	–	127	H	–	–	–	–
96	F/ TCK	62	64	62	99	128	H/ GCLK3	81	87	85	137

ATF1508ASL Standard Package Options

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
20	12	83.3	ATF1508ASL-20 JC84	84J	Commercial (0°C to 70°C)
			ATF1508ASL-20 QC100	100Q1	
			ATF1508ASL-20 AC100	100A	
			ATF1508ASL-20 QC160	160Q1	
25	15	70	ATF1508ASL-25 JI84	84J	Industrial (-40°C to +85°C)
			ATF1508ASL-25 QI100	100Q1	
			ATF1508ASL-25 AI100	100A	
			ATF1508ASL-25 QI160	160Q1	

Note: 1. The last time buy is Sept. 30, 2005 for shaded parts.

Using "C" Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the "I" to the "C" device (7 ns "C" = 10 ns "I") and de-rate power by 30%.
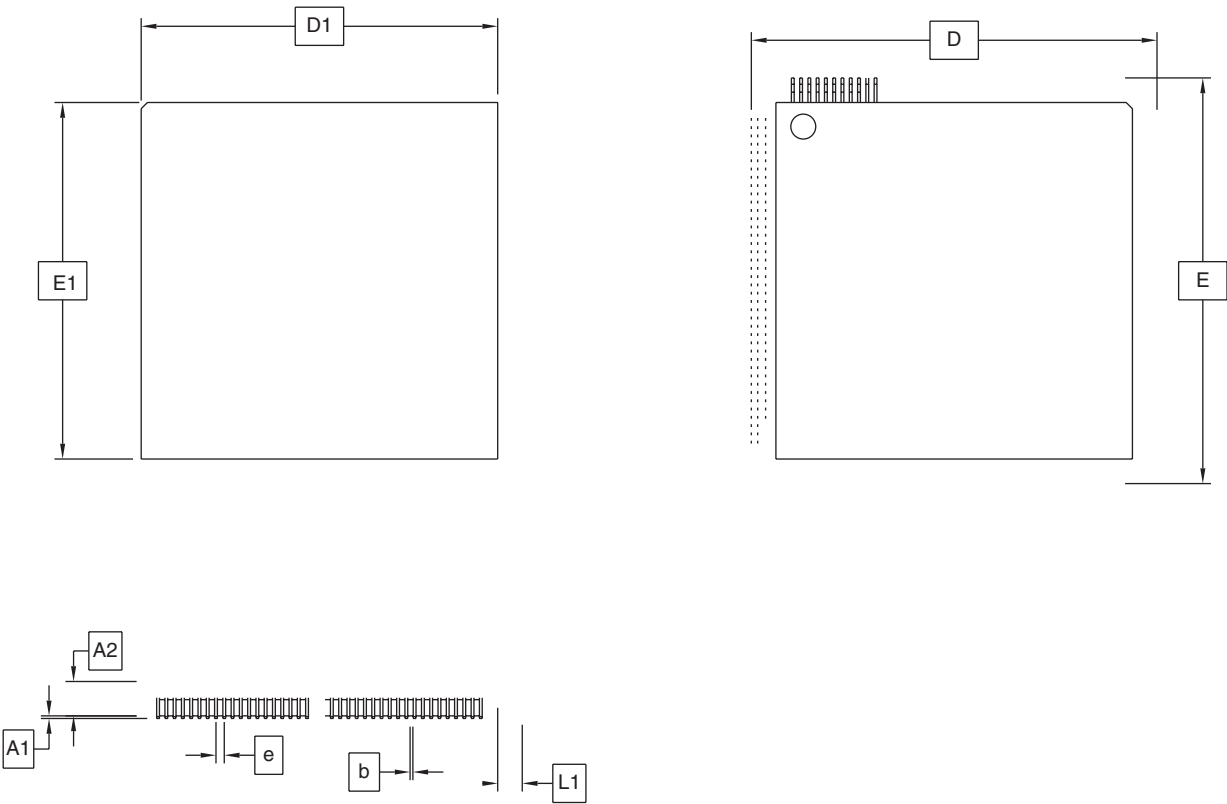
ATF1508ASL Green Package Options (Pb/Halide-free/RoHS Compliant)

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
25	15	70	ATF1508ASL-25 JU84 ATF1508ASL-25 AU100	84J 100A	Industrial (-40°C to +85°C)

Package Type	
84J	84-lead, Plastic J-leaded Chip Carrier (PLCC)
100Q1	100-lead, Plastic Quad Pin Flat Package (PQFP)
100A	100-lead, Very Thin Plastic Gull Wing Quad Flat Package (TQFP)
160Q1	160-lead, Plastic Quad Pin Flat Package (PQFP)

160Q1 – PQFP

3/28/02

		TITLE	DRAWING NO.	REV.
![AMEL]	2325 Orchard Parkway San Jose, CA 95131	**160Q1,** 160-lead, 28 x 28 mm Body, 3.2 Form Opt., Plastic Quad Flat Pack (PQFP)	160Q1	A

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