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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

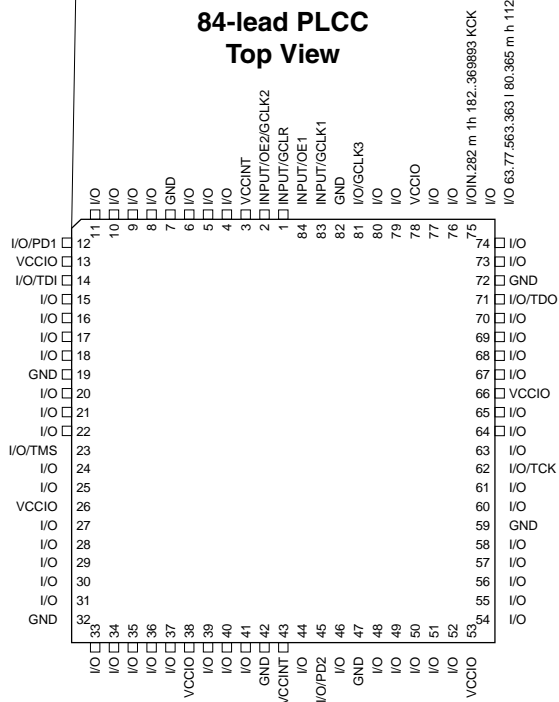
Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

| | |
|---------------------------------|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable (min 10K program/erase cycles) |
| Delay Time tpd(1) Max | 15 ns |
| Voltage Supply - Internal | 4.5V ~ 5.5V |
| Number of Logic Elements/Blocks | - |
| Number of Macrocells | 128 |
| Number of Gates | - |
| Number of I/O | 80 |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-BQFP |
| Supplier Device Package | 100-PQFP (14x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atf1508as-15qi100 |

84-lead PLCC Top View



100-lead TQFP Top View



Description

The ATF1508AS is a high-performance, high-density complex programmable logic device (CPLD) that utilizes Atmel's proven electrically-erasable technology. With 128 logic macrocells and up to 100 inputs, it easily integrates logic from several TTL, SSI, MSI, LSI and classic PLDs. The ATF1508AS's enhanced routing switch matrices increase usable gate count and increase odds of successful pin-locked design modifications.

The ATF1508AS has up to 96 bi-directional I/O pins and four dedicated input pins, depending on the type of device package selected. Each dedicated pin can also serve as a global control signal, register clock, register reset or output enable. Each of these control signals can be selected for use individually within each macrocell.

Each of the 128 macrocells generates a buried feedback that goes to the global bus. Each input and I/O pin also feeds into the global bus. The switch matrix in each logic block then selects 40 individual signals from the global bus. Each macrocell also generates a foldback logic term that goes to a regional bus. Cascade logic between macrocells in the ATF1508AS allows fast, efficient generation of complex logic functions. The ATF1508AS contains eight such logic chains, each capable of creating sum term logic with a fan-in of up to 40 product terms.

The ATF1508AS macrocell, shown in Figure 1, is flexible enough to support highly-complex logic functions operating at high speed. The macrocell consists of five sections: product terms and product term select multiplexer; OR/XOR/CASCADE logic, a flip-flop, output select and enable, and logic array inputs.

Unused macrocells are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the contents of the ATF1508AS. Two bytes (16 bits) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the security fuse.

The ATF1508AS device is an in-system programmable (ISP) device. It uses the industry-standard 4-pin JTAG interface (IEEE Std. 1149.1), and is fully compliant with JTAG's Boundary-scan Description Language (BSDL). ISP allows the device to be programmed without removing it from the printed circuit board. In addition to simplifying the manufacturing flow, ISP also allows design modifications to be made in the field via software.

Product Terms and Select Mux

Each ATF1508AS macrocell has five product terms. Each product term receives as its inputs all signals from both the global bus and regional bus.

The product term select multiplexer (PTMUX) allocates the five product terms as needed to the macrocell logic gates and control signals. The PTMUX programming is determined by the design compiler, which selects the optimum macrocell configuration.

OR/XOR/ CASCADE Logic

The ATF1508AS's logic structure is designed to efficiently support all types of logic. Within a single macrocell, all the product terms can be routed to the OR gate, creating a 5-input

Flip-flop

The ATF1508AS's flip-flop has very flexible data and control functions. The data input can come from either the XOR gate, from a separate product term or directly from the I/O pin. Selecting the separate product term allows creation of a buried registered feedback within a combinatorial output macrocell. (This feature is automatically implemented by the fitter software). In addition to D, T, JK and SR operation, the flip-flop can also be configured as a flow-through latch. In this mode, data passes through when the clock is high and is latched when the clock is low.

The clock itself can be either the Global CLK Signal (GCK) or an individual product term. The flip-flop changes state on the clock's rising edge. When the GCK signal is used as the clock, one of the macrocell product terms can be selected as a clock enable. When the clock enable function is active and the enable signal (product term) is low, all clock edges are ignored. The flip-flop's asynchronous reset signal (AR) can be either the Global Clear (GCLEAR), a product term, or always off. AR can also be a logic OR of GCLEAR with a product term. The asynchronous preset (AP) can be a product term or always off.

Extra Feedback

The ATF15xxSE Family macrocell output can be selected as registered or combinatorial. The extra buried feedback signal can be either combinatorial or a registered signal regardless of whether the output is combinatorial or registered. (This enhancement function is automatically implemented by the fitter software.) Feedback of a buried combinatorial output allows the creation of a second latch within a macrocell.

I/O Control

The output enable multiplexer (MOE) controls the output enable signal. Each I/O can be individually configured as an input, output or for bi-directional operation. The output enable for each macrocell can be selected from the true or compliment of the two output enable pins, a subset of the I/O pins, or a subset of the I/O macrocells. This selection is automatically done by the fitter software when the I/O is configured as an input, all macrocell resources are still available, including the buried feedback, expander and cascade logic.

Global Bus/Switch Matrix

The global bus contains all input and I/O pin signals as well as the buried feedback signal from all 128 macrocells. The switch matrix in each logic block receives as its inputs all signals from the global bus. Under software control, up to 40 of these signals can be selected as inputs to the logic block.

Foldback Bus

Each macrocell also generates a foldback product term. This signal goes to the regional bus and is available to 16 macrocells. The foldback is an inverse polarity of one of the macrocell's product terms. The 16 foldback terms in each region allows generation of high fan-in sum terms (up to 21 product terms) with a little additional delay.

3.3V or 5.0V I/O Operation

The ATF1508AS device has two sets of V_{CC} pins viz, V_{CCINT} and V_{CCIO} . V_{CCINT} pins must always be connected to a 5.0V power supply. V_{CCINT} pins are for input buffers and are "compatible" with both 3.3V and 5.0V inputs. V_{CCIO} pins are for I/O output drives and can be connected for 3.3/5.0V power supply.

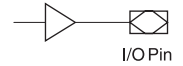
Open-collector Output Option

This option enables the device output to provide control signals such as an interrupt that can be asserted by any of the several devices.

Figure 1. ATF1508AS Macrocell

SWITCH REGIONAL
F●

D/T/L



I/O Pin

SLEW
RATE

OPEN COLLECTOR
OPTION

MACROCELL REDUCED POWER BIT

Programmable Pin-keeper Option for Inputs and I/Os

The ATF1508AS offers the option of programming all input and I/O pins so that “pin-keeper” circuits can be utilized. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high- or low-level. This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

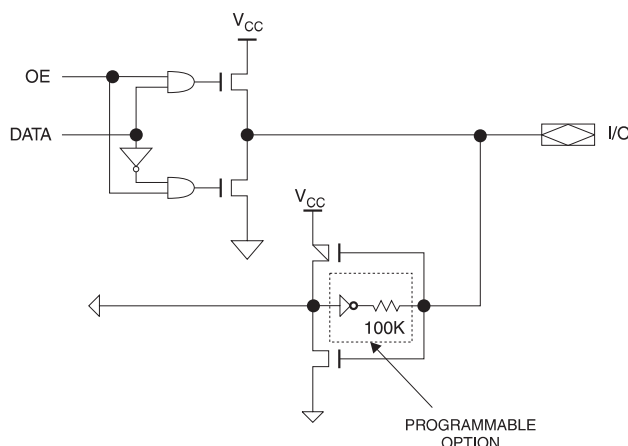
Input Diagram

Speed/Power Management

The ATF1508AS has several built-in speed and power management features. The ATF1508AS contains circuitry that automatically puts the device into a low-power stand-by mode when no logic transitions are occurring. This not only reduces power consumption during inactive periods, but also provides proportional power-savings for most applications running at system speeds below 5 MHz.

To further reduce power, each ATF1508AS macrocell has a Reduced-power bit feature. This feature allows individual macrocells to be configured for maximum power savings. This feature may be selected as a design option.

I/O Diagram



All ATF1508 also have an optional power-down mode. In this mode, current drops to below 10 mA. When the power-down option is selected, either PD1 or PD2 pins (or both) can be used to power down the part. The power-down option is selected in the design source file. When enabled, the device goes into power-down when either PD1 or PD2 is high. In the power-down mode, all internal logic signals are latched and held, as are any enabled outputs.

All pin transitions are ignored until the PD pin is brought low. When the power-down feature is enabled, the PD1 or PD2 pin cannot be used as a logic input or output. However, the pin's macrocell may still be used to generate buried foldback and cascade logic signals.

All power-down AC characteristic parameters are computed from external input or I/O pins, with Reduced-power Bit turned on. For macrocells in reduced-power mode (Reduced-power bit turned on), the reduced-power adder, tRPA, must be added to the AC parameters, which include the data paths t_{LAD} , t_{LAC} , t_{IC} , t_{ACL} , t_{ACH} and t_{SEXP} .

Each output also has individual slew rate control. This may be used to reduce system noise by slowing down outputs that do not need to operate at maximum speed. Outputs default to slow switching, and may be specified as fast switching in the design file.



Design
Software
Support





BSC Configuration Pins and Macrocells (Except JTAG TAP Pins)

Dedic

To Internal

D

TDO

TDI

(From Next Register)

Note: The ATF1508AS has a pull-up option on TMS and TDI pins. This feature is selected as a design option.

BSC Configuration for Macrocell

Boundary Scan Definition Language (BSDL) Models for the ATF1508

These are now available in all package types via the Atmel Web Site. These models can be used for Boundary-scan Test Operation in the ATF1508AS and have been scheduled to conform to the IEEE 1149.1 standard.

PCI DC Characteristics

| Symbol | Parameter | Conditions | Min | Max | Units |
|-------------|---|--------------------------------------|------|----------------|---------|
| V_{CC} | Supply Voltage | | 4.75 | 5.25 | V |
| V_{IH} | Input High Voltage | | 2.0 | $V_{CC} + 0.5$ | V |
| V_{IL} | Input Low Voltage | | -0.5 | 0.8 | V |
| I_{IH} | Input High Leakage Current ⁽¹⁾ | $V_{IN} = 2.7V$ | | 70 | μA |
| I_{IL} | Input Low Leakage Current ⁽¹⁾ | $V_{IN} = 0.5V$ | | -70 | μA |
| V_{OH} | Output High Voltage | $I_{OUT} = -2\text{ mA}$ | 2.4 | | V |
| V_{OL} | Output Low Voltage | $I_{OUT} = 3\text{ mA}, 6\text{ mA}$ | | 0.55 | V |
| C_{IN} | Input Pin Capacitance | | | 10 | pF |
| C_{CLK} | CLK Pin Capacitance | | | 12 | pF |
| C_{IDSEL} | IDSEL Pin Capacitance | | | 8 | pF |
| L_{PIN} | Pin Inductance | | | 20 | nH |

Note: 1. Leakage current is without pin-keeper off.

PCI AC Characteristics

| Symbol | Parameter | Conditions | Min | Max | Units |
|--------------|--------------|--------------------------|-------------------------------|---------------------------|-------|
| $I_{OH(AC)}$ | Switching | $0 < V_{OUT} \leq 1.4$ | -44 | | mA |
| | Current High | $1.4 < V_{OUT} < 2.4$ | $-44 + (V_{OUT} - 1.4)/0.024$ | | mA |
| | | $3.1 < V_{OUT} < V_{CC}$ | | Equation A ⁽¹⁾ | mA |

Notes: 1. Equation A: $I_{OH} = 11.9 (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$ for $V_{CC} > V_{OUT} > 3.1V$.
2. Equation B: $I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$ for $0V < V_{OUT} < 0.71V$.

DC and AC Operating Conditions

| | Commercial | Industrial |
|---|-------------|--------------|
| Operating Temperature (Ambient) | 0°C - 70°C | -40°C - 85°C |
| V _{CCINT} or V _{CCIO} (5V) Power Supply | 5V ± 5% | 5V ± 10% |
| V _{CCIO} (3.3V) Power Supply | 2.7V - 3.6V | 2.7V - 3.6V |

DC Characteristics⁽¹⁾

| Symbol | Parameter | Condition | | | Min | Typ | Max | Units |
|---------------------------------|---------------------------------------|--|-----------|------|------|-----|-------------------------|-------|
| I _{IL} | Input or I/O Low Leakage Current | V _{IN} = V _{CC} | | | | -2 | -10 | μA |
| I _{IH} | Input or I/O High Leakage Current | | | | | 2 | 10 | μA |
| I _{OZ} | Tri-state Output Off-state Current | V _O = V _{CC} or GND | | | -40 | | 40 | μA |
| I _{CC1} | Power Supply Current, Standby | V _{CC} = Max V _{IN} = 0, V _{CC} | Std Mode | Com. | | 160 | | mA |
| | | | | Ind. | | 180 | | mA |
| | | | “L” Mode | Com. | | 10 | | μA |
| | | | | Ind. | | 10 | | μA |
| I _{CC2} | Power Supply Current, Power-down Mode | V _{CC} = Max V _{IN} = 0, V _{CC} | “PD” Mode | | | 1 | 10 | mA |
| I _{CC3} ⁽²⁾ | Reduced-power Mode Supply Current | V _{CC} = Max V _{IN} = 0, V _{CC} | Std Mode | Com. | | 65 | | mA |
| | | | | Ind. | | 85 | | mA |
| V _{CCIO} | Supply Voltage | 5.0V Device Output | Com. | | 4.75 | | 5.25 | V |
| | | | Ind. | | 4.5 | | 5.5 | V |
| V _{CCIO} | Supply Voltage | 3.3V Device Output | | | 3.0 | | 3.6 | V |
| V _{IL} | Input Low Voltage | | | | -0.3 | | 0.8 | V |
| V _{IH} | Input High Voltage | | | | 2.0 | | V _{CCIO} + 0.3 | V |
| V _{OL} | Output Low Voltage (TTL) | V _{IN} = V _{IH} or V _{IL} V _{CCIO} = MIN, I _{OL} = 12 mA | Com. | | | | 0.45 | V |
| | | | Ind. | | | | 0.45 | V |
| | Output Low Voltage (CMOS) | V _{IN} = V _{IH} or V _{IL} V _{CC} = MIN, I _{OL} = 0.1 mA | Com. | | | | 0.2 | V |
| | | | Ind. | | | | 0.2 | V |
| V _{OH} | Output High Voltage (TTL) | V _{IN} = V _{IH} or V _{IL} V _{CCIO} = MIN, I _{OH} = -4.0 mA | | | 2.4 | | | V |

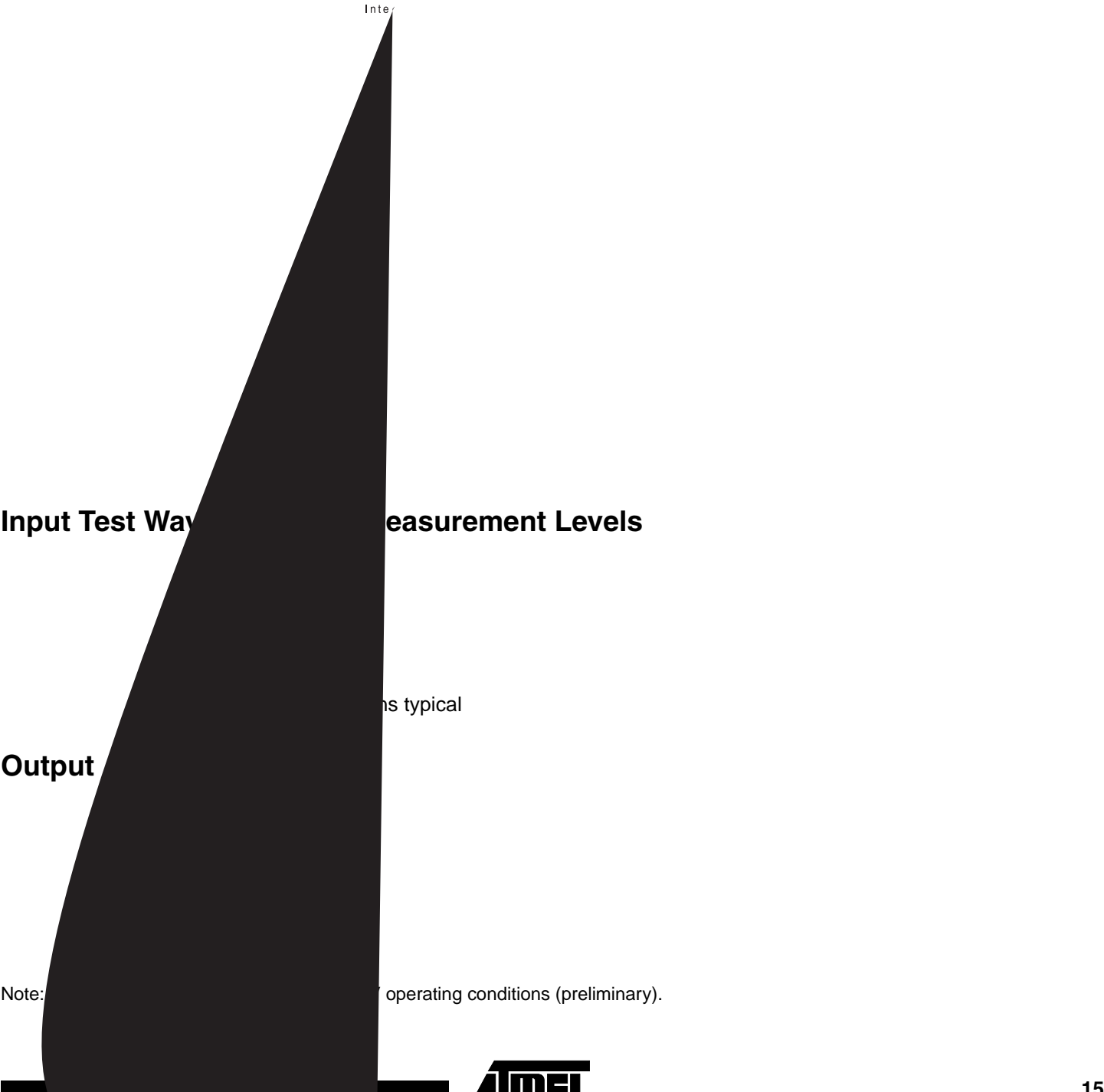
Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. I_{CC3} refers to the current in the reduced-power mode when macrocell reduced-power is turned ON.

Pin Capacitance⁽¹⁾

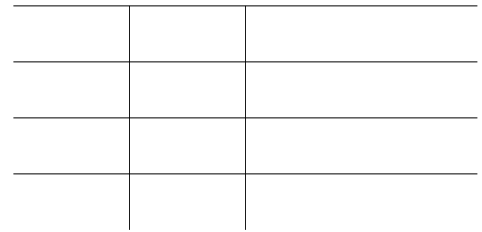
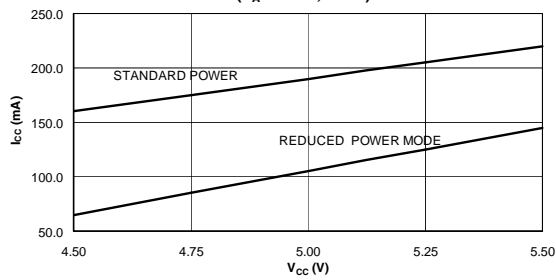
| | Typ | Max | Units | Conditions |
|------------------|-----|-----|-------|------------------------------------|
| C _{IN} | 8 | 10 | pF | V _{IN} = 0V; f = 1.0 MHz |
| C _{I/O} | 8 | 10 | pF | V _{OUT} = 0V; f = 1.0 MHz |

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested. The OGI pin (high-voltage pin during programming) has a maximum capacitance of 12 pF.

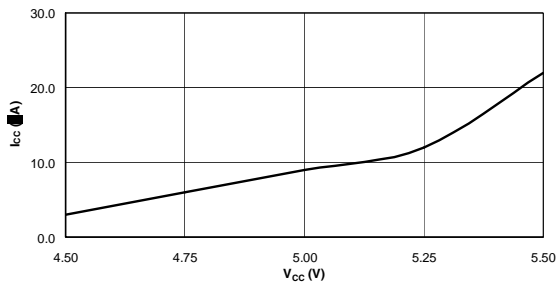
Timing Model



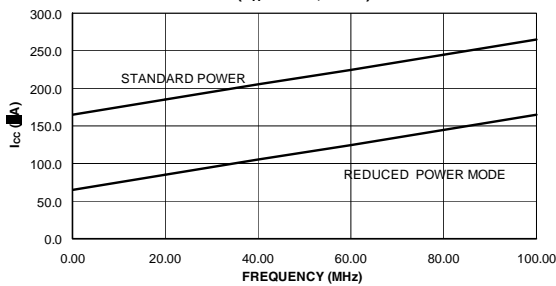
SUPPLY CURRENT VS. SUPPLY VOLTAGE
($T_A = 25^\circ\text{C}$, $F = 0$)



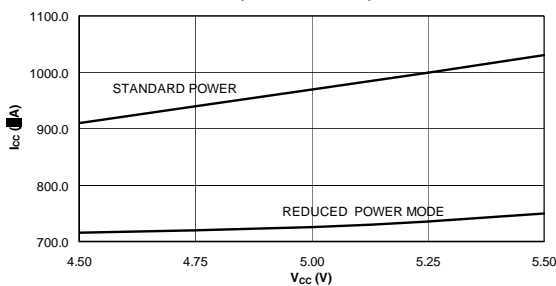
SUPPLY CURRENT VS. SUPPLY VOLTAGE
LOW-POWER ("L") VERSION
($T_A = 25^\circ\text{C}$, $F = 0$)

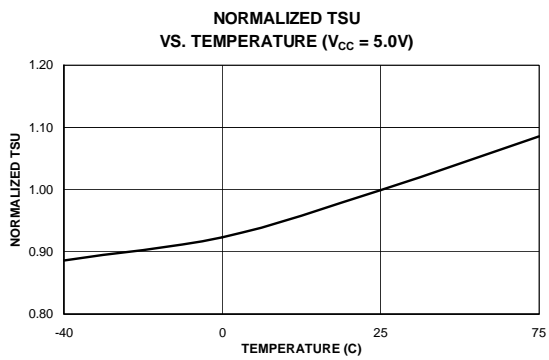


SUPPLY CURRENT VS. FREQUENCY
STANDARD POWER
($T_A = 25^\circ\text{C}$, $F = 0$)



SUPPLY CURRENT VS. SUPPLY VOLTAGE
PIN-CONTROLLED POWER-DOWN MODE
($T_A = 25^\circ\text{C}$, $F = 0$)





AC Characteristics (Continued)⁽¹⁾

| Symbol | Parameter | -7 | | -10 | | -15 | | -20 | | -25 | | Units |
|------------|--|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{OD2} | Output Buffer and Pad Delay (Slow slew rate = OFF; $V_{CCIO} = 3.3V$; $C_L = 35$ pF) | | 2.5 | | 2.0 | | 5 | | 6 | | 7 | ns |
| t_{OD3} | Output Buffer and Pad Delay (Slow slew rate = ON; $V_{CCIO} = 5V$ or $3.3V$; $C_L = 35$ pF) | | 5 | | 5.5 | | 8 | | 10 | | 12 | ns |
| t_{ZX1} | Output Buffer Enable Delay (Slow slew rate = OFF; $V_{CCIO} = 5.0V$; $C_L = 35$ pF) | | 4.0 | | 5.0 | | 7 | | 9 | | 10 | ns |
| t_{ZX2} | Output Buffer Enable Delay (Slow slew rate = OFF; $V_{CCIO} = 3.3V$; $C_L = 35$ pF) | | 4.5 | | 5.5 | | 7 | | 9 | | 10 | ns |
| t_{ZX3} | Output Buffer Enable Delay (Slow slew rate = ON; $V_{CCIO} = 5.0V/3.3V$; $C_L = 35$ pF) | | 9 | | 9 | | 10 | | 11 | | 12 | ns |
| t_{XZ} | Output Buffer Disable Delay ($C_L = 5$ pF) | | 4 | | 5 | | 6 | | 7 | | 8 | ns |
| t_{SU} | Register Setup Time | 3 | | 2 | | 4 | | 5 | | 6 | | ns |
| t_H | Register Hold Time | 2 | | 3 | | 4 | | 5 | | 6 | | ns |
| t_{FSU} | Register Setup Time of Fast Input | 3 | | 3 | | 2 | | 2 | | 3 | | ns |
| t_{FH} | Register Hold Time of Fast Input | 0.5 | | 0.5 | | 2 | | 2 | | 2.5 | | ns |
| t_{RD} | Register Delay | | 1 | | 2 | | 1 | | 2 | | 2 | ns |
| t_{COMB} | Combinatorial Delay | | 1 | | 2 | | 1 | | 2 | | 2 | ns |
| t_{IC} | Array Clock Delay | | 3 | | 5 | | 6 | | 7 | | 8 | ns |
| t_{EN} | Register Enable Time | | 3 | | 5 | | 6 | | 7 | | 8 | ns |
| t_{GLOB} | Global Control Delay | | 1 | | 1 | | 1 | | 1 | | 1 | ns |
| t_{PRE} | Register Preset Time | | 2 | | 3 | | 4 | | 5 | | 6 | ns |
| t_{CLR} | Register Clear Time | | 2 | | 3 | | 4 | | 5 | | 6 | ns |
| t_{UIM} | Switch Matrix Delay | | 1 | | 1 | | 2 | | 2 | | 2 | ns |
| t_{RPA} | Reduced-power Adder ⁽²⁾ | | 10 | | 11 | | 13 | | 14 | | 15 | ns |

- Notes: 1. See ordering information for valid part numbers.
2. The t_{RPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{TIC} , t_{ACL} , and t_{SEXP} parameters for macrocells running in the reduced-power mode.

ATF1508AS I/O Pinouts (Continued)

| MC | PLB | 84-lead J-lead | 100-lead PQFP | 100-lead TQFP | 160-lead PQFP | MC | PLB | 84-lead J-lead | 100-lead PQFP | 100-lead TQFP | 160-lead PQFP |
|----|-----------|-------------------|------------------|------------------|------------------|-----|-------------|-------------------|------------------|------------------|------------------|
| 66 | E | — | — | — | — | 98 | G | — | — | — | — |
| 67 | E/ PD2 | 45 | 43 | 41 | 63 | 99 | G | 64 | 66 | 64 | 101 |
| 68 | E | — | — | — | 64 | 100 | G | — | — | — | 102 |
| 69 | E | 46 | 44 | 42 | 65 | 101 | G | 65 | 67 | 65 | 103 |
| 70 | E | — | 46 | 44 | 67 | 102 | G | — | 69 | 67 | 105 |
| 71 | E | — | — | — | — | 103 | G | — | — | — | — |
| 72 | E | 48 | 47 | 45 | 68 | 104 | G | 67 | 70 | 68 | 106 |
| 73 | E | 49 | 48 | 46 | 69 | 105 | G | 68 | 71 | 69 | 107 |
| 74 | E | — | — | — | — | 106 | G | — | — | — | — |
| 75 | E | 50 | 49 | 47 | 70 | 107 | G | 69 | 72 | 70 | 108 |
| 76 | E | — | — | — | 71 | 108 | G | — | — | — | 109 |
| 77 | E | 51 | 50 | 48 | 72 | 109 | G | 70 | 73 | 71 | 110 |
| 78 | E | — | 51 | 49 | 73 | 110 | G | — | 74 | 72 | 111 |
| 79 | E | — | — | — | — | 111 | G | — | — | — | — |
| 80 | E | 52 | 52 | 50 | 78 | 112 | G/ TDO | 71 | 75 | 73 | 112 |
| 81 | F | — | 54 | 52 | 80 | 113 | H | — | 77 | 75 | 121 |
| 82 | F | — | — | — | — | 114 | H | — | — | — | — |
| 83 | F | 54 | 55 | 53 | 88 | 115 | H | 73 | 78 | 76 | 122 |
| 84 | F | — | — | — | 89 | 116 | H | — | — | — | 123 |
| 85 | F | 55 | 56 | 54 | 90 | 117 | H | 74 | 79 | 77 | 128 |
| 86 | F | 56 | 57 | 55 | 91 | 118 | H | 75 | 80 | 78 | 129 |
| 87 | F | — | — | — | — | 119 | H | — | — | — | — |
| 88 | F | 57 | 58 | 56 | 92 | 120 | H | 76 | 81 | 79 | 130 |
| 89 | F | — | 59 | 57 | 93 | 121 | H | — | 82 | 80 | 131 |
| 90 | F | — | — | — | — | 122 | H | — | — | — | — |
| 91 | F | 58 | 60 | 58 | 94 | 123 | H | 77 | 83 | 81 | 132 |
| 92 | F | — | — | — | 96 | 124 | H | — | — | — | 134 |
| 93 | F | 60 | 62 | 60 | 97 | 125 | H | 79 | 85 | 83 | 135 |
| 94 | F | 61 | 63 | 61 | 98 | 126 | H | 80 | 86 | 84 | 136 |
| 95 | F | — | — | — | — | 127 | H | — | — | — | — |
| 96 | F/ TCK | 62 | 64 | 62 | 99 | 128 | H/ GCLK3 | 81 | 87 | 85 | 137 |

ATF1508ASL Standard Package Options

| t_{PD} (ns) | t_{CO1} (ns) | f_{MAX} (MHz) | Ordering Code | Package | Operation Range |
|------------------|-------------------|--------------------|---------------------|---------|--------------------------------|
| 20 | 12 | 83.3 | ATF1508ASL-20 JC84 | 84J | Commercial (0°C to 70°C) |
| | | | ATF1508ASL-20 QC100 | 100Q1 | |
| | | | ATF1508ASL-20 AC100 | 100A | |
| | | | ATF1508ASL-20 QC160 | 160Q1 | |
| 25 | 15 | 70 | ATF1508ASL-25 JI84 | 84J | Industrial (-40°C to +85°C) |
| | | | ATF1508ASL-25 QI100 | 100Q1 | |
| | | | ATF1508ASL-25 AI100 | 100A | |
| | | | ATF1508ASL-25 QI160 | 160Q1 | |

Note: 1. The last time buy is Sept. 30, 2005 for shaded parts.

Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

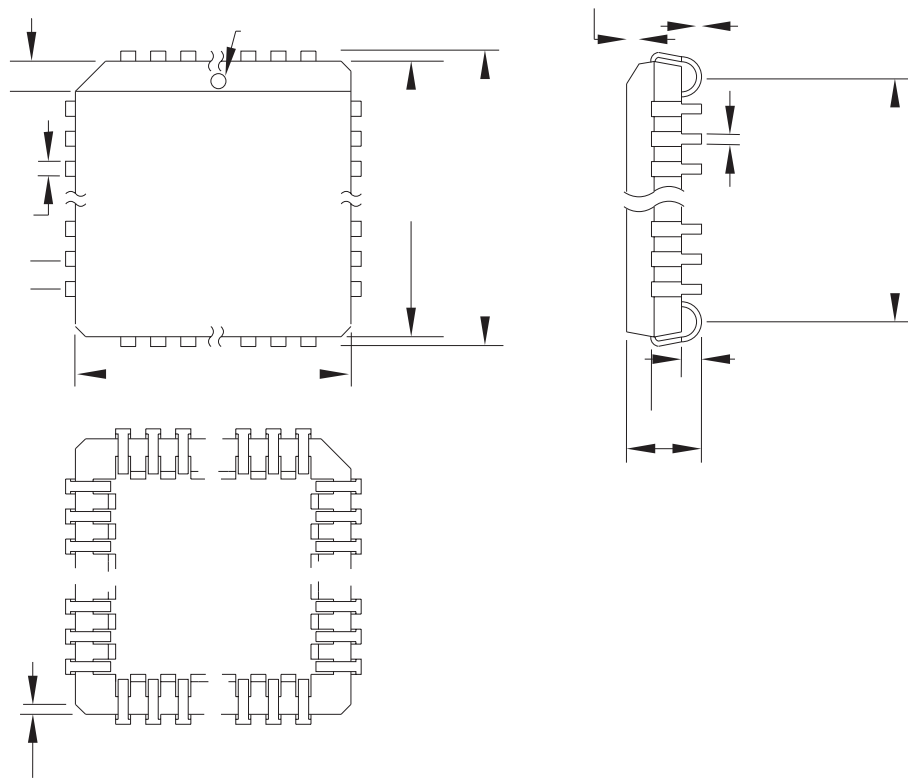
ATF1508ASL Green Package Options (Pb/Halide-free/RoHS Compliant)

| t_{PD} (ns) | t_{CO1} (ns) | f_{MAX} (MHz) | Ordering Code | Package | Operation Range |
|------------------|-------------------|--------------------|---------------------|---------|--------------------------------|
| 25 | 15 | 70 | ATF1508ASL-25 JU84 | 84J | Industrial (-40°C to +85°C) |
| | | | ATF1508ASL-25 AU100 | 100A | |

| Package Type | |
|--------------|--|
| 84J | 84-lead, Plastic J-leaded Chip Carrier (PLCC) |
| 100Q1 | 100-lead, Plastic Quad Pin Flat Package (PQFP) |
| 100A | 100-lead, Very Thin Plastic Gull Wing Quad Flat Package (TQFP) |
| 160Q1 | 160-lead, Plastic Quad Pin Flat Package (PQFP) |

Package Information

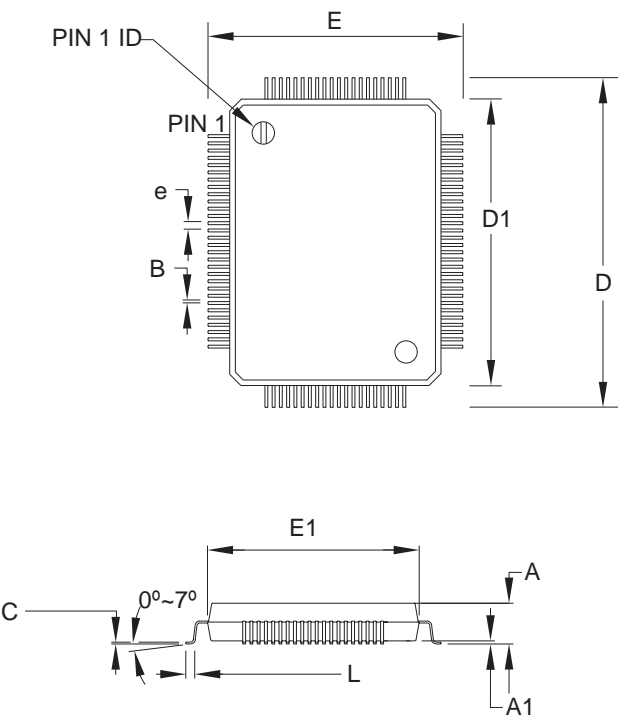
84J – PLCC



10/04/01

| | | | |
|--|---|---------------------------|------------------|
|  2325 Orchard Parkway San Jose, CA 95131 | TITLE 84J, 84-lead, Plastic J-leaded Chip Carrier (PLCC) | DRAWING NO. 84J | REV. B |
|--|---|---------------------------|------------------|

100Q1 – PQFP



COMMON DIMENSIONS
(Unit of Measure = mm)
JEDEC STANDARD MS-022, GC-1

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----------|------|------|------|
| A | – | 3.04 | 3.4 | |
| A1 | 0.25 | 0.33 | 0.5 | |
| D | 23.20 BSC | | | |
| E | 17.20 BSC | | | |
| E1 | 14.00 BSC | | | |
| B | 0.22 | – | 0.40 | |
| C | 0.11 | – | 0.23 | |
| D1 | 20 BSC | | | |
| L | 0.73 | – | 1.03 | |
| e | 0.65 BSC | | | |

07/6/2005



2325 Orchard Parkway
San Jose, CA 95131

TITLE

100Q1, 100-lead, 14 x 20 mm Body, 3.2 mm Footprint, 0.65 mm Pitch,
Plastic Quad Flat Package (PQFP)

DRAWING NO.

100Q1

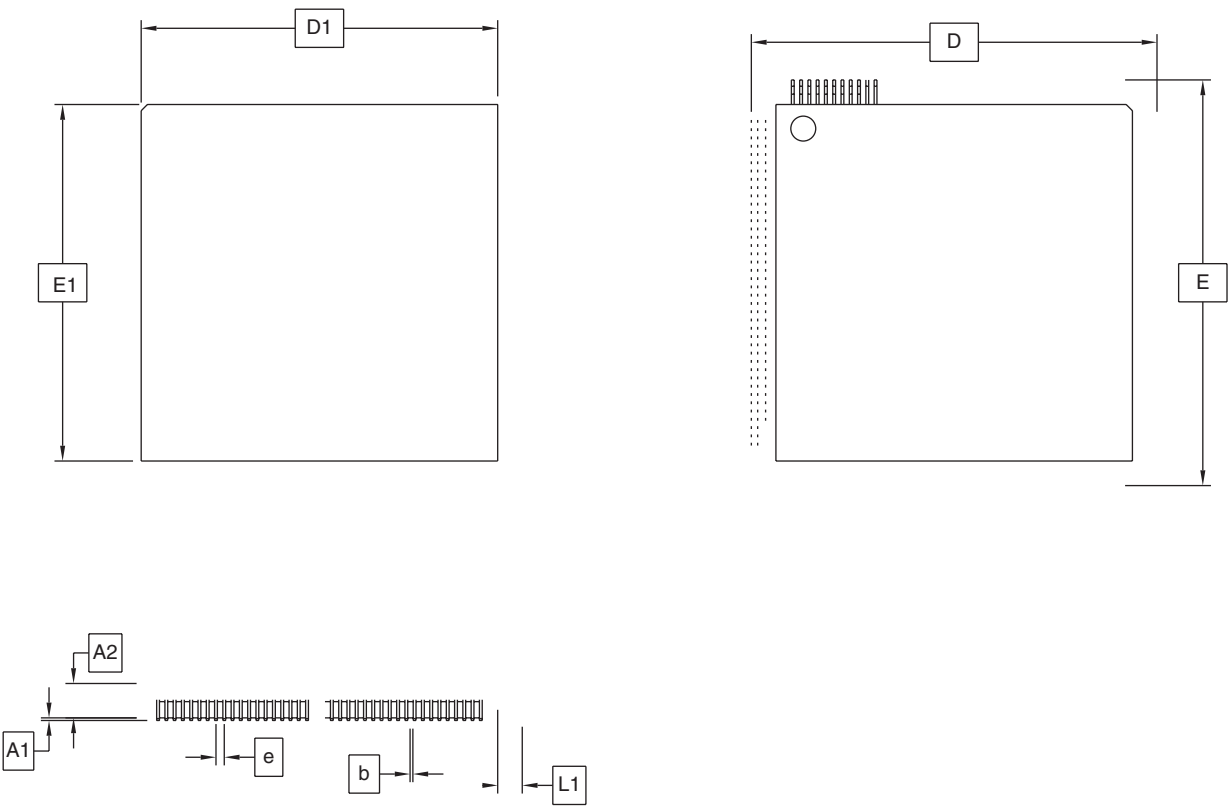
REV.

C






160Q1 – PQFP



3/28/02

| | | | |
|--|---|-----------------------------|------------------|
|  2325 Orchard Parkway San Jose, CA 95131 | TITLE 160Q1 , 160-lead, 28 x 28 mm Body, 3.2 Form Opt., Plastic Quad Flat Pack (PQFP) | DRAWING NO. 160Q1 | REV. A |
|--|---|-----------------------------|------------------|



Revision History

| Revision | Comments |
|----------|---|
| 0784P | Green package options added. |
| 0784O | The ATF1508ASL-25 commercial speed offering was obsoleted in 2002 and replaced by the ATF1508ASL-20 commercial speed grade. |