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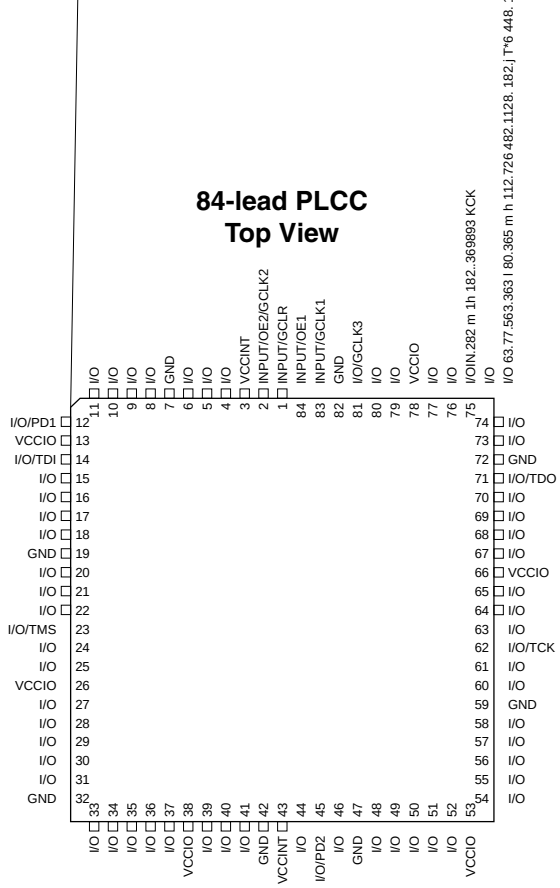
Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable (min 10K program/erase cycles)
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	80
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atf1508as-7ac100

84-lead PLCC
Top View



100-lead TQFP
Top View

Description

The ATF1508AS is a high-performance, high-density complex programmable logic device (CPLD) that utilizes Atmel's proven electrically-erasable technology. With 128 logic macrocells and up to 100 inputs, it easily integrates logic from several TTL, SSI, MSI, LSI and classic PLDs. The ATF1508AS's enhanced routing switch matrices increase usable gate count and increase odds of successful pin-locked design modifications.

The ATF1508AS has up to 96 bi-directional I/O pins and four dedicated input pins, depending on the type of device package selected. Each dedicated pin can also serve as a global control signal, register clock, register reset or output enable. Each of these control signals can be selected for use individually within each macrocell.

Each of the 128 macrocells generates a buried feedback that goes to the global bus. Each input and I/O pin also feeds into the global bus. The switch matrix in each logic block then selects 40 individual signals from the global bus. Each macrocell also generates a foldback logic term that goes to a regional bus. Cascade logic between macrocells in the ATF1508AS allows fast, efficient generation of complex logic functions. The ATF1508AS contains eight such logic chains, each capable of creating sum term logic with a fan-in of up to 40 product terms.

The ATF1508AS macrocell, shown in Figure 1, is flexible enough to support highly-complex logic functions operating at high speed. The macrocell consists of five sections: product terms and product term select multiplexer; OR/XOR/CASCADE logic, a flip-flop, output select and enable, and logic array inputs.

Unused macrocells are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the contents of the ATF1508AS. Two bytes (16 bits) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the security fuse.

The ATF1508AS device is an in-system programmable (ISP) device. It uses the industry-standard 4-pin JTAG interface (IEEE Std. 1149.1), and is fully compliant with JTAG's Boundary-scan Description Language (BSDL). ISP allows the device to be programmed without removing it from the printed circuit board. In addition to simplifying the manufacturing flow, ISP also allows design modifications to be made in the field via software.

Product Terms and Select Mux

Each ATF1508AS macrocell has five product terms. Each product term receives as its inputs all signals from both the global bus and regional bus.

The product term select multiplexer (PTMUX) allocates the five product terms as needed to the macrocell logic gates and control signals. The PTMUX programming is determined by the design compiler, which selects the optimum macrocell configuration.

OR/XOR/ CASCADE Logic

The ATF1508AS's logic structure is designed to efficiently support all types of logic. Within a single macrocell, all the product terms can be routed to the OR gate, creating a 5-input
e opeme(e6c-)e.4.e9hd.6cagicrLogic1.3(o5.)(6cagigic1.3ic1.3.n6c4)n6a0uLu9y3(.3mDEsi2ih.1eiy)1-5

Figure 1. ATF1508AS Macrocell

Programmable Pin-keeper Option for Inputs and I/Os

The ATF1508AS offers the option of programming all input and I/O pins so that “pin-keeper” circuits can be utilized. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high- or low-level. This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

Input Diagram

ISP Programming Protection

The ATF1508AS has a special feature that locks the device and prevents the inputs and I/O from driving if the programming process is interrupted for any reason. The inputs and I/O default to high-Z state during such a condition. In addition the pin-keeper option preserves the former state during device programming.

All ATF1508AS devices are initially shipped in the erased state thereby making them ready to use for ISP.

Note: For more information refer to the “Designing for In-System Programmability with Atmel CPLDs” application note.

JTAG-BST Overview

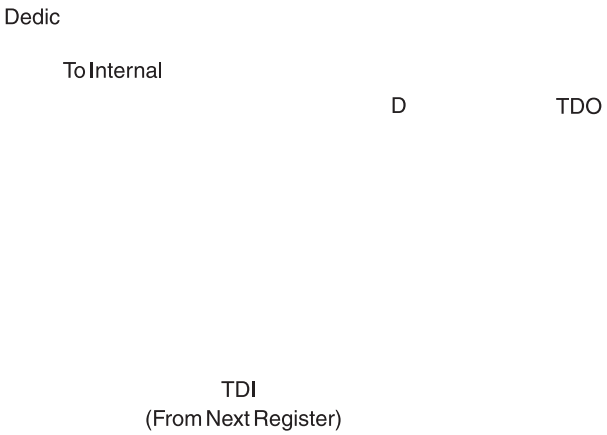
The JTAG boundary-scan testing is controlled by the Test Access Port (TAP) controller in the ATF1508AS. The boundary-scan technique involves the inclusion of a shift-register stage (contained in a boundary-scan cell) adjacent to each component so that signals at component boundaries can be controlled and observed using scan testing principles. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary-scan testing. The ATF1508AS does not currently include a Test Reset (TRST) input pin because the TAP controller is automatically reset at power-up. The six JTAG BST modes supported include: SAMPLE/PRELOAD, EXTEST, BYPASS and IDCODE. BST on the ATF1508AS is implemented using the Boundary-scan Definition Language (BSDL) described in the JTAG specification (IEEE Standard 1149.1). Any third-party tool that supports the BSDL format can be used to perform BST on the ATF1508AS.

The ATF1508AS also has the option of using four JTAG-standard I/O pins for In-System programming (ISP). The ATF1508AS is programmable through the four JTAG pins using programming compatible with the IEEE JTAG Standard 1149.1. Programming is performed by using 5V TTL-level programming signals from the JTAG ISP interface. The JTAG feature is a programmable option. If JTAG (BST or ISP) is not needed, then the four JTAG control pins are available as I/O pins.

JTAG Boundary-scan Cell (BSC) Testing

The ATF1508AS contains up to 96 I/O pins and four input pins, depending on the device type and package type selected. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary-scan testing as described in detail by IEEE Standard 1149.1. A typical BSC consists of three capture registers or scan registers and up to two update registers. There are two types of BSCs, one for input or I/O pin, and one for the macrocells. The BSCs in the device are chained together through the (BST) capture registers. Input to the capture register chain is fed in from the TDI pin while the output is directed to the TDO pin. Capture registers are used to capture active device data signals, to shift data in and out of the device and to load data into the update registers. Control signals are generated internally by the JTAG TAP controller. The BSC configuration for the input and I/O pins and macrocells are shown below.

BSC Configuration Pins and Macrocells (Except JTAG TAP Pins)



Note: The ATF1508AS has a pull-up option on TMS and TDI pins. This feature is selected as a design option.

BSC Configuration for Macrocell

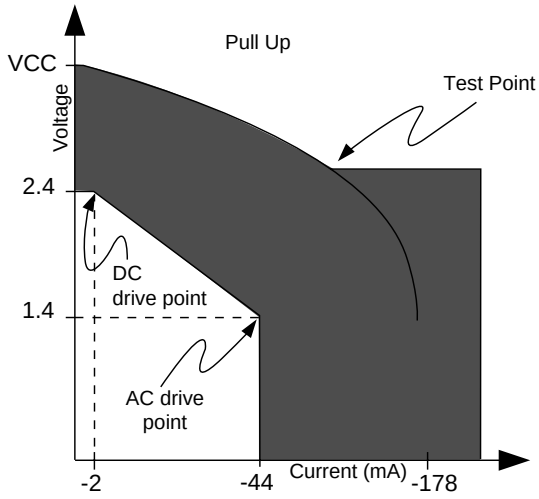
Boundary Scan Definition Language (BSDL) Models for the ATF1508

These are now available in all package types via the Atmel Web Site. These models can be used for Boundary-scan Test Operation in the ATF1508AS and have been scheduled to conform to the IEEE 1149.1 standard.

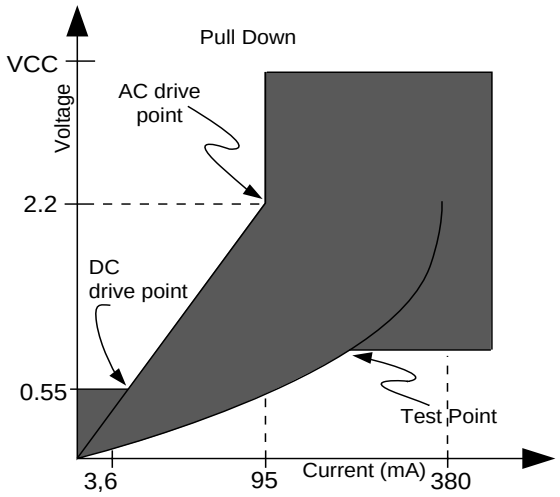
PCI Compliance

The ATF1508AS also supports the growing need in the industry to support the new Peripheral Component Interconnect (PCI) interface standard in PCI-based designs and specifications. The PCI interface calls for high current drivers, which are much larger than the traditional TTL drivers.

PCI Voltage-to-current Curves for +5V Signaling in Pull-up Mode



PCI Voltage-to-current Curves for +5V Signaling in Pull-down Mode



Power-down Mode

The ATF1508AS includes two pins for optional pin-controlled power-down feature. When this mode is enabled, the PD pin acts as the power-down pin. When the PD1 and PD2 pin is high, the device supply current is reduced to less than 10 mA. During power-down, all output data and internal logic states are latched and held. Therefore, all registered and combinatorial output data remain valid. Any outputs that were in a high-Z state at the onset will remain at high-Z. During power-down, all input signals except the power-down pin are blocked. Input and I/O hold latches remain active to ensure that pins do not float to indeterminate levels, further reducing system power. The power-down pin feature is enabled in the logic design file. Designs using either power-down pin may not use the PD pin logic array input. However, buried logic resources in this macrocell may still be used.

Power-down AC Characteristics(1)(2)

		-7		-10		-15		-20		-25		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{IVDH}	Valid I, I/O before PD High	7		10		15		20		25		ns
t_{GVDH}	Valid OE(2) before PD High	7		10		15		20		25		ns
t_{CVDH}	Valid Clock(2) before PD High	7		10		15		20		25		ns
t_{DHIX}	I, I/O Don't Care after PD High		12		15		25		30		35	ns
t_{DHGX}	OE(2) Don't Care after PD High		12		15		25		30		35	ns
t_{DHCX}	Clock(2) Don't Care after PD High		12		15		25		30		35	ns
t_{DLIV}	PD Low to Valid I, I/O		1		1		1		1		1	µs
t_{DLGV}	PD Low to Valid OE (Pin or Term)		1		1		1		1		1	µs
t_{DLCV}	PD Low to Valid Clock (Pin or Term)		1		1		1		1		1	µs
t_{DLOV}	PD Low to Valid Output		1		1		1		1		1	µs

Notes: 1. For slow slew outputs, add t_{SSO}.
2. Pin or product term.

Absolute Maximum Ratings*

Temperature Under Bias ..... -40°C to +85°C

Storage Temperature ..... -65°C to +150°C

Voltage on Any Pin with
Respect to Ground .....-2.0V to +7.0V(1)

Voltage on Input Pins
with Respect to Ground
During Programming.....-2.0V to +14.0V(1)

Programming Voltage with
Respect to Ground .....-2.0V to +14.0V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to 7.0V for pulses of less than 20 ns.

Pin Capacitance[1]

	Typ	Max	Units	Conditions
C_{IN}	8	10	pF	V_{IN} = 0V; f = 1.0 MHz
$C_{I/O}$	8	10	pF	V_{OUT} = 0V; f = 1.0 MHz

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested. The OGI pin (high-voltage pin during programming) has a maximum capacitance of 12 pF.

Timing Model

Inte

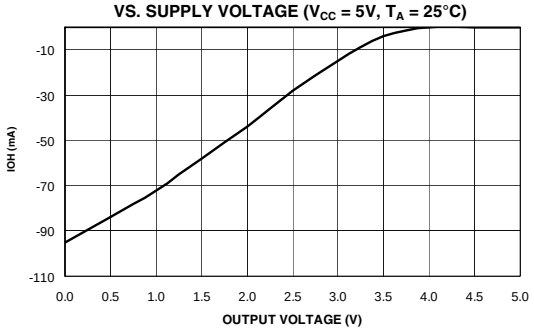
Input Test Wav easurement Levels

ns typical

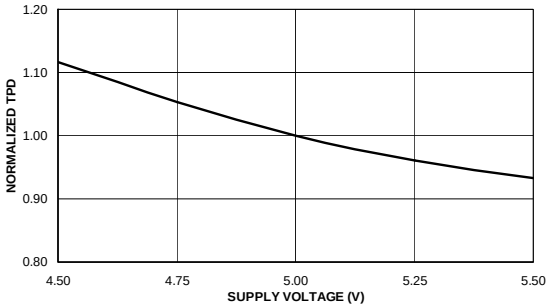
Output

Note: operating conditions (preliminary).

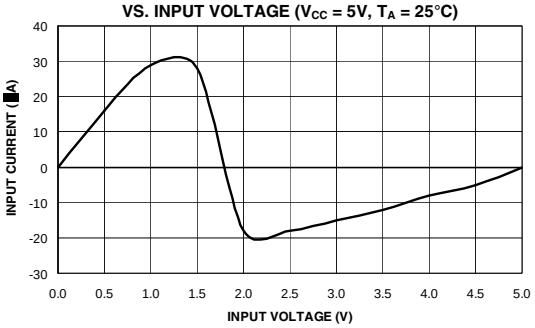
OUTPUT SOURCE CURRENT
VS. SUPPLY VOLTAGE (V_{CC} = 5V, T_A = 25°C)



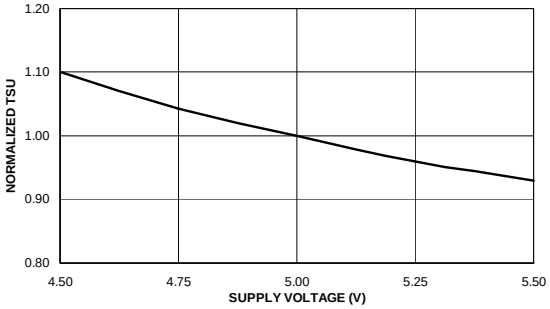
NORMALIZED TCO
VS. SUPPLY VOLTAGE (T_A = 25°C)



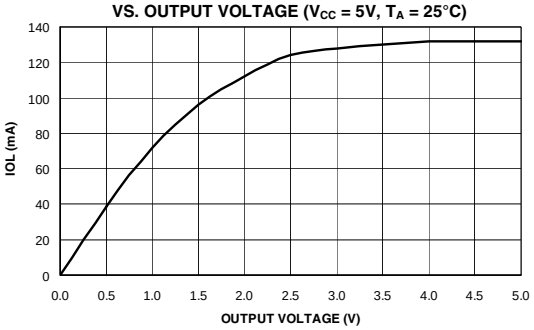
INPUT CURRENT
VS. INPUT VOLTAGE (V_{CC} = 5V, T_A = 25°C)



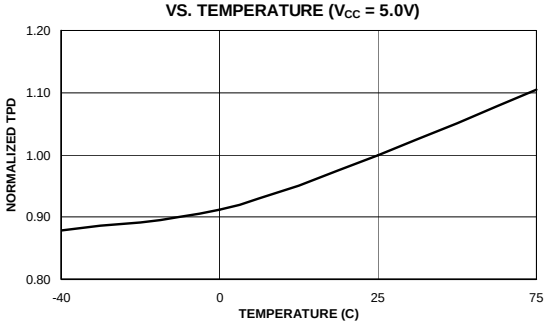
NORMALIZED TSU
VS. SUPPLY VOLTAGE (T_A = 25°C)



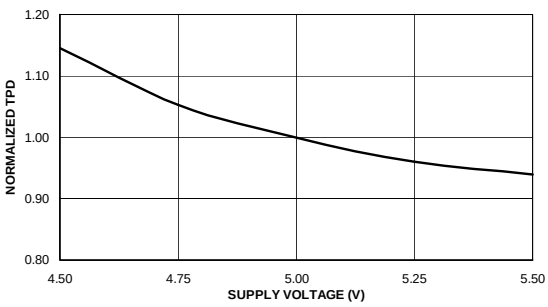
OUTPUT SINK CURRENT
VS. OUTPUT VOLTAGE (V_{CC} = 5V, T_A = 25°C)



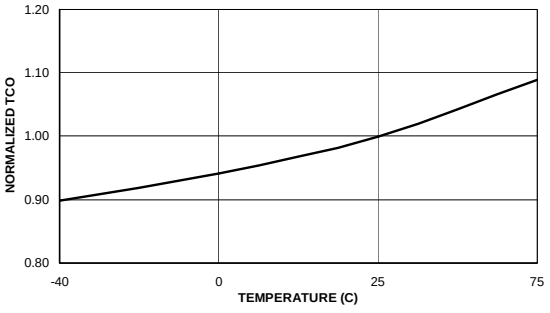
NORMALIZED TPD
VS. TEMPERATURE (V_{CC} = 5.0V)



NORMALIZED TPD
VS. SUPPLY VOLTAGE (T_A = 25°C)



NORMALIZED TCO
VS. TEMPERATURE (V_{CC} = 5.0V)



AC Characteristics (1)

		-7		-10		-15		-20		-25		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
t_{PD1}	Input or Feedback to Non-registered Output		7.5		10	3	15		20		25	ns
t_{PD2}	I/O Input or Feedback to Non-registered Feedback		7		9	3	12		16		20	ns
t_{SU}	Global Clock Setup Time	6		7		11		16		20		ns
t_{H}	Global Clock Hold Time	0		0		0		0		0		ns
t_{FSU}	Global Clock Setup Time of Fast Input	3		3		3		3		3		ns
t_{FH}	Global Clock Hold Time of Fast Input	0.5		0.5		1.0		1.5		2		MHz
t_{COP}	Global Clock to Output Delay		4.5		5		8		10		13	ns
t_{CH}	Global Clock High Time	3		4		5		6		7		ns
t_{CL}	Global Clock Low Time	3		4		5		6		7		ns
t_{ASU}	Array Clock Setup Time	3		3		4		4		5		ns
t_{AH}	Array Clock Hold Time	2		3		4		5		6		ns
t_{ACOP}	Array Clock Output Delay		7.5		10		15		20		25	ns
t_{ACH}	Array Clock High Time	3		4		6		8		10		ns
t_{ACL}	Array Clock Low Time	3		4		6		8		10		ns
t_{CNT}	Minimum Clock Global Period		8		10		13		17		22	ns
f_{CNT}	Maximum Internal Global Clock Frequency	125		100		76.9		66		50		MHz
t_{ACNT}	Minimum Array Clock Period		8		10		13		17		22	ns
f_{ACNT}	Maximum Internal Array Clock Frequency	125		100		76.9		66		50		MHz
f_{MAX}	Maximum Clock Frequency	166.7		125		100		41.7		33.3		MHz
t_{IN}	Input Pad and Buffer Delay		0.5		0.5		2		2		2	ns
t_{IO}	I/O Input Pad and Buffer Delay		0.5		0.5		2		2		2	ns
t_{FIN}	Fast Input Delay		1		1		2		2		2	ns
t_{SEXP}	Foldback Term Delay		4		5		8		10		12	ns
t_{PEXP}	Cascade Logic Delay		0.8		0.8		1		1		1.2	ns
t_{LAD}	Logic Array Delay		3		5		6		7		8	ns
t_{LAC}	Logic Control Delay		3		5		6		7		8	ns
t_{IOE}	Internal Output Enable Delay		2		2		3		3		4	ns
t_{OD1}	Output Buffer and Pad Delay											

AC Characteristics (Continued)[1]

Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{OD2}	Output Buffer and Pad Delay (Slow slew rate = OFF; V_{CCIO} = 3.3V; C_L = 35 pF)		2.5		2.0		5		6		7	ns
t_{OD3}	Output Buffer and Pad Delay (Slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L = 35 pF)		5		5.5		8		10		12	ns
t_{ZX1}	Output Buffer Enable Delay (Slow slew rate = OFF; V_{CCIO} = 5.0V; C_L = 35 pF)		4.0		5.0		7		9		10	ns
t_{ZX2}	Output Buffer Enable Delay (Slow slew rate = OFF; V_{CCIO} = 3.3V; C_L = 35 pF)		4.5		5.5		7		9		10	ns
t_{ZX3}	Output Buffer Enable Delay (Slow slew rate = ON; V_{CCIO} = 5.0V/3.3V; C_L = 35 pF)		9		9		10		11		12	ns
t_{XZ}	Output Buffer Disable Delay (C_L = 5 pF)		4		5		6		7		8	ns
t_{SU}	Register Setup Time	3		2		4		5		6		ns
t_{H}	Register Hold Time	2		3		4		5		6		ns
t_{FSU}	Register Setup Time of Fast Input	3		3		2		2		3		ns
t_{FH}	Register Hold Time of Fast Input	0.5		0.5		2		2		2.5		ns
t_{RD}	Register Delay		1		2		1		2		2	ns
t_{COMB}	Combinatorial Delay		1		2		1		2		2	ns
t_{IC}	Array Clock Delay		3		5		6		7		8	ns
t_{EN}	Register Enable Time		3		5		6		7		8	ns
t_{GLOB}	Global Control Delay		1		1		1		1		1	ns
t_{PRE}	Register Preset Time		2		3		4		5		6	ns
t_{CLR}	Register Clear Time		2		3		4		5		6	ns
t_{UIM}	Switch Matrix Delay		1		1		2		2		2	ns
t_{RPA}	Reduced-power Adder[2]		10		11		13		14		15	ns

Notes: 1. See ordering information for valid part numbers.
2. The t_{RPA} parameter must be added to the t_{LAD}, t_{LAC},t_{TIC}, t_{ACL}, and t_{SEXP} parameters for macrocells running in the reduced-power mode.

ATF1508AS Dedicated Pinouts

Dedicated Pin	84-lead J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP
INPUT/OE2/GCLK2	2	92	90	142
INPUT/GCLR	1	91	89	141
INPUT/OE1	84	90	88	140
INPUT/GCLK1	83	89	87	139
I/O /GCLK3	81	87	85	137
I/O / PD (1, 2)	12,45	3,43	1,41	63,159
I/O / TDI(JTAG)	14	6	4	9
I/O / TMS(JTAG)	23	17	15	22
I/O / TCK(JTAG)	62	64	62	99
I/O / TDO(JTAG)	71	75	73	112
GND	7,19,32,42, 47,59,72,82	13,28,40,45, 61,76,88,97	11,26,38,43, 59,74,86,95	17,42,60,66,95, 113,138,148
VCCINT	3,43	41,93	39,91	61,143
VCCIO	13,26,38, 53,66,78	5,20,36,53,68,84	3,18,34,51,66,82	8,26,55,79,104,133
N/C	–	–	–	1,2,3,4,5,6,7,34,35,36, 37,38,39,40,44,45,46, 47,74,75,76,77,81,82, 83,84,85,86,87,114, 115,116,117,118,119, 120,124,125,126,127, 154,155,156,157
# of SIGNAL PINS	68	84	84	100
# USER I/O PINS	64	80	80	96

OE (1, 2)	Global OE Pins
GCLR	Global Clear Pin
GCLK (1, 2, 3)	Global Clock Pins
PD (1, 2)	Power-down pins
TDI, TMS, TCK, TDO	JTAG pins used for boundary scan testing or in-system programming
GND	Ground Pins
VCCINT	VCC pins for the device (+5V - Internal)
VCCIO	VCC pins for output drivers (for I/O pins) (+5V or 3.3V - I/Os)

ATF1508AS I/O Pinouts

MC	PLB	84-lead J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP	MC	PLB	84-lead J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP
1	A	–	4	2	160	33	C	–	27	25	41
2	A	–	–	–	–	34	C	–	–	–	–
3	A/ **PD1**	12	3	1	159	35	C	31	26	24	33
4	A	–	–	–	158	36	C	–	–	–	32
5	A	11	2	100	153	37	C	30	25	23	31
6	A	10	1	99	152	38	C	29	24	22	30
7	A	–	–	–	–	39	C	–	–	–	–
8	A	9	100	98	151	40	C	28	23	21	29
9	A	–	99	97	150	41	C	–	22	20	28
10	A	–	–	–	–	42	C	–	–	–	–
11	A	8	98	96	149	43	C	27	21	19	27
12	A	–	–	–	147	44	C	–	–	–	25
13	A	6	96	94	146	45	C	25	19	17	24
14	A	5	95	93	145	46	C	24	18	16	23
15	A	–	–	–	–	47	C	–	–	–	–
16	A	4	94	92	144	48	C/ **TMS**	23	17	15	22
17	B	22	16	14	21	49	D	41	39	37	59
18	B	–	–	–	–	50	D	–	–	–	–
19	B	21	15	13	20	51	D	40	38	36	58
20	B	–	–	–	19	52	D	–	–	–	57
21	B	20	14	12	18	53	D	39	37	35	56
22	B	–	12	10	16	54	D	–	35	33	54
23	B	–	–	–	–	55	D	–	–	–	–
24	B	18	11	9	15	56	D	37	34	32	53
25	B	17	10	8	14	57	D	36	33	31	52
26	B	–	–	–	–	58	D	–	–	–	–
27	B	16	9	7	13	59	D	35	32	30	51
28	B	–	–	–	12	60	D	–	–	–	50
29	B	15	8	6	11	61	D	34	31	29	49
30	B	–	7	5	10	62	D	–	30	28	48
31	B	–	–	–	–	63	D	–	–	–	–
32	B/ **TDI**	14	6	4	9	64	D	33	29	27	43
65	E	44	42	40	62	97	G	63	65	63	100

ATF1508ASL Standard Package Options

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
20	12	83.3	ATF1508ASL-20 JC84	84J	Commercial (0°C to 70°C)
			ATF1508ASL-20 QC100	100Q1	
			ATF1508ASL-20 AC100	100A	
			ATF1508ASL-20 QC160	160Q1	
25	15	70	ATF1508ASL-25 JI84	84J	Industrial (-40°C to +85°C)
			ATF1508ASL-25 QI100	100Q1	
			ATF1508ASL-25 AI100	100A	
			ATF1508ASL-25 QI160	160Q1	

Note: 1. The last time buy is Sept. 30, 2005 for shaded parts.

Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

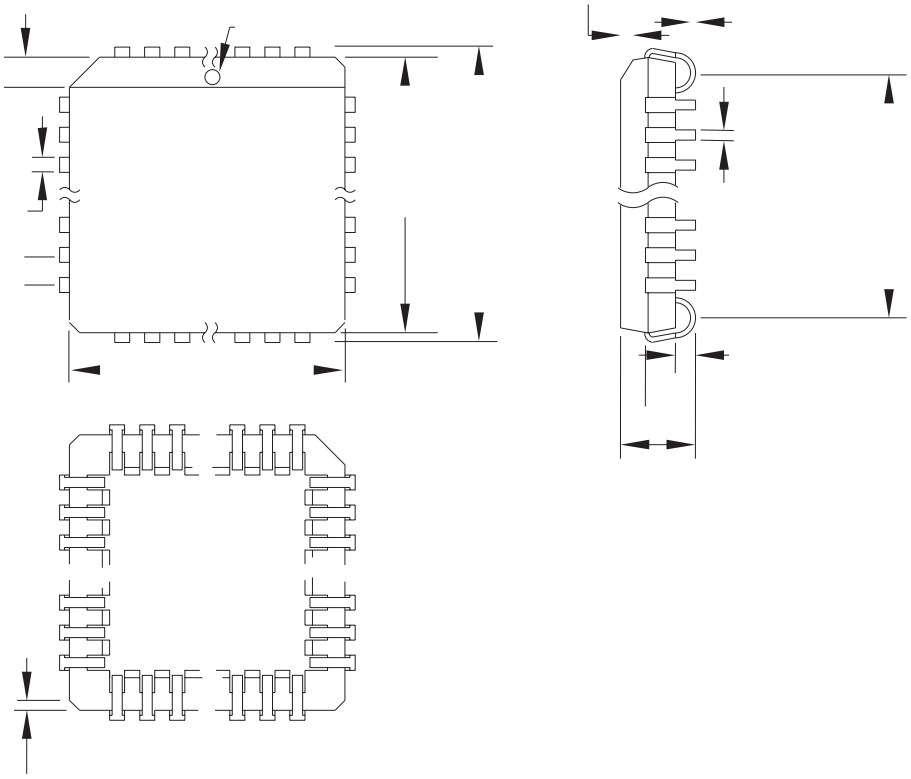
ATF1508ASL Green Package Options (Pb/Halide-free/RoHS Compliant)

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
25	15	70	ATF1508ASL-25 JU84	84J	Industrial (-40°C to +85°C)
			ATF1508ASL-25 AU100	100A	

Package Type	
84J	84-lead, Plastic J-leaded Chip Carrier (PLCC)
100Q1	100-lead, Plastic Quad Pin Flat Package (PQFP)
100A	100-lead, Very Thin Plastic Gull Wing Quad Flat Package (TQFP)
160Q1	160-lead, Plastic Quad Pin Flat Package (PQFP)

Package Information

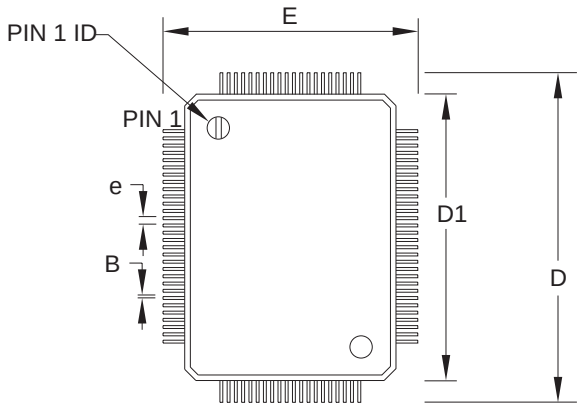
84J – PLCC

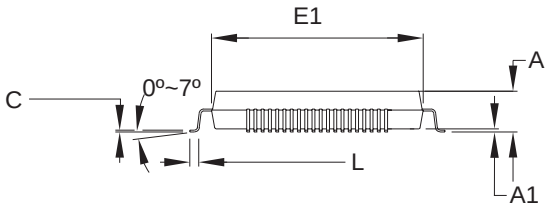


10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**84J**, 84-lead, Plastic J-leaded Chip Carrier (PLCC)	84J	B

100Q1 – PQFP





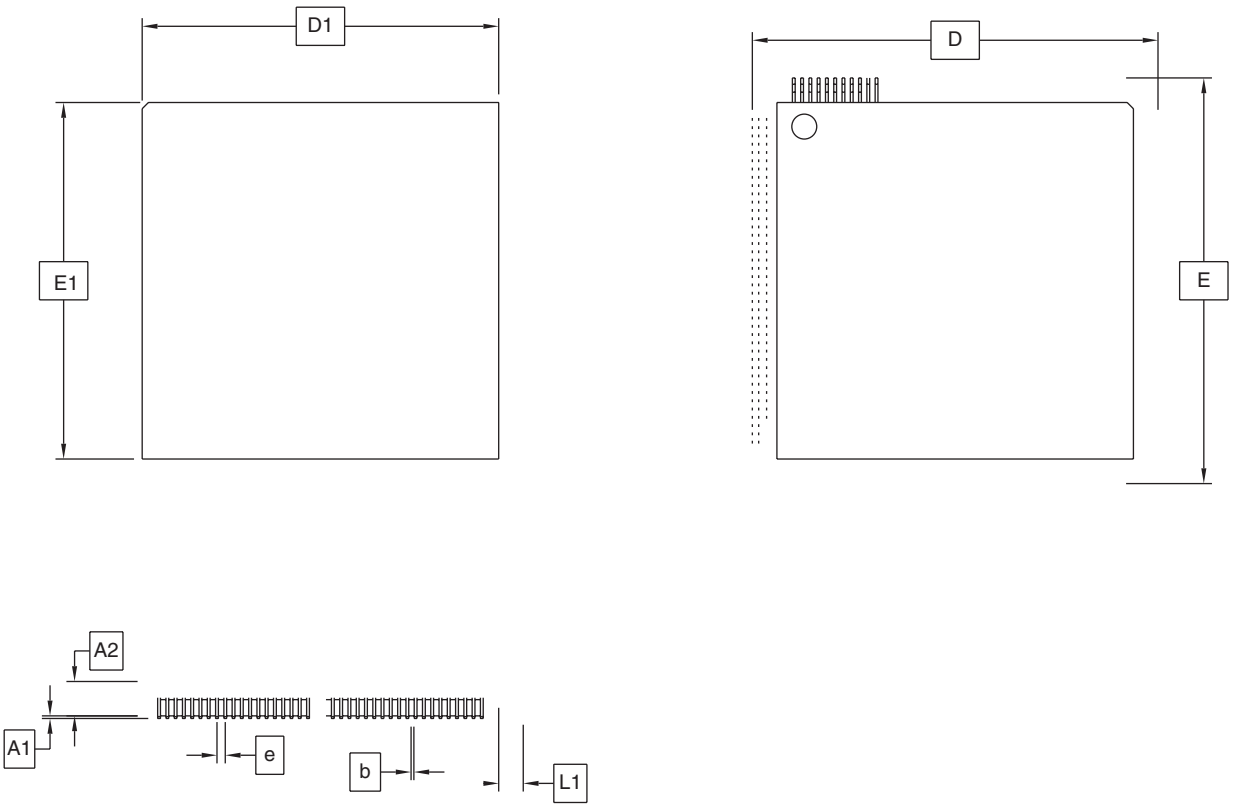
COMMON DIMENSIONS
(Unit of Measure = mm)
JEDEC STANDARD MS-022, GC-1

SYMBOL	MIN	NOM	MAX	NOTE
A	–	3.04	3.4	
A1	0.25	0.33	0.5	
D		23.20 BSC		
E		17.20 BSC		
E1		14.00 BSC		
B	0.22	–	0.40	
C	0.11	–	0.23	
D1		20 BSC		
L	0.73	–	1.03	
e		0.65 BSC		

07/6/2005

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**100Q1**, 100-lead, 14 x 20 mm Body, 3.2 mm Footprint, 0.65 mm Pitch, Plastic Quad Flat Package (PQFP)	100Q1	C

160Q1 – PQFP



3/28/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**160Q1,** 160-lead, 28 x 28 mm Body, 3.2 Form Opt., Plastic Quad Flat Pack (PQFP)	160Q1	A

Revision History

Revision	Comments
0784P	Green package options added.
0784O	The ATF1508ASL-25 commercial speed offering was obsoleted in 2002 and replaced by the ATF1508ASL-20 commercial speed grade.

0784P–PLD–7/05 xM