

Welcome to [E-XFL.COM](https://www.e-xfl.com)

### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

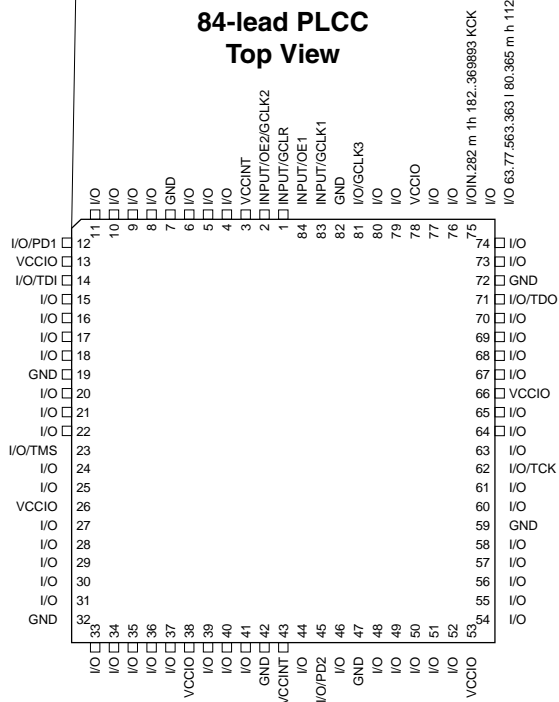
### Applications of Embedded - CPLDs

#### Details

Product Status	Active
Programmable Type	In System Programmable (min 10K program/erase cycles)
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	64
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/atf1508as-7jx84">https://www.e-xfl.com/product-detail/microchip-technology/atf1508as-7jx84</a>



## 84-lead PLCC Top View



## 100-lead TQFP Top View



**Flip-flop**

The ATF1508AS's flip-flop has very flexible data and control functions. The data input can come from either the XOR gate, from a separate product term or directly from the I/O pin. Selecting the separate product term allows creation of a buried registered feedback within a combinatorial output macrocell. (This feature is automatically implemented by the fitter software). In addition to D, T, JK and SR operation, the flip-flop can also be configured as a flow-through latch. In this mode, data passes through when the clock is high and is latched when the clock is low.

The clock itself can be either the Global CLK Signal (GCK) or an individual product term. The flip-flop changes state on the clock's rising edge. When the GCK signal is used as the clock, one of the macrocell product terms can be selected as a clock enable. When the clock enable function is active and the enable signal (product term) is low, all clock edges are ignored. The flip-flop's asynchronous reset signal (AR) can be either the Global Clear (GCLEAR), a product term, or always off. AR can also be a logic OR of GCLEAR with a product term. The asynchronous preset (AP) can be a product term or always off.

**Extra Feedback**

The ATF15xxSE Family macrocell output can be selected as registered or combinatorial. The extra buried feedback signal can be either combinatorial or a registered signal regardless of whether the output is combinatorial or registered. (This enhancement function is automatically implemented by the fitter software.) Feedback of a buried combinatorial output allows the creation of a second latch within a macrocell.

**I/O Control**

The output enable multiplexer (MOE) controls the output enable signal. Each I/O can be individually configured as an input, output or for bi-directional operation. The output enable for each macrocell can be selected from the true or compliment of the two output enable pins, a subset of the I/O pins, or a subset of the I/O macrocells. This selection is automatically done by the fitter software when the I/O is configured as an input, all macrocell resources are still available, including the buried feedback, expander and cascade logic.

**Global Bus/Switch Matrix**

The global bus contains all input and I/O pin signals as well as the buried feedback signal from all 128 macrocells. The switch matrix in each logic block receives as its inputs all signals from the global bus. Under software control, up to 40 of these signals can be selected as inputs to the logic block.

**Foldback Bus**

Each macrocell also generates a foldback product term. This signal goes to the regional bus and is available to 16 macrocells. The foldback is an inverse polarity of one of the macrocell's product terms. The 16 foldback terms in each region allows generation of high fan-in sum terms (up to 21 product terms) with a little additional delay.

**3.3V or 5.0V I/O Operation**

The ATF1508AS device has two sets of  $V_{CC}$  pins viz,  $V_{CCINT}$  and  $V_{CCIO}$ .  $V_{CCINT}$  pins must always be connected to a 5.0V power supply.  $V_{CCINT}$  pins are for input buffers and are "compatible" with both 3.3V and 5.0V inputs.  $V_{CCIO}$  pins are for I/O output drives and can be connected for 3.3/5.0V power supply.

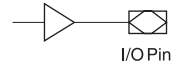
**Open-collector Output Option**

This option enables the device output to provide control signals such as an interrupt that can be asserted by any of the several devices.

**Figure 1. ATF1508AS Macrocell**

SWITCH REGIONAL  
F●

D/T/L



SLEW  
RATE

OPEN COLLECTOR  
OPTION

MACROCELL REDUCED POWER BIT

## Programmable Pin-keeper Option for Inputs and I/Os

The ATF1508AS offers the option of programming all input and I/O pins so that “pin-keeper” circuits can be utilized. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high- or low-level. This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

## Input Diagram



## BSC Configuration Pins and Macrocells (Except JTAG TAP Pins)

Dedic

To Internal

D

TDO

TDI

(From Next Register)

Note: The ATF1508AS has a pull-up option on TMS and TDI pins. This feature is selected as a design option.

## BSC Configuration for Macrocell

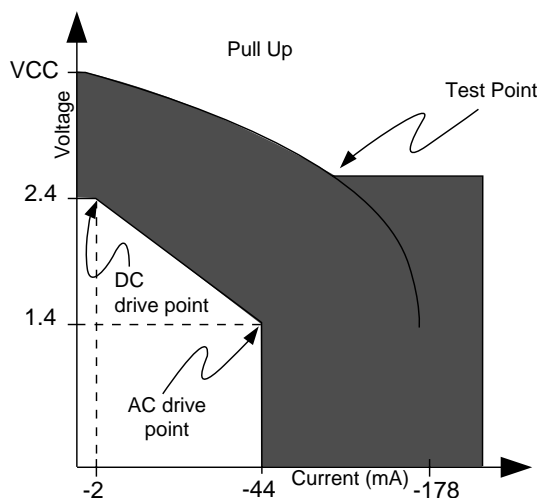
## Boundary Scan Definition Language (BSDL) Models for the ATF1508

These are now available in all package types via the Atmel Web Site. These models can be used for Boundary-scan Test Operation in the ATF1508AS and have been scheduled to conform to the IEEE 1149.1 standard.

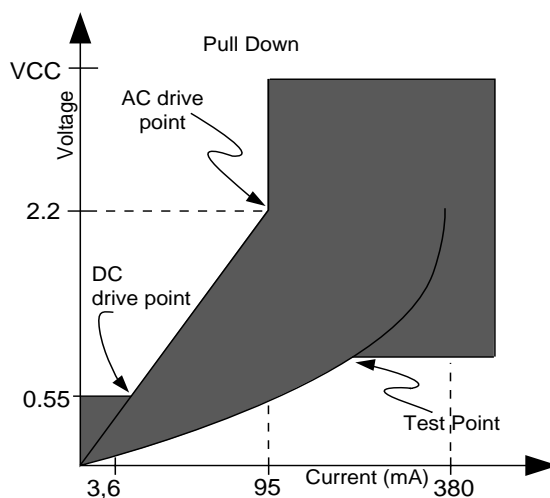
## PCI Compliance

The ATF1508AS also supports the growing need in the industry to support the new Peripheral Component Interconnect (PCI) interface standard in PCI-based designs and specifications. The PCI interface calls for high current drivers, which are much larger than the traditional TTL drivers.

## PCI Voltage-to-current Curves for +5V Signaling in Pull-up Mode



## PCI Voltage-to-current Curves for +5V Signaling in Pull-down Mode



## Power-down Mode

The ATF1508AS includes two pins for optional pin-controlled power-down feature. When this mode is enabled, the PD pin acts as the power-down pin. When the PD1 and PD2 pin is high, the device supply current is reduced to less than 10 mA. During power-down, all output data and internal logic states are latched and held. Therefore, all registered and combinatorial output data remain valid. Any outputs that were in a high-Z state at the onset will remain at high-Z. During power-down, all input signals except the power-down pin are blocked. Input and I/O hold latches remain active to ensure that pins do not float to indeterminate levels, further reducing system power. The power-down pin feature is enabled in the logic design file. Designs using either power-down pin may not use the PD pin logic array input. However, buried logic resources in this macrocell may still be used.

## Power-down AC Characteristics<sup>(1)(2)</sup>

Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{IVDH}$	Valid I, I/O before PD High	7		10		15		20		25		ns
$t_{GVDH}$	Valid OE <sup>(2)</sup> before PD High	7		10		15		20		25		ns
$t_{CVDH}$	Valid Clock <sup>(2)</sup> before PD High	7		10		15		20		25		ns
$t_{DHIX}$	I, I/O Don't Care after PD High		12		15		25		30		35	ns
$t_{DHGX}$	OE <sup>(2)</sup> Don't Care after PD High		12		15		25		30		35	ns
$t_{DHCX}$	Clock <sup>(2)</sup> Don't Care after PD High		12		15		25		30		35	ns
$t_{DLIV}$	PD Low to Valid I, I/O		1		1		1		1		1	μs
$t_{DLGV}$	PD Low to Valid OE (Pin or Term)		1		1		1		1		1	μs
$t_{DLCV}$	PD Low to Valid Clock (Pin or Term)		1		1		1		1		1	μs
$t_{DLOV}$	PD Low to Valid Output		1		1		1		1		1	μs

- Notes: 1. For slow slew outputs, add  $t_{SSO}$ .  
2. Pin or product term.

## Absolute Maximum Ratings\*

Temperature Under Bias.....	-40°C to +85°C
Storage Temperature .....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground .....	-2.0V to +7.0V <sup>(1)</sup>
Voltage on Input Pins with Respect to Ground During Programming.....	-2.0V to +14.0V <sup>(1)</sup>
Programming Voltage with Respect to Ground .....	-2.0V to +14.0V <sup>(1)</sup>

\*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

- Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is  $V_{CC} + 0.75V$  DC, which may overshoot to 7.0V for pulses of less than 20 ns.



## DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Ambient)	0°C - 70°C	-40°C - 85°C
V <sub>CCINT</sub> or V <sub>CCIO</sub> (5V) Power Supply	5V ± 5%	5V ± 10%
V <sub>CCIO</sub> (3.3V) Power Supply	2.7V - 3.6V	2.7V - 3.6V

## DC Characteristics<sup>(1)</sup>

Symbol	Parameter	Condition			Min	Typ	Max	Units
I <sub>IL</sub>	Input or I/O Low Leakage Current	V <sub>IN</sub> = V <sub>CC</sub>				-2	-10	μA
I <sub>IH</sub>	Input or I/O High Leakage Current					2	10	μA
I <sub>OZ</sub>	Tri-state Output Off-state Current	V <sub>O</sub> = V <sub>CC</sub> or GND			-40		40	μA
I <sub>CC1</sub>	Power Supply Current, Standby	V <sub>CC</sub> = Max V <sub>IN</sub> = 0, V <sub>CC</sub>	Std Mode	Com.		160		mA
				Ind.		180		mA
			“L” Mode	Com.		10		μA
				Ind.		10		μA
I <sub>CC2</sub>	Power Supply Current, Power-down Mode	V <sub>CC</sub> = Max V <sub>IN</sub> = 0, V <sub>CC</sub>	“PD” Mode			1	10	mA
I <sub>CC3</sub> <sup>(2)</sup>	Reduced-power Mode Supply Current	V <sub>CC</sub> = Max V <sub>IN</sub> = 0, V <sub>CC</sub>	Std Mode	Com.		65		mA
				Ind.		85		mA
V <sub>CCIO</sub>	Supply Voltage	5.0V Device Output	Com.		4.75		5.25	V
			Ind.		4.5		5.5	V
V <sub>CCIO</sub>	Supply Voltage	3.3V Device Output			3.0		3.6	V
V <sub>IL</sub>	Input Low Voltage				-0.3		0.8	V
V <sub>IH</sub>	Input High Voltage				2.0		V <sub>CCIO</sub> + 0.3	V
V <sub>OL</sub>	Output Low Voltage (TTL)	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>CCIO</sub> = MIN, I <sub>OL</sub> = 12 mA	Com.				0.45	V
			Ind.				0.45	V
	Output Low Voltage (CMOS)	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>CC</sub> = MIN, I <sub>OL</sub> = 0.1 mA	Com.				0.2	V
			Ind.				0.2	V
V <sub>OH</sub>	Output High Voltage (TTL)	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>CCIO</sub> = MIN, I <sub>OH</sub> = -4.0 mA			2.4			V

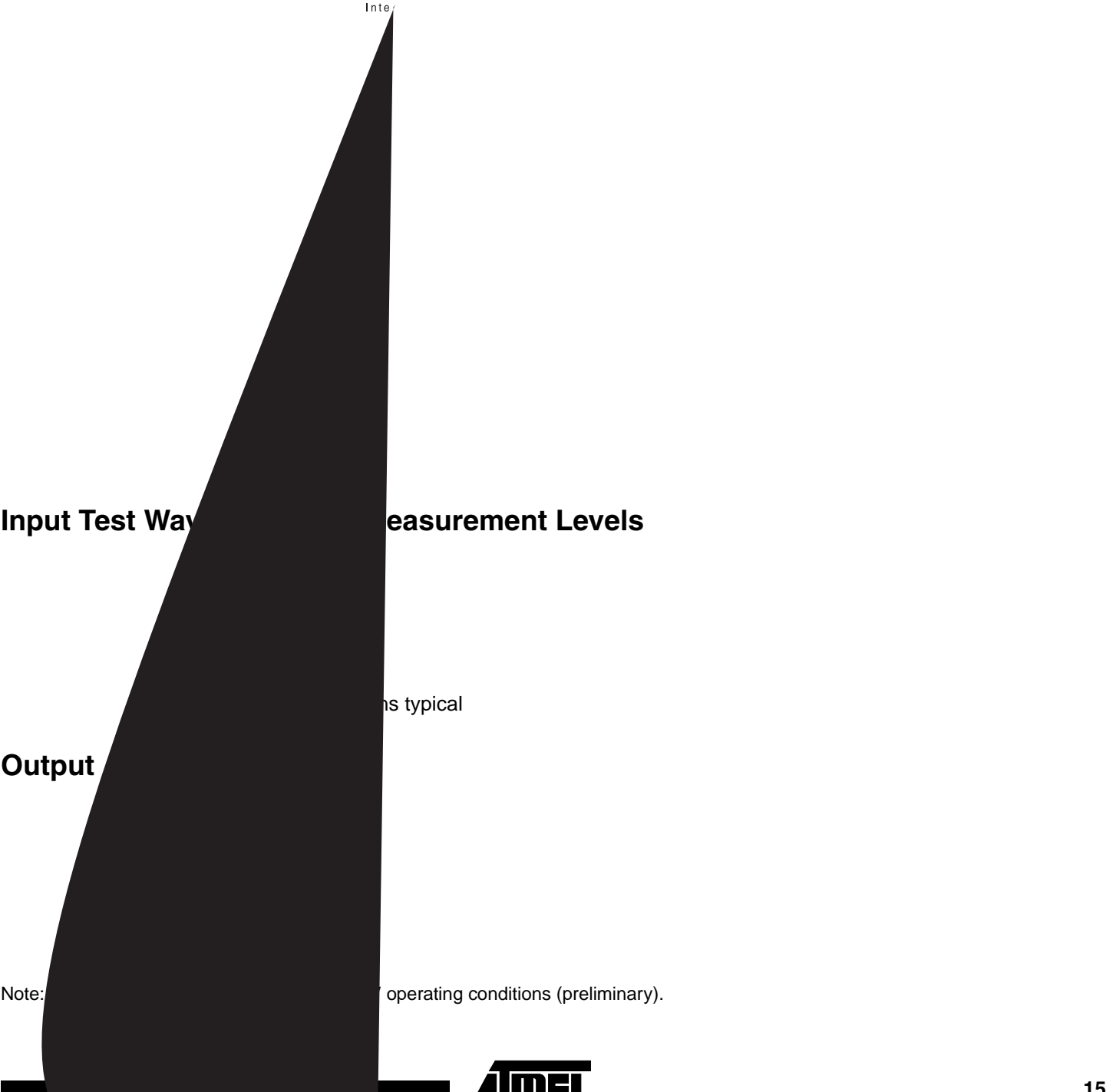
Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.  
2. I<sub>CC3</sub> refers to the current in the reduced-power mode when macrocell reduced-power is turned ON.

Pin Capacitance<sup>(1)</sup>

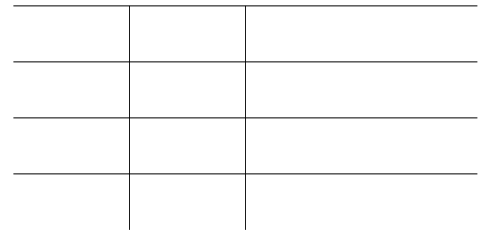
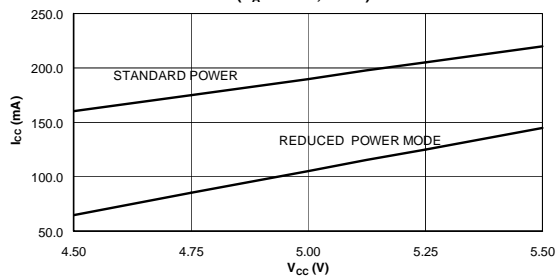
	Typ	Max	Units	Conditions
C <sub>IN</sub>	8	10	pF	V <sub>IN</sub> = 0V; f = 1.0 MHz
C <sub>I/O</sub>	8	10	pF	V <sub>OUT</sub> = 0V; f = 1.0 MHz

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested. The OGI pin (high-voltage pin during programming) has a maximum capacitance of 12 pF.

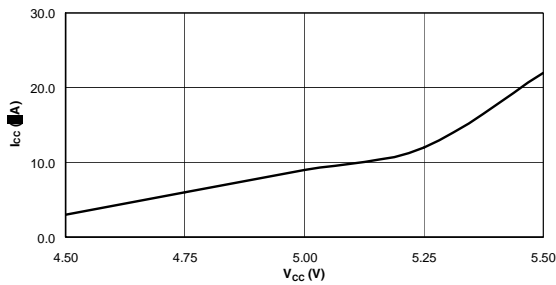
Timing Model



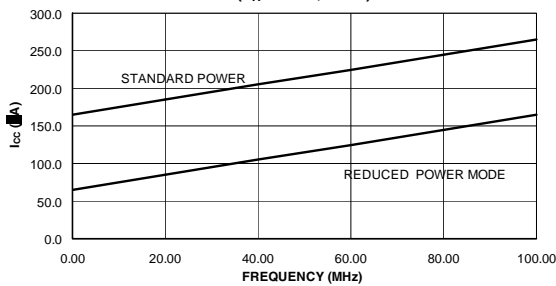
**SUPPLY CURRENT VS. SUPPLY VOLTAGE**  
( $T_A = 25^\circ\text{C}$ ,  $F = 0$ )



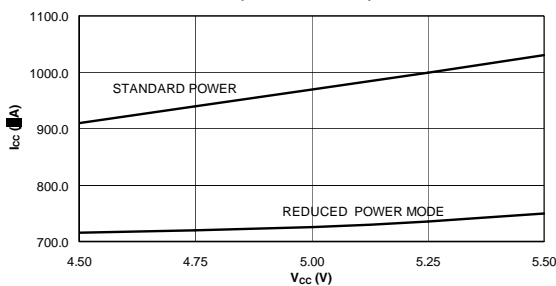
**SUPPLY CURRENT VS. SUPPLY VOLTAGE**  
**LOW-POWER ("L") VERSION**  
( $T_A = 25^\circ\text{C}$ ,  $F = 0$ )

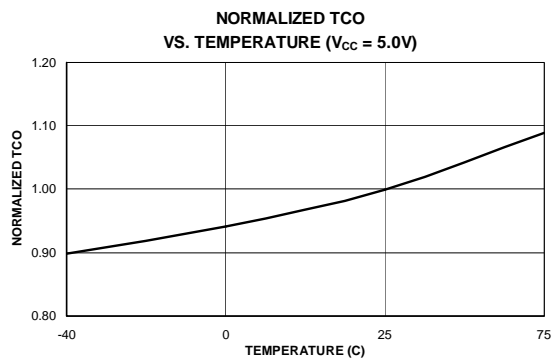
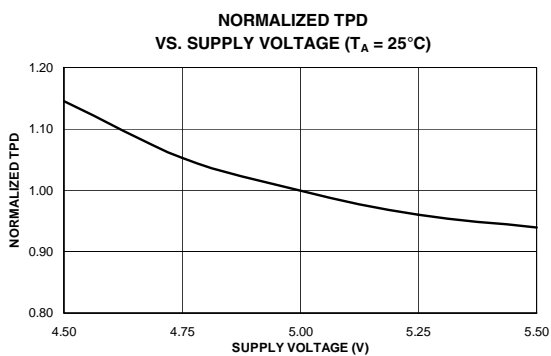
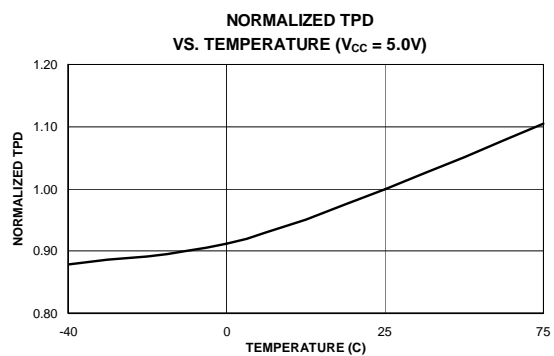
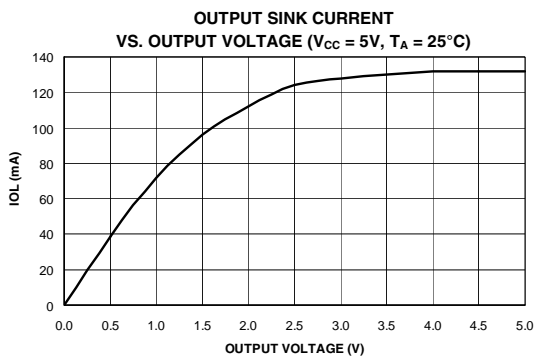
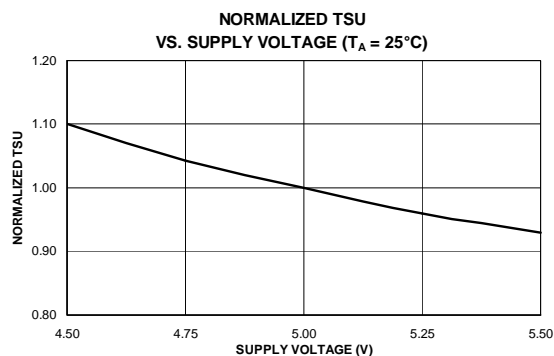
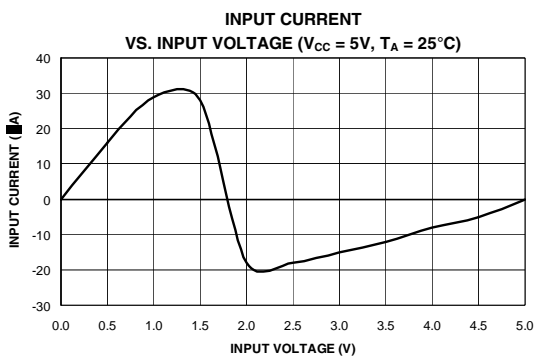
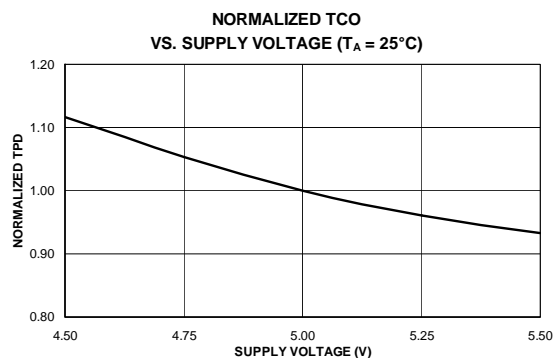
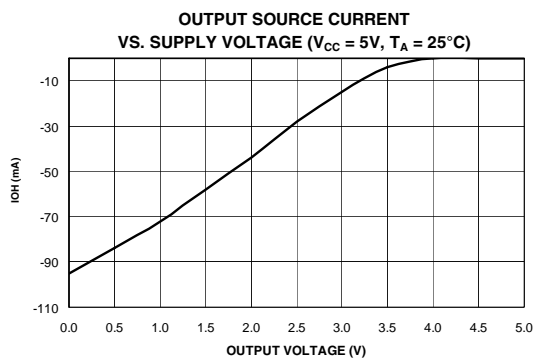


**SUPPLY CURRENT VS. FREQUENCY**  
**STANDARD POWER**  
( $T_A = 25^\circ\text{C}$ ,  $F = 0$ )



**SUPPLY CURRENT VS. SUPPLY VOLTAGE**  
**PIN-CONTROLLED POWER-DOWN MODE**  
( $T_A = 25^\circ\text{C}$ ,  $F = 0$ )





AC Characteristics <sup>(1)</sup>

Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input or Feedback to Non-registered Output		7.5		10	3	15		20		25	ns
t <sub>PD2</sub>	I/O Input or Feedback to Non-registered Feedback		7		9	3	12		16		20	ns
t <sub>SU</sub>	Global Clock Setup Time	6		7		11		16		20		ns
t <sub>H</sub>	Global Clock Hold Time	0		0		0		0		0		ns
t <sub>FSU</sub>	Global Clock Setup Time of Fast Input	3		3		3		3		3		ns
t <sub>FH</sub>	Global Clock Hold Time of Fast Input	0.5		0.5		1.0		1.5		2		MHz
t <sub>COP</sub>	Global Clock to Output Delay		4.5		5		8		10		13	ns
t <sub>CH</sub>	Global Clock High Time	3		4		5		6		7		ns
t <sub>CL</sub>	Global Clock Low Time	3		4		5		6		7		ns
t <sub>ASU</sub>	Array Clock Setup Time	3		3		4		4		5		ns
t <sub>AH</sub>	Array Clock Hold Time	2		3		4		5		6		ns
t <sub>ACOP</sub>	Array Clock Output Delay		7.5		10		15		20		25	ns
t <sub>ACH</sub>	Array Clock High Time	3		4		6		8		10		ns
t <sub>ACL</sub>	Array Clock Low Time	3		4		6		8		10		ns
t <sub>CNT</sub>	Minimum Clock Global Period		8		10		13		17		22	ns
f <sub>CNT</sub>	Maximum Internal Global Clock Frequency	125		100		76.9		66		50		MHz
t <sub>ACNT</sub>	Minimum Array Clock Period		8		10		13		17		22	ns
f <sub>ACNT</sub>	Maximum Internal Array Clock Frequency	125		100		76.9		66		50		MHz
f <sub>MAX</sub>	Maximum Clock Frequency	166.7		125		100		41.7		33.3		MHz
t <sub>IN</sub>	Input Pad and Buffer Delay		0.5		0.5		2		2		2	ns
t <sub>IO</sub>	I/O Input Pad and Buffer Delay		0.5		0.5		2		2		2	ns
t <sub>FIN</sub>	Fast Input Delay		1		1		2		2		2	ns
t <sub>SEXP</sub>	Foldback Term Delay		4		5		8		10		12	ns
t <sub>PEXP</sub>	Cascade Logic Delay		0.8		0.8		1		1		1.2	ns
t <sub>LAD</sub>	Logic Array Delay		3		5		6		7		8	ns
t <sub>LAC</sub>	Logic Control Delay		3		5		6		7		8	ns
t <sub>IOE</sub>	Internal Output Enable Delay		2		2		3		3		4	ns
t <sub>OD1</sub>	Output Buffer and Pad Delay											

## AC Characteristics (Continued)<sup>(1)</sup>

Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{OD2}$	Output Buffer and Pad Delay (Slow slew rate = OFF; $V_{CCIO} = 3.3V$ ; $C_L = 35$ pF)		2.5		2.0		5		6		7	ns
$t_{OD3}$	Output Buffer and Pad Delay (Slow slew rate = ON; $V_{CCIO} = 5V$ or $3.3V$ ; $C_L = 35$ pF)		5		5.5		8		10		12	ns
$t_{ZX1}$	Output Buffer Enable Delay (Slow slew rate = OFF; $V_{CCIO} = 5.0V$ ; $C_L = 35$ pF)		4.0		5.0		7		9		10	ns
$t_{ZX2}$	Output Buffer Enable Delay (Slow slew rate = OFF; $V_{CCIO} = 3.3V$ ; $C_L = 35$ pF)		4.5		5.5		7		9		10	ns
$t_{ZX3}$	Output Buffer Enable Delay (Slow slew rate = ON; $V_{CCIO} = 5.0V/3.3V$ ; $C_L = 35$ pF)		9		9		10		11		12	ns
$t_{XZ}$	Output Buffer Disable Delay ( $C_L = 5$ pF)		4		5		6		7		8	ns
$t_{SU}$	Register Setup Time	3		2		4		5		6		ns
$t_H$	Register Hold Time	2		3		4		5		6		ns
$t_{FSU}$	Register Setup Time of Fast Input	3		3		2		2		3		ns
$t_{FH}$	Register Hold Time of Fast Input	0.5		0.5		2		2		2.5		ns
$t_{RD}$	Register Delay		1		2		1		2		2	ns
$t_{COMB}$	Combinatorial Delay		1		2		1		2		2	ns
$t_{IC}$	Array Clock Delay		3		5		6		7		8	ns
$t_{EN}$	Register Enable Time		3		5		6		7		8	ns
$t_{GLOB}$	Global Control Delay		1		1		1		1		1	ns
$t_{PRE}$	Register Preset Time		2		3		4		5		6	ns
$t_{CLR}$	Register Clear Time		2		3		4		5		6	ns
$t_{UIM}$	Switch Matrix Delay		1		1		2		2		2	ns
$t_{RPA}$	Reduced-power Adder <sup>(2)</sup>		10		11		13		14		15	ns

- Notes: 1. See ordering information for valid part numbers.  
2. The  $t_{RPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{TIC}$ ,  $t_{ACL}$ , and  $t_{SEXP}$  parameters for macrocells running in the reduced-power mode.

## ATF1508AS Dedicated Pinouts

Dedicated Pin	84-lead J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP
INPUT/OE2/GCLK2	2	92	90	142
INPUT/GCLR	1	91	89	141
INPUT/OE1	84	90	88	140
INPUT/GCLK1	83	89	87	139
I/O /GCLK3	81	87	85	137
I/O / PD (1, 2)	12,45	3,43	1,41	63,159
I/O / TDI(JTAG)	14	6	4	9
I/O / TMS(JTAG)	23	17	15	22
I/O / TCK(JTAG)	62	64	62	99
I/O / TDO(JTAG)	71	75	73	112
GND	7,19,32,42, 47,59,72,82	13,28,40,45, 61,76,88,97	11,26,38,43, 59,74,86,95	17,42,60,66,95, 113,138,148
VCCINT	3,43	41,93	39,91	61,143
VCCIO	13,26,38, 53,66,78	5,20,36,53,68,84	3,18,34,51,66,82	8,26,55,79,104,133
N/C	—	—	—	1,2,3,4,5,6,7,34,35,36, 37,38,39,40,44,45,46, 47,74,75,76,77,81,82, 83,84,85,86,87,114, 115,116,117,118,119, 120,124,125,126,127, 154,155,156,157
# of SIGNAL PINS	68	84	84	100
# USER I/O PINS	64	80	80	96

OE (1, 2)	Global OE Pins
GCLR	Global Clear Pin
GCLK (1, 2, 3)	Global Clock Pins
PD (1, 2)	Power-down pins
TDI, TMS, TCK, TDO	JTAG pins used for boundary scan testing or in-system programming
GND	Ground Pins
VCCINT	VCC pins for the device (+5V - Internal)
VCCIO	VCC pins for output drivers (for I/O pins) (+5V or 3.3V - I/Os)

## ATF1508AS I/O Pinouts

MC	PLB	84-lead J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP	MC	PLB	84-lead J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP
1	A	—	4	2	160	33	C	—	27	25	41
2	A	—	—	—	—	34	C	—	—	—	—
3	A/ PD1	12	3	1	159	35	C	31	26	24	33
4	A	—	—	—	158	36	C	—	—	—	32
5	A	11	2	100	153	37	C	30	25	23	31
6	A	10	1	99	152	38	C	29	24	22	30
7	A	—	—	—	—	39	C	—	—	—	—
8	A	9	100	98	151	40	C	28	23	21	29
9	A	—	99	97	150	41	C	—	22	20	28
10	A	—	—	—	—	42	C	—	—	—	—
11	A	8	98	96	149	43	C	27	21	19	27
12	A	—	—	—	147	44	C	—	—	—	25
13	A	6	96	94	146	45	C	25	19	17	24
14	A	5	95	93	145	46	C	24	18	16	23
15	A	—	—	—	—	47	C	—	—	—	—
16	A	4	94	92	144	48	C/ TMS	23	17	15	22
17	B	22	16	14	21	49	D	41	39	37	59
18	B	—	—	—	—	50	D	—	—	—	—
19	B	21	15	13	20	51	D	40	38	36	58
20	B	—	—	—	19	52	D	—	—	—	57
21	B	20	14	12	18	53	D	39	37	35	56
22	B	—	12	10	16	54	D	—	35	33	54
23	B	—	—	—	—	55	D	—	—	—	—
24	B	18	11	9	15	56	D	37	34	32	53
25	B	17	10	8	14	57	D	36	33	31	52
26	B	—	—	—	—	58	D	—	—	—	—
27	B	16	9	7	13	59	D	35	32	30	51
28	B	—	—	—	12	60	D	—	—	—	50
29	B	15	8	6	11	61	D	34	31	29	49
30	B	—	7	5	10	62	D	—	30	28	48
31	B	—	—	—	—	63	D	—	—	—	—
32	B/ TDI	14	6	4	9	64	D	33	29	27	43
65	E	44	42	40	62	97	G	63	65	63	100



## ATF1508ASL Standard Package Options

$t_{PD}$ (ns)	$t_{CO1}$ (ns)	$f_{MAX}$ (MHz)	Ordering Code	Package	Operation Range
20	12	83.3	ATF1508ASL-20 JC84	84J	Commercial (0°C to 70°C)
			ATF1508ASL-20 QC100	100Q1	
			ATF1508ASL-20 AC100	100A	
			ATF1508ASL-20 QC160	160Q1	
25	15	70	ATF1508ASL-25 JI84	84J	Industrial (-40°C to +85°C)
			ATF1508ASL-25 QI100	100Q1	
			ATF1508ASL-25 AI100	100A	
			ATF1508ASL-25 QI160	160Q1	

Note: 1. The last time buy is Sept. 30, 2005 for shaded parts.

## Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

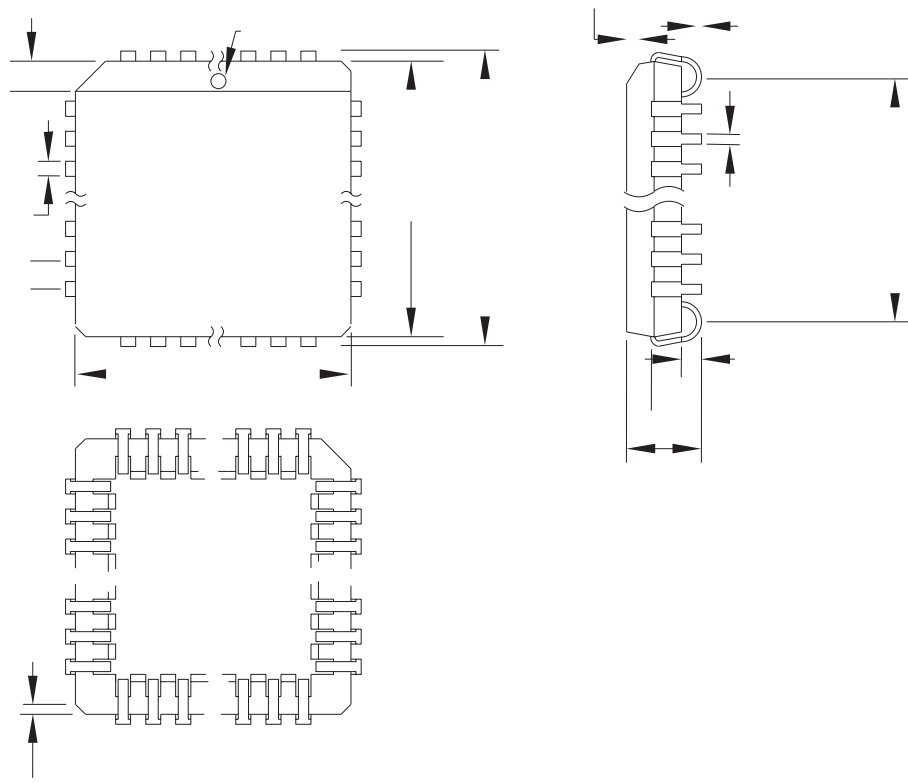
## ATF1508ASL Green Package Options (Pb/Halide-free/RoHS Compliant)

$t_{PD}$ (ns)	$t_{CO1}$ (ns)	$f_{MAX}$ (MHz)	Ordering Code	Package	Operation Range
25	15	70	ATF1508ASL-25 JU84	84J	Industrial (-40°C to +85°C)
			ATF1508ASL-25 AU100	100A	

Package Type	
<b>84J</b>	84-lead, Plastic J-leaded Chip Carrier (PLCC)
<b>100Q1</b>	100-lead, Plastic Quad Pin Flat Package (PQFP)
<b>100A</b>	100-lead, Very Thin Plastic Gull Wing Quad Flat Package (TQFP)
<b>160Q1</b>	160-lead, Plastic Quad Pin Flat Package (PQFP)

# Package Information

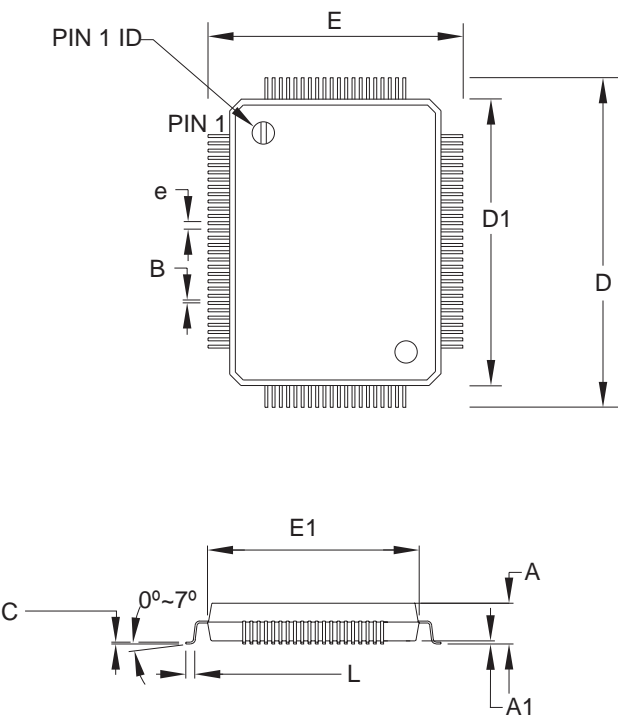
## 84J – PLCC



10/04/01

 2325 Orchard Parkway San Jose, CA 95131	<b>TITLE</b> <b>84J, 84-lead, Plastic J-leaded Chip Carrier (PLCC)</b>	<b>DRAWING NO.</b> 84J	<b>REV.</b> B
--	---	---------------------------	------------------

## 100Q1 – PQFP



**COMMON DIMENSIONS**  
(Unit of Measure = mm)  
JEDEC STANDARD MS-022, GC-1

SYMBOL	MIN	NOM	MAX	NOTE
A	–	3.04	3.4	
A1	0.25	0.33	0.5	
D	23.20 BSC			
E	17.20 BSC			
E1	14.00 BSC			
B	0.22	–	0.40	
C	0.11	–	0.23	
D1	20 BSC			
L	0.73	–	1.03	
e	0.65 BSC			

07/6/2005



2325 Orchard Parkway  
San Jose, CA 95131

### TITLE

**100Q1**, 100-lead, 14 x 20 mm Body, 3.2 mm Footprint, 0.65 mm Pitch,  
Plastic Quad Flat Package (PQFP)

### DRAWING NO.

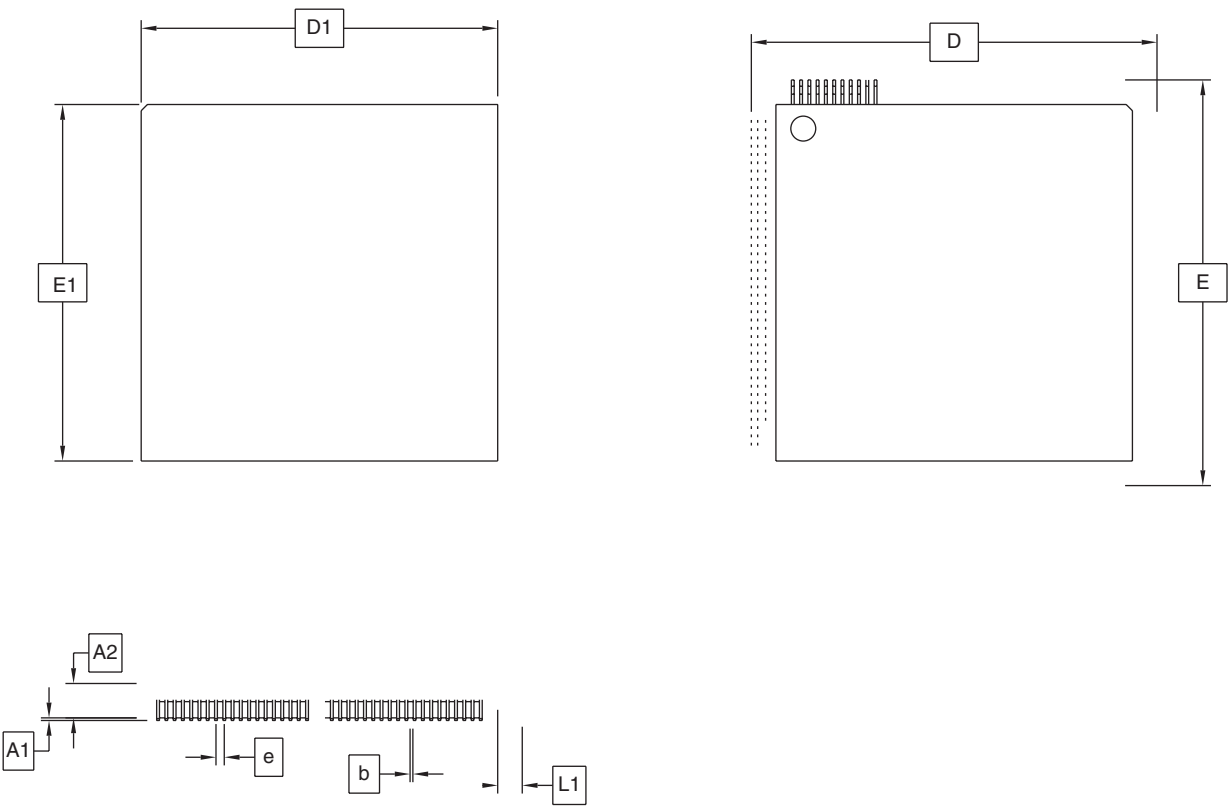
100Q1

### REV.


C



160Q1 – PQFP



3/28/02

 2325 Orchard Parkway San Jose, CA 95131	<b>TITLE</b> <b>160Q1</b> , 160-lead, 28 x 28 mm Body, 3.2 Form Opt., Plastic Quad Flat Pack (PQFP)	<b>DRAWING NO.</b> 160Q1	<b>REV.</b> A
--	---	-----------------------------	------------------



## Revision History

Revision	Comments
0784P	Green package options added.
0784O	The ATF1508ASL-25 commercial speed offering was obsoleted in 2002 and replaced by the ATF1508ASL-20 commercial speed grade.