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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Obsolete
Programmable Type	In System Programmable (min 10K program/erase cycles)
Delay Time tpd(1) Max	20 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	96
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/atf1508asl-20qc160">https://www.e-xfl.com/product-detail/microchip-technology/atf1508asl-20qc160</a>

**Flip-flop**

The ATF1508AS's flip-flop has very flexible data and control functions. The data input can come from either the XOR gate, from a separate product term or directly from the I/O pin. Selecting the separate product term allows creation of a buried registered feedback within a combinatorial output macrocell. (This feature is automatically implemented by the fitter software). In addition to D, T, JK and SR operation, the flip-flop can also be configured as a flow-through latch. In this mode, data passes through when the clock is high and is latched when the clock is low.

The clock itself can be either the Global CLK Signal (GCK) or an individual product term. The flip-flop changes state on the clock's rising edge. When the GCK signal is used as the clock, one of the macrocell product terms can be selected as a clock enable. When the clock enable function is active and the enable signal (product term) is low, all clock edges are ignored. The flip-flop's asynchronous reset signal (AR) can be either the Global Clear (GCLEAR), a product term, or always off. AR can also be a logic OR of GCLEAR with a product term. The asynchronous preset (AP) can be a product term or always off.

**Extra Feedback**

The ATF15xxSE Family macrocell output can be selected as registered or combinatorial. The extra buried feedback signal can be either combinatorial or a registered signal regardless of whether the output is combinatorial or registered. (This enhancement function is automatically implemented by the fitter software.) Feedback of a buried combinatorial output allows the creation of a second latch within a macrocell.

**I/O Control**

The output enable multiplexer (MOE) controls the output enable signal. Each I/O can be individually configured as an input, output or for bi-directional operation. The output enable for each macrocell can be selected from the true or compliment of the two output enable pins, a subset of the I/O pins, or a subset of the I/O macrocells. This selection is automatically done by the fitter software when the I/O is configured as an input, all macrocell resources are still available, including the buried feedback, expander and cascade logic.

**Global Bus/Switch Matrix**

The global bus contains all input and I/O pin signals as well as the buried feedback signal from all 128 macrocells. The switch matrix in each logic block receives as its inputs all signals from the global bus. Under software control, up to 40 of these signals can be selected as inputs to the logic block.

**Foldback Bus**

Each macrocell also generates a foldback product term. This signal goes to the regional bus and is available to 16 macrocells. The foldback is an inverse polarity of one of the macrocell's product terms. The 16 foldback terms in each region allows generation of high fan-in sum terms (up to 21 product terms) with a little additional delay.

**3.3V or 5.0V I/O Operation**

The ATF1508AS device has two sets of  $V_{CC}$  pins viz,  $V_{CCINT}$  and  $V_{CCIO}$ .  $V_{CCINT}$  pins must always be connected to a 5.0V power supply.  $V_{CCINT}$  pins are for input buffers and are "compatible" with both 3.3V and 5.0V inputs.  $V_{CCIO}$  pins are for I/O output drives and can be connected for 3.3/5.0V power supply.

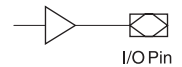
**Open-collector Output Option**

This option enables the device output to provide control signals such as an interrupt that can be asserted by any of the several devices.

**Figure 1. ATF1508AS Macrocell**

SWITCH REGIONAL  
F●

D/T/L



SLEW  
RATE

OPEN COLLECTOR  
OPTION

MACROCELL REDUCED POWER BIT

## Programmable Pin-keeper Option for Inputs and I/Os

The ATF1508AS offers the option of programming all input and I/O pins so that “pin-keeper” circuits can be utilized. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high- or low-level. This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

## Input Diagram



**Design  
Software  
Support**

## **ISP Programming Protection**

The ATF1508AS has a special feature that locks the device and prevents the inputs and I/O from driving if the programming process is interrupted for any reason. The inputs and I/O default to high-Z state during such a condition. In addition the pin-keeper option preserves the former state during device programming.

All ATF1508AS devices are initially shipped in the erased state thereby making them ready to use for ISP.

Note: For more information refer to the "Designing for In-System Programmability with Atmel CPLDs" application note.

## **JTAG-BST Overview**

The JTAG boundary-scan testing is controlled by the Test Access Port (TAP) controller in the ATF1508AS. The boundary-scan technique involves the inclusion of a shift-register stage (contained in a boundary-scan cell) adjacent to each component so that signals at component boundaries can be controlled and observed using scan testing principles. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary-scan testing. The ATF1508AS does not currently include a Test Reset (TRST) input pin because the TAP controller is automatically reset at power-up. The six JTAG BST modes supported include: SAMPLE/PRELOAD, EXTEST, BYPASS and IDCODE. BST on the ATF1508AS is implemented using the Boundary-scan Definition Language (BSDL) described in the JTAG specification (IEEE Standard 1149.1). Any third-party tool that supports the BSDL format can be used to perform BST on the ATF1508AS.

The ATF1508AS also has the option of using four JTAG-standard I/O pins for In-System programming (ISP). The ATF1508AS is programmable through the four JTAG pins using programming compatible with the IEEE JTAG Standard 1149.1. Programming is performed by using 5V TTL-level programming signals from the JTAG ISP interface. The JTAG feature is a programmable option. If JTAG (BST or ISP) is not needed, then the four JTAG control pins are available as I/O pins.

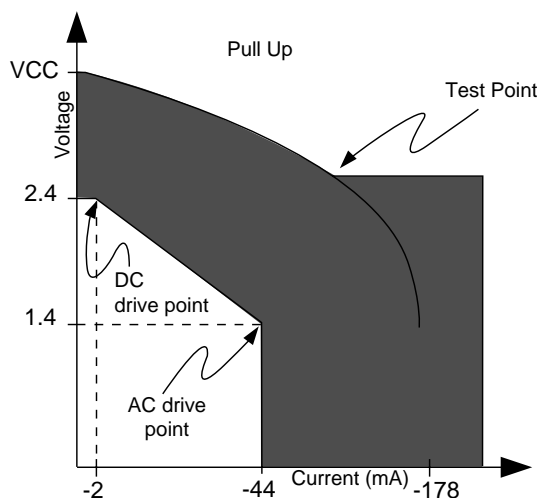
## **JTAG Boundary-scan Cell (BSC) Testing**

The ATF1508AS contains up to 96 I/O pins and four input pins, depending on the device type and package type selected. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary-scan testing as described in detail by IEEE Standard 1149.1. A typical BSC consists of three capture registers or scan registers and up to two update registers. There are two types of BSCs, one for input or I/O pin, and one for the macrocells. The BSCs in the device are chained together through the (BST) capture registers. Input to the capture register chain is fed in from the TDI pin while the output is directed to the TDO pin. Capture registers are used to capture active device data signals, to shift data in and out of the device and to load data into the update registers. Control signals are generated internally by the JTAG TAP controller. The BSC configuration for the input and I/O pins and macrocells are shown below.

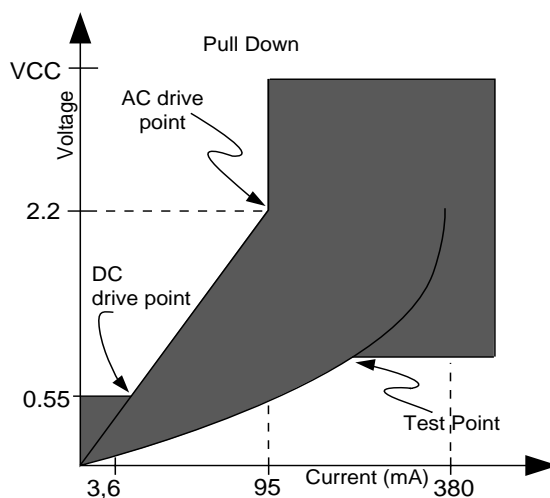
## PCI Compliance

The ATF1508AS also supports the growing need in the industry to support the new Peripheral Component Interconnect (PCI) interface standard in PCI-based designs and specifications. The PCI interface calls for high current drivers, which are much larger than the traditional TTL drivers.

## PCI Voltage-to-current Curves for +5V Signaling in Pull-up Mode



## PCI Voltage-to-current Curves for +5V Signaling in Pull-down Mode



## PCI DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
$V_{CC}$	Supply Voltage		4.75	5.25	V
$V_{IH}$	Input High Voltage		2.0	$V_{CC} + 0.5$	V
$V_{IL}$	Input Low Voltage		-0.5	0.8	V
$I_{IH}$	Input High Leakage Current <sup>(1)</sup>	$V_{IN} = 2.7V$		70	$\mu A$
$I_{IL}$	Input Low Leakage Current <sup>(1)</sup>	$V_{IN} = 0.5V$		-70	$\mu A$
$V_{OH}$	Output High Voltage	$I_{OUT} = -2\text{ mA}$	2.4		V
$V_{OL}$	Output Low Voltage	$I_{OUT} = 3\text{ mA}, 6\text{ mA}$		0.55	V
$C_{IN}$	Input Pin Capacitance			10	pF
$C_{CLK}$	CLK Pin Capacitance			12	pF
$C_{IDSEL}$	IDSEL Pin Capacitance			8	pF
$L_{PIN}$	Pin Inductance			20	nH

Note: 1. Leakage current is without pin-keeper off.

## PCI AC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
$I_{OH(AC)}$	Switching	$0 < V_{OUT} \leq 1.4$	-44		mA
	Current High	$1.4 < V_{OUT} < 2.4$	$-44 + (V_{OUT} - 1.4)/0.024$		mA
		$3.1 < V_{OUT} < V_{CC}$	Equation A <sup>(1)</sup>		mA

Notes: 1. Equation A:  $I_{OH} = 11.9 (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$  for  $V_{CC} > V_{OUT} > 3.1V$ .  
2. Equation B:  $I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$  for  $0V < V_{OUT} < 0.71V$ .

## Power-down Mode

The ATF1508AS includes two pins for optional pin-controlled power-down feature. When this mode is enabled, the PD pin acts as the power-down pin. When the PD1 and PD2 pin is high, the device supply current is reduced to less than 10 mA. During power-down, all output data and internal logic states are latched and held. Therefore, all registered and combinatorial output data remain valid. Any outputs that were in a high-Z state at the onset will remain at high-Z. During power-down, all input signals except the power-down pin are blocked. Input and I/O hold latches remain active to ensure that pins do not float to indeterminate levels, further reducing system power. The power-down pin feature is enabled in the logic design file. Designs using either power-down pin may not use the PD pin logic array input. However, buried logic resources in this macrocell may still be used.

## Power-down AC Characteristics<sup>(1)(2)</sup>

Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{IVDH}$	Valid I, I/O before PD High	7		10		15		20		25		ns
$t_{GVDH}$	Valid OE <sup>(2)</sup> before PD High	7		10		15		20		25		ns
$t_{CVDH}$	Valid Clock <sup>(2)</sup> before PD High	7		10		15		20		25		ns
$t_{DHIX}$	I, I/O Don't Care after PD High		12		15		25		30		35	ns
$t_{DHGX}$	OE <sup>(2)</sup> Don't Care after PD High		12		15		25		30		35	ns
$t_{DHCX}$	Clock <sup>(2)</sup> Don't Care after PD High		12		15		25		30		35	ns
$t_{DLIV}$	PD Low to Valid I, I/O		1		1		1		1		1	μs
$t_{DLGV}$	PD Low to Valid OE (Pin or Term)		1		1		1		1		1	μs
$t_{DLCV}$	PD Low to Valid Clock (Pin or Term)		1		1		1		1		1	μs
$t_{DLOV}$	PD Low to Valid Output		1		1		1		1		1	μs

- Notes: 1. For slow slew outputs, add  $t_{SSO}$ .  
2. Pin or product term.

## Absolute Maximum Ratings\*

Temperature Under Bias.....	-40°C to +85°C
Storage Temperature .....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground .....	-2.0V to +7.0V <sup>(1)</sup>
Voltage on Input Pins with Respect to Ground During Programming.....	-2.0V to +14.0V <sup>(1)</sup>
Programming Voltage with Respect to Ground .....	-2.0V to +14.0V <sup>(1)</sup>

\*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

- Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is  $V_{CC} + 0.75V$  DC, which may overshoot to 7.0V for pulses of less than 20 ns.

## DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Ambient)	0°C - 70°C	-40°C - 85°C
V <sub>CCINT</sub> or V <sub>CCIO</sub> (5V) Power Supply	5V ± 5%	5V ± 10%
V <sub>CCIO</sub> (3.3V) Power Supply	2.7V - 3.6V	2.7V - 3.6V

## DC Characteristics<sup>(1)</sup>

Symbol	Parameter	Condition			Min	Typ	Max	Units
I <sub>IL</sub>	Input or I/O Low Leakage Current	V <sub>IN</sub> = V <sub>CC</sub>				-2	-10	μA
I <sub>IH</sub>	Input or I/O High Leakage Current					2	10	μA
I <sub>OZ</sub>	Tri-state Output Off-state Current	V <sub>O</sub> = V <sub>CC</sub> or GND			-40		40	μA
I <sub>CC1</sub>	Power Supply Current, Standby	V <sub>CC</sub> = Max V <sub>IN</sub> = 0, V <sub>CC</sub>	Std Mode	Com.		160		mA
				Ind.		180		mA
			“L” Mode	Com.		10		μA
				Ind.		10		μA
I <sub>CC2</sub>	Power Supply Current, Power-down Mode	V <sub>CC</sub> = Max V <sub>IN</sub> = 0, V <sub>CC</sub>	“PD” Mode			1	10	mA
I <sub>CC3</sub> <sup>(2)</sup>	Reduced-power Mode Supply Current	V <sub>CC</sub> = Max V <sub>IN</sub> = 0, V <sub>CC</sub>	Std Mode	Com.		65		mA
				Ind.		85		mA
V <sub>CCIO</sub>	Supply Voltage	5.0V Device Output	Com.		4.75		5.25	V
			Ind.		4.5		5.5	V
V <sub>CCIO</sub>	Supply Voltage	3.3V Device Output			3.0		3.6	V
V <sub>IL</sub>	Input Low Voltage				-0.3		0.8	V
V <sub>IH</sub>	Input High Voltage				2.0		V <sub>CCIO</sub> + 0.3	V
V <sub>OL</sub>	Output Low Voltage (TTL)	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>CCIO</sub> = MIN, I <sub>OL</sub> = 12 mA	Com.				0.45	V
			Ind.				0.45	V
	Output Low Voltage (CMOS)	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>CC</sub> = MIN, I <sub>OL</sub> = 0.1 mA	Com.				0.2	V
			Ind.				0.2	V
V <sub>OH</sub>	Output High Voltage (TTL)	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>CCIO</sub> = MIN, I <sub>OH</sub> = -4.0 mA			2.4			V

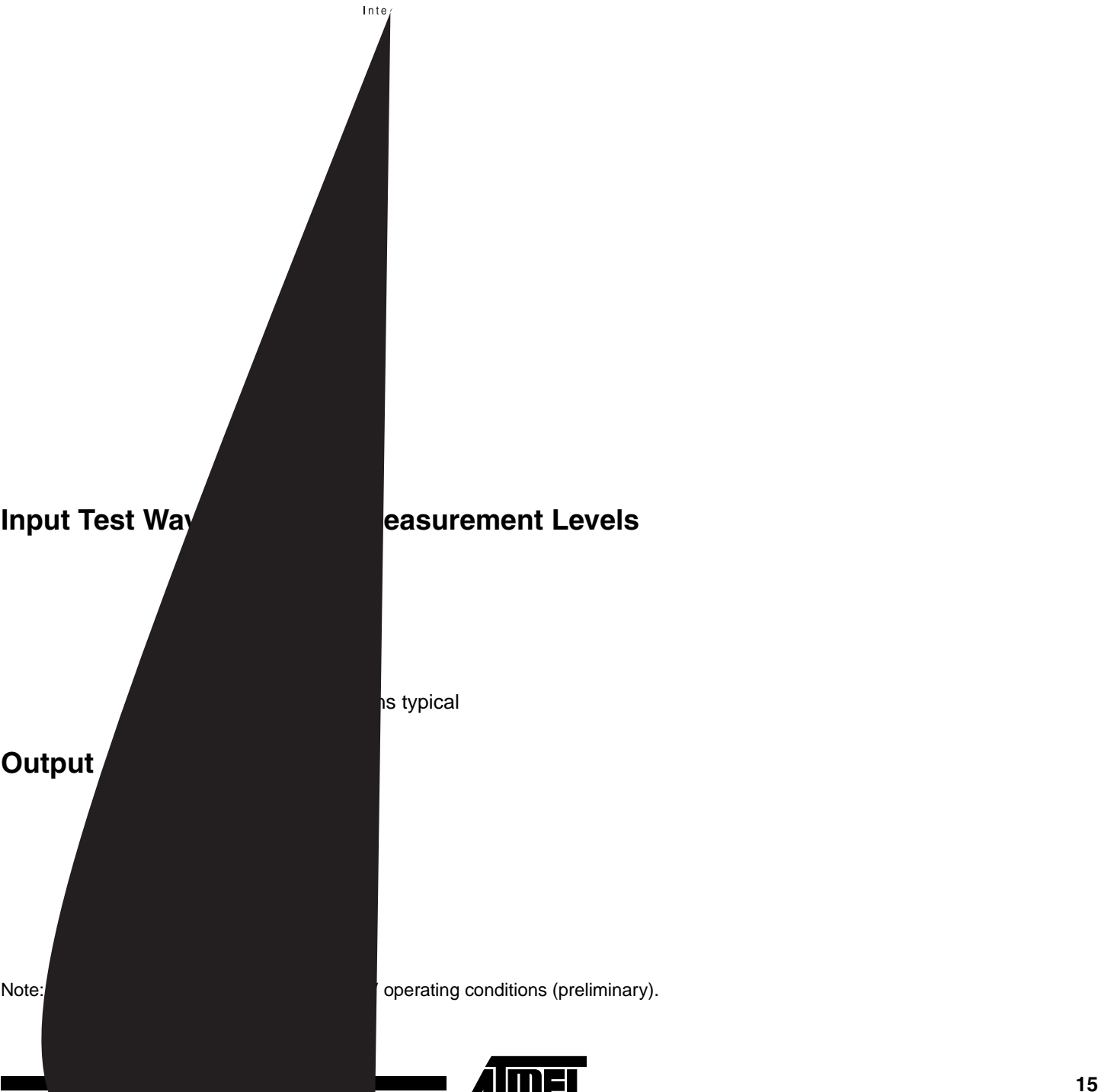
Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.  
2. I<sub>CC3</sub> refers to the current in the reduced-power mode when macrocell reduced-power is turned ON.

Pin Capacitance<sup>(1)</sup>

	Typ	Max	Units	Conditions
C <sub>IN</sub>	8	10	pF	V <sub>IN</sub> = 0V; f = 1.0 MHz
C <sub>I/O</sub>	8	10	pF	V <sub>OUT</sub> = 0V; f = 1.0 MHz

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested. The OGI pin (high-voltage pin during programming) has a maximum capacitance of 12 pF.

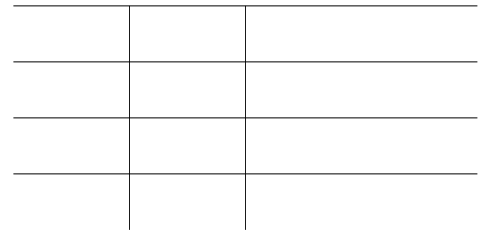
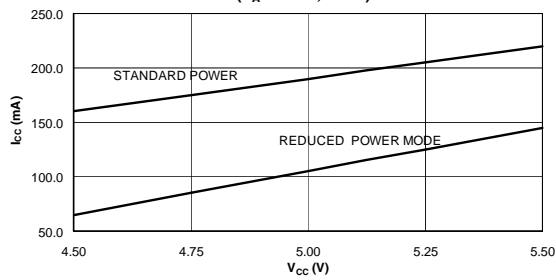
Timing Model



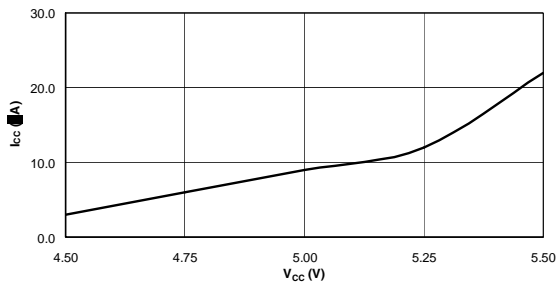
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested. The OGI pin (high-voltage pin during programming) has a maximum capacitance of 12 pF.



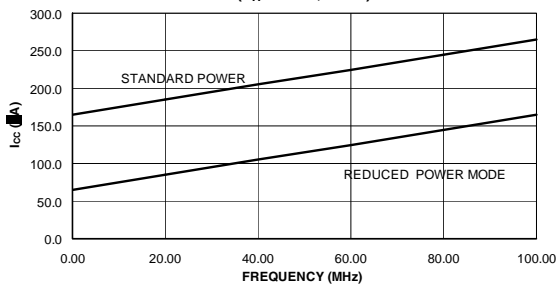
**SUPPLY CURRENT VS. SUPPLY VOLTAGE**  
( $T_A = 25^\circ\text{C}$ ,  $F = 0$ )



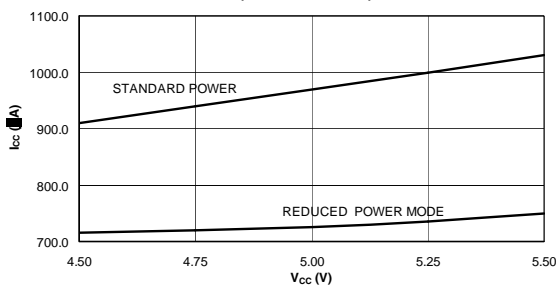
**SUPPLY CURRENT VS. SUPPLY VOLTAGE**  
**LOW-POWER ("L") VERSION**  
( $T_A = 25^\circ\text{C}$ ,  $F = 0$ )

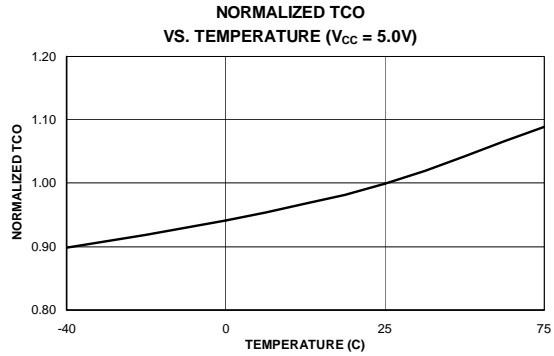
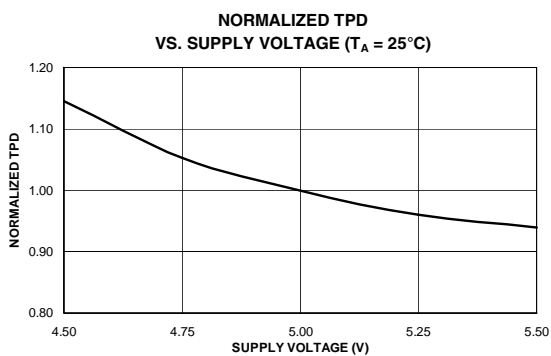
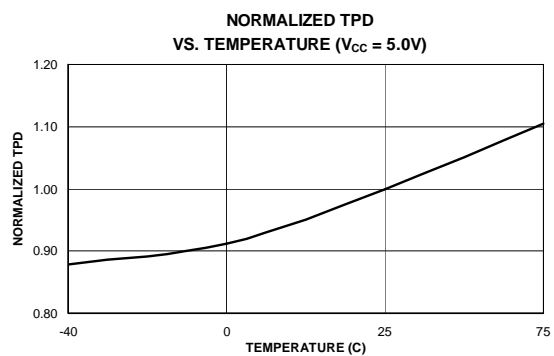
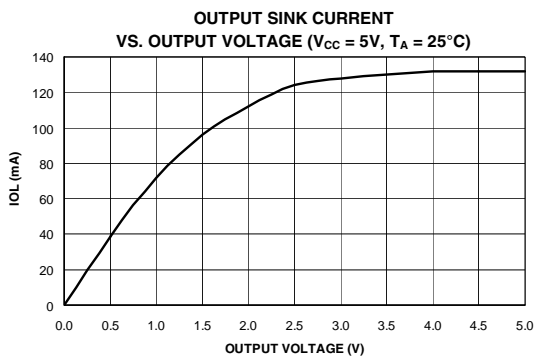
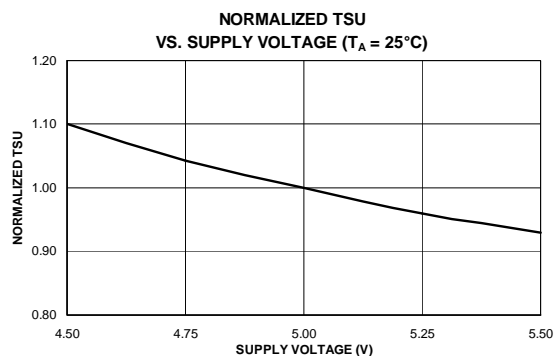
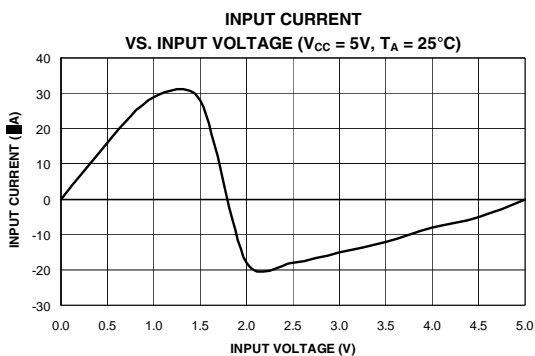
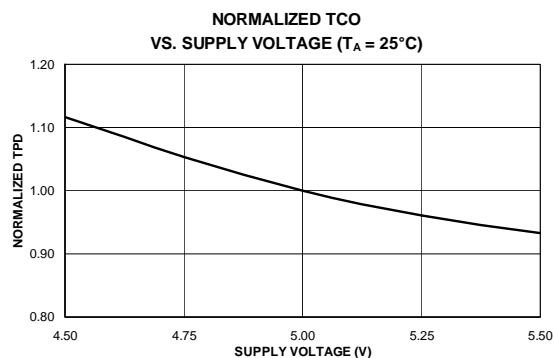
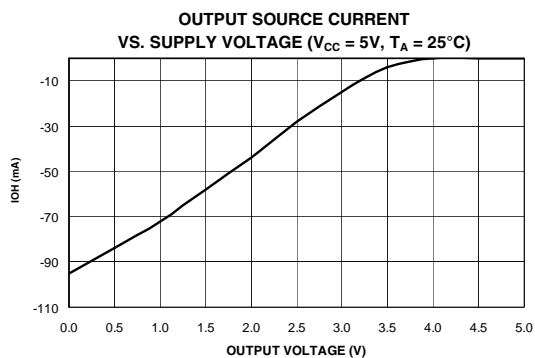


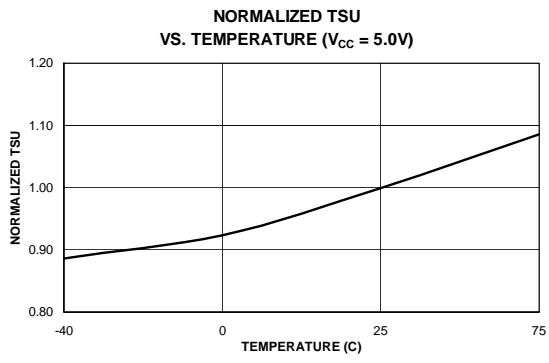
**SUPPLY CURRENT VS. FREQUENCY**  
**STANDARD POWER**  
( $T_A = 25^\circ\text{C}$ ,  $F = 0$ )



**SUPPLY CURRENT VS. SUPPLY VOLTAGE**  
**PIN-CONTROLLED POWER-DOWN MODE**  
( $T_A = 25^\circ\text{C}$ ,  $F = 0$ )







AC Characteristics <sup>(1)</sup>

Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input or Feedback to Non-registered Output		7.5		10	3	15		20		25	ns
t <sub>PD2</sub>	I/O Input or Feedback to Non-registered Feedback		7		9	3	12		16		20	ns
t <sub>SU</sub>	Global Clock Setup Time	6		7		11		16		20		ns
t <sub>H</sub>	Global Clock Hold Time	0		0		0		0		0		ns
t <sub>FSU</sub>	Global Clock Setup Time of Fast Input	3		3		3		3		3		ns
t <sub>FH</sub>	Global Clock Hold Time of Fast Input	0.5		0.5		1.0		1.5		2		MHz
t <sub>COP</sub>	Global Clock to Output Delay		4.5		5		8		10		13	ns
t <sub>CH</sub>	Global Clock High Time	3		4		5		6		7		ns
t <sub>CL</sub>	Global Clock Low Time	3		4		5		6		7		ns
t <sub>ASU</sub>	Array Clock Setup Time	3		3		4		4		5		ns
t <sub>AH</sub>	Array Clock Hold Time	2		3		4		5		6		ns
t <sub>ACOP</sub>	Array Clock Output Delay		7.5		10		15		20		25	ns
t <sub>ACH</sub>	Array Clock High Time	3		4		6		8		10		ns
t <sub>ACL</sub>	Array Clock Low Time	3		4		6		8		10		ns
t <sub>CNT</sub>	Minimum Clock Global Period		8		10		13		17		22	ns
f <sub>CNT</sub>	Maximum Internal Global Clock Frequency	125		100		76.9		66		50		MHz
t <sub>ACNT</sub>	Minimum Array Clock Period		8		10		13		17		22	ns
f <sub>ACNT</sub>	Maximum Internal Array Clock Frequency	125		100		76.9		66		50		MHz
f <sub>MAX</sub>	Maximum Clock Frequency	166.7		125		100		41.7		33.3		MHz
t <sub>IN</sub>	Input Pad and Buffer Delay		0.5		0.5		2		2		2	ns
t <sub>IO</sub>	I/O Input Pad and Buffer Delay		0.5		0.5		2		2		2	ns
t <sub>FIN</sub>	Fast Input Delay		1		1		2		2		2	ns
t <sub>SEXP</sub>	Foldback Term Delay		4		5		8		10		12	ns
t <sub>PEXP</sub>	Cascade Logic Delay		0.8		0.8		1		1		1.2	ns
t <sub>LAD</sub>	Logic Array Delay		3		5		6		7		8	ns
t <sub>LAC</sub>	Logic Control Delay		3		5		6		7		8	ns
t <sub>IOE</sub>	Internal Output Enable Delay		2		2		3		3		4	ns
t <sub>OD1</sub>	Output Buffer and Pad Delay											

## ATF1508AS I/O Pinouts

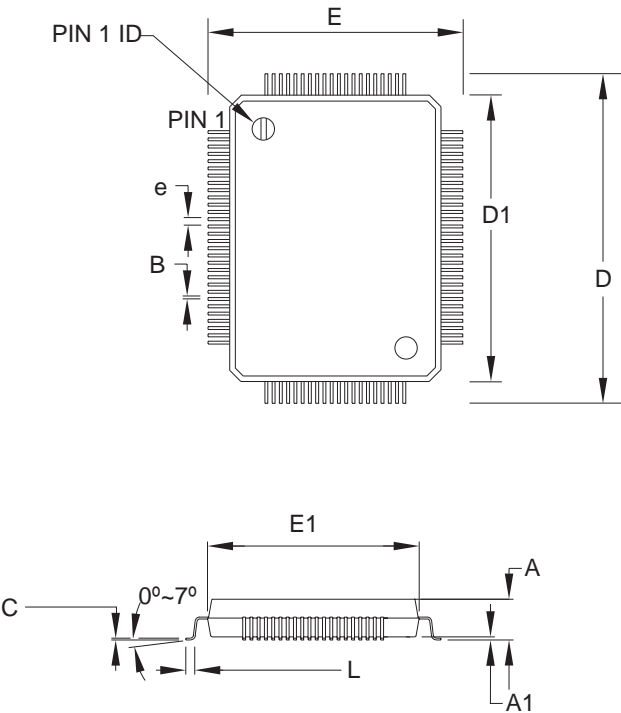
MC	PLB	84-lead J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP	MC	PLB	84-lead J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP
1	A	—	4	2	160	33	C	—	27	25	41
2	A	—	—	—	—	34	C	—	—	—	—
3	A/ PD1	12	3	1	159	35	C	31	26	24	33
4	A	—	—	—	158	36	C	—	—	—	32
5	A	11	2	100	153	37	C	30	25	23	31
6	A	10	1	99	152	38	C	29	24	22	30
7	A	—	—	—	—	39	C	—	—	—	—
8	A	9	100	98	151	40	C	28	23	21	29
9	A	—	99	97	150	41	C	—	22	20	28
10	A	—	—	—	—	42	C	—	—	—	—
11	A	8	98	96	149	43	C	27	21	19	27
12	A	—	—	—	147	44	C	—	—	—	25
13	A	6	96	94	146	45	C	25	19	17	24
14	A	5	95	93	145	46	C	24	18	16	23
15	A	—	—	—	—	47	C	—	—	—	—
16	A	4	94	92	144	48	C/ TMS	23	17	15	22
17	B	22	16	14	21	49	D	41	39	37	59
18	B	—	—	—	—	50	D	—	—	—	—
19	B	21	15	13	20	51	D	40	38	36	58
20	B	—	—	—	19	52	D	—	—	—	57
21	B	20	14	12	18	53	D	39	37	35	56
22	B	—	12	10	16	54	D	—	35	33	54
23	B	—	—	—	—	55	D	—	—	—	—
24	B	18	11	9	15	56	D	37	34	32	53
25	B	17	10	8	14	57	D	36	33	31	52
26	B	—	—	—	—	58	D	—	—	—	—
27	B	16	9	7	13	59	D	35	32	30	51
28	B	—	—	—	12	60	D	—	—	—	50
29	B	15	8	6	11	61	D	34	31	29	49
30	B	—	7	5	10	62	D	—	30	28	48
31	B	—	—	—	—	63	D	—	—	—	—
32	B/ TDI	14	6	4	9	64	D	33	29	27	43
65	E	44	42	40	62	97	G	63	65	63	100

**ATF1508AS I/O Pinouts (Continued)**

MC	PLB	84-lead J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP	MC	PLB	84-lead J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP
66	E	—	—	—	—	98	G	—	—	—	—
67	E/ PD2	45	43	41	63	99	G	64	66	64	101
68	E	—	—	—	64	100	G	—	—	—	102
69	E	46	44	42	65	101	G	65	67	65	103
70	E	—	46	44	67	102	G	—	69	67	105
71	E	—	—	—	—	103	G	—	—	—	—
72	E	48	47	45	68	104	G	67	70	68	106
73	E	49	48	46	69	105	G	68	71	69	107
74	E	—	—	—	—	106	G	—	—	—	—
75	E	50	49	47	70	107	G	69	72	70	108
76	E	—	—	—	71	108	G	—	—	—	109
77	E	51	50	48	72	109	G	70	73	71	110
78	E	—	51	49	73	110	G	—	74	72	111
79	E	—	—	—	—	111	G	—	—	—	—
80	E	52	52	50	78	112	G/ TDO	71	75	73	112
81	F	—	54	52	80	113	H	—	77	75	121
82	F	—	—	—	—	114	H	—	—	—	—
83	F	54	55	53	88	115	H	73	78	76	122
84	F	—	—	—	89	116	H	—	—	—	123
85	F	55	56	54	90	117	H	74	79	77	128
86	F	56	57	55	91	118	H	75	80	78	129
87	F	—	—	—	—	119	H	—	—	—	—
88	F	57	58	56	92	120	H	76	81	79	130
89	F	—	59	57	93	121	H	—	82	80	131
90	F	—	—	—	—	122	H	—	—	—	—
91	F	58	60	58	94	123	H	77	83	81	132
92	F	—	—	—	96	124	H	—	—	—	134
93	F	60	62	60	97	125	H	79	85	83	135
94	F	61	63	61	98	126	H	80	86	84	136
95	F	—	—	—	—	127	H	—	—	—	—
96	F/ TCK	62	64	62	99	128	H/ GCLK3	81	87	85	137



100Q1 – PQFP



**COMMON DIMENSIONS**  
(Unit of Measure = mm)  
JEDEC STANDARD MS-022, GC-1

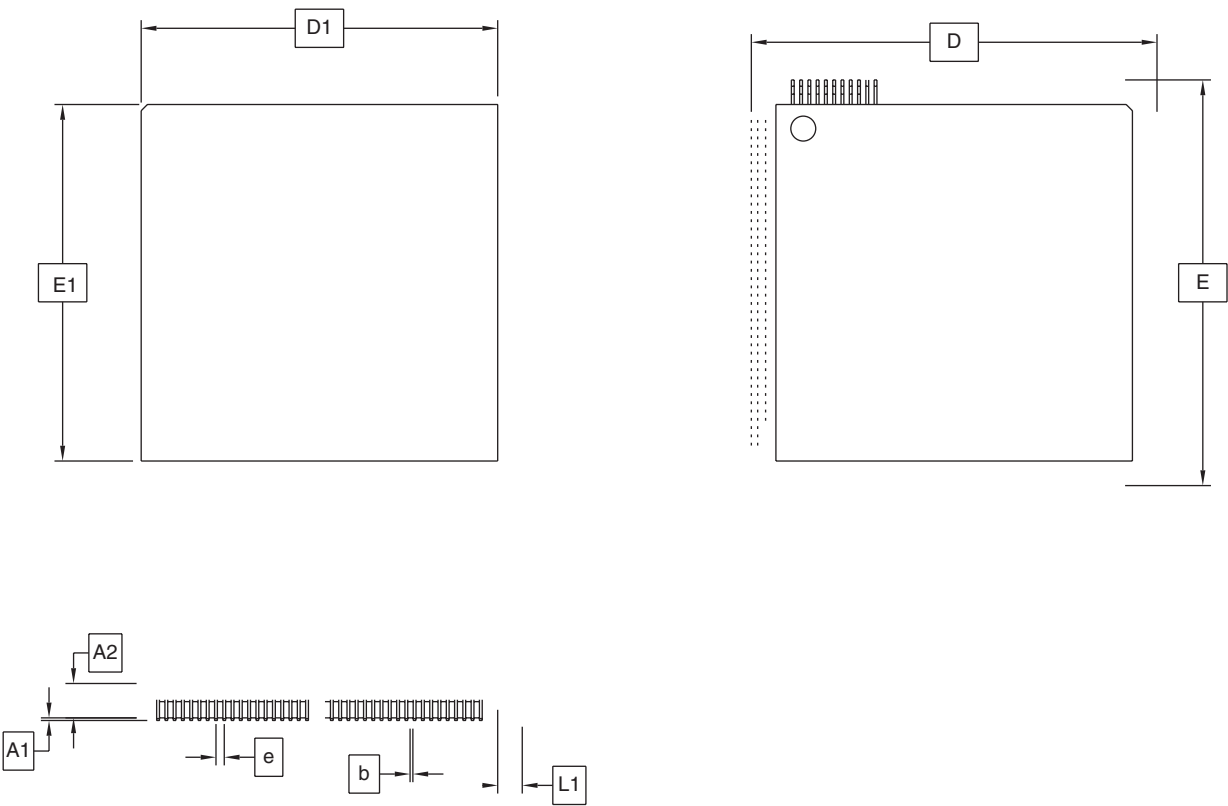
SYMBOL	MIN	NOM	MAX	NOTE
A	–	3.04	3.4	
A1	0.25	0.33	0.5	
D	23.20 BSC			
E	17.20 BSC			
E1	14.00 BSC			
B	0.22	–	0.40	
C	0.11	–	0.23	
D1	20 BSC			
L	0.73	–	1.03	
e	0.65 BSC			

07/6/2005


 2325 Orchard Parkway San Jose, CA 95131	<b>TITLE</b> <b>100Q1</b> , 100-lead, 14 x 20 mm Body, 3.2 mm Footprint, 0.65 mm Pitch, Plastic Quad Flat Package (PQFP)	<b>DRAWING NO.</b> 100Q1	<b>REV.</b> C
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160Q1 – PQFP



3/28/02

 2325 Orchard Parkway San Jose, CA 95131	<b>TITLE</b> <b>160Q1</b> , 160-lead, 28 x 28 mm Body, 3.2 Form Opt., Plastic Quad Flat Pack (PQFP)	<b>DRAWING NO.</b> 160Q1	<b>REV.</b> A
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## Revision History

Revision	Comments
0784P	Green package options added.
0784O	The ATF1508ASL-25 commercial speed offering was obsoleted in 2002 and replaced by the ATF1508ASL-20 commercial speed grade.