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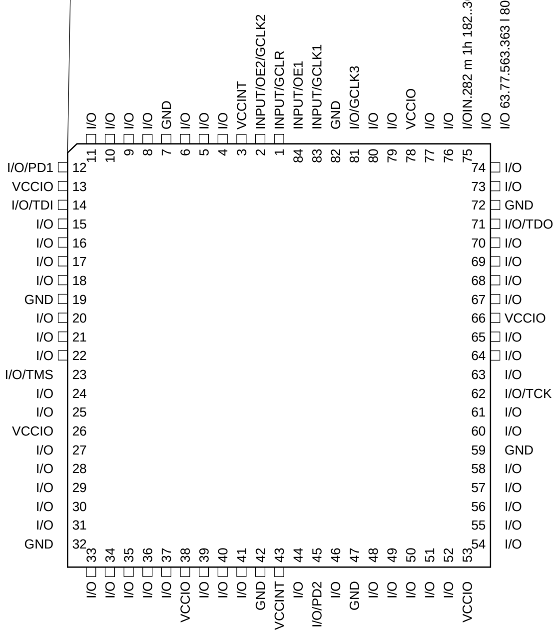
Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

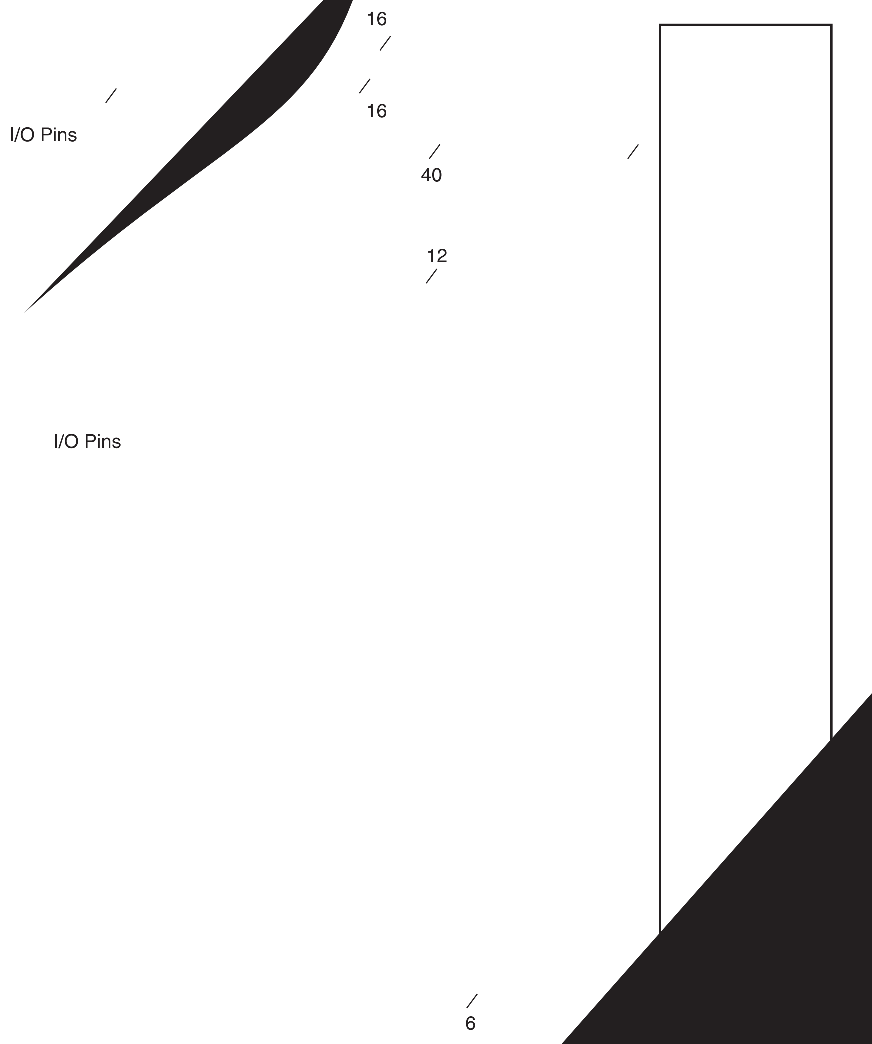
Details	
Product Status	Active
Programmable Type	In System Programmable (min 10K program/erase cycles)
Delay Time tpd(1) Max	25 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	64
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atf1508asl-25ju84

84-lead PLCC
Top View



100-lead TQFP
Top View

Block Diagram



Flip-flop

The ATF1508AS's flip-flop has very flexible data and control functions. The data input can come from either the XOR gate, from a separate product term or directly from the I/O pin. Selecting the separate product term allows creation of a buried registered feedback within a combinatorial output macrocell. (This feature is automatically implemented by the fitter software). In addition to D, T, JK and SR operation, the flip-flop can also be configured as a flow-through latch. In this mode, data passes through when the clock is high and is latched when the clock is low.

The clock itself can be either the Global CLK Signal (GCK) or an individual product term. The flip-flop changes state on the clock's rising edge. When the GCK signal is used as the clock, one of the macrocell product terms can be selected as a clock enable. When the clock enable function is active and the enable signal (product term) is low, all clock edges are ignored. The flip-flop's asynchronous reset signal (AR) can be either the Global Clear (GCLEAR), a product term, or always off. AR can also be a logic OR of GCLEAR with a product term. The asynchronous preset (AP) can be a product term or always off.

Extra Feedback

The ATF15xxSE Family macrocell output can be selected as registered or combinatorial. The extra buried feedback signal can be either combinatorial or a registered signal regardless of whether the output is combinatorial or registered. (This enhancement function is automatically implemented by the fitter software.) Feedback of a buried combinatorial output allows the creation of a second latch within a macrocell.

I/O Control

The output enable multiplexer (MOE) controls the output enable signal. Each I/O can be individually configured as an input, output or for bi-directional operation. The output enable for each macrocell can be selected from the true or compliment of the two output enable pins, a subset of the I/O pins, or a subset of the I/O macrocells. This selection is automatically done by the fitter software when the I/O is configured as an input, all macrocell resources are still available, including the buried feedback, expander and cascade logic.

Global Bus/Switch Matrix

The global bus contains all input and I/O pin signals as well as the buried feedback signal from all 128 macrocells. The switch matrix in each logic block receives as its inputs all signals from the global bus. Under software control, up to 40 of these signals can be selected as inputs to the logic block.

Foldback Bus

Each macrocell also generates a foldback product term. This signal goes to the regional bus and is available to 16 macrocells. The foldback is an inverse polarity of one of the macrocell's product terms. The 16 foldback terms in each region allows generation of high fan-in sum terms (up to 21 product terms) with a little additional delay.

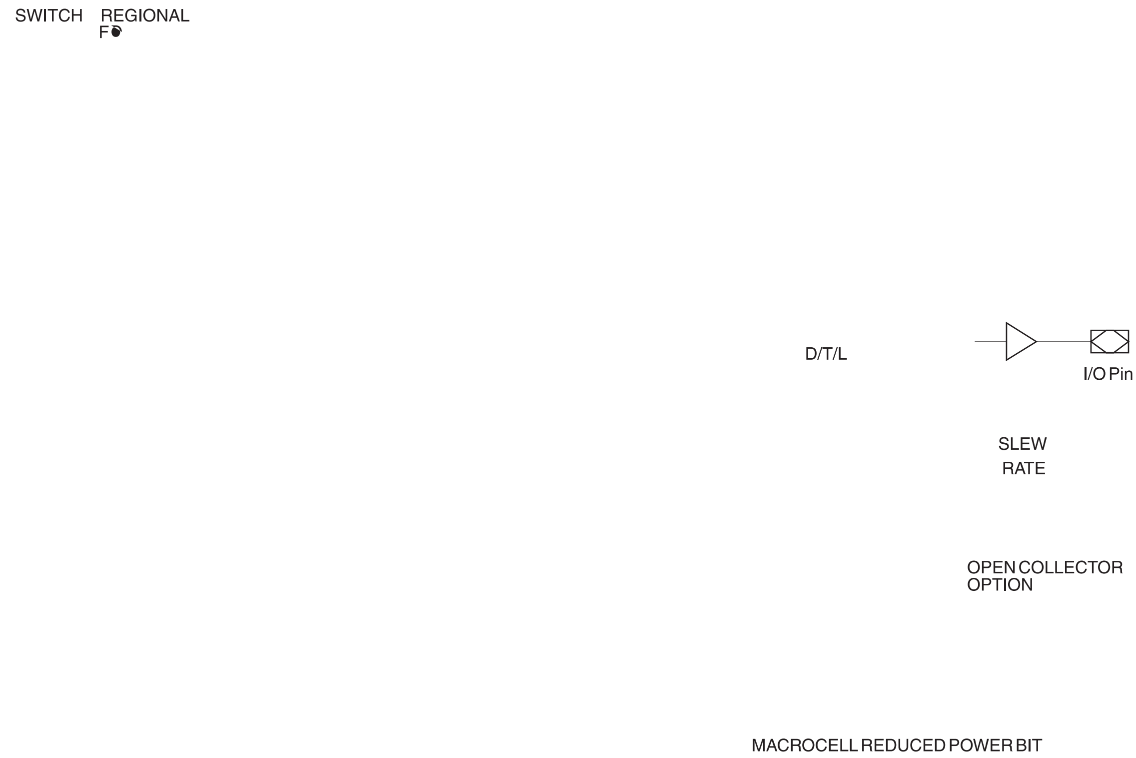
3.3V or 5.0V I/O Operation

The ATF1508AS device has two sets of V_{CC} pins viz, V_{CCINT} and V_{CCIO}. V_{CCINT} pins must always be connected to a 5.0V power supply. V_{CCINT} pins are for input buffers and are "compatible" with both 3.3V and 5.0V inputs. V_{CCIO} pins are for I/O output drives and can be connected for 3.3/5.0V power supply.

Open-collector Output Option

This option enables the device output to provide control signals such as an interrupt that can be asserted by any of the several devices.

Figure 1. ATF1508AS Macrocell



Programmable Pin-keeper Option for Inputs and I/Os

The ATF1508AS offers the option of programming all input and I/O pins so that “pin-keeper” circuits can be utilized. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high- or low-level. This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

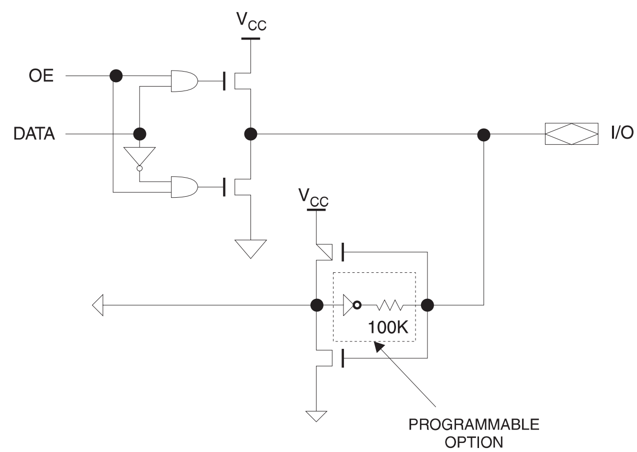
Input Diagram

Speed/Power Management

The ATF1508AS has several built-in speed and power management features. The ATF1508AS contains circuitry that automatically puts the device into a low-power stand-by mode when no logic transitions are occurring. This not only reduces power consumption during inactive periods, but also provides proportional power-savings for most applications running at system speeds below 5 MHz.

To further reduce power, each ATF1508AS macrocell has a Reduced-power bit feature. This feature allows individual macrocells to be configured for maximum power savings. This feature may be selected as a design option.

I/O Diagram



All ATF1508 also have an optional power-down mode. In this mode, current drops to below 10 mA. When the power-down option is selected, either PD1 or PD2 pins (or both) can be used to power down the part. The power-down option is selected in the design source file. When enabled, the device goes into power-down when either PD1 or PD2 is high. In the power-down mode, all internal logic signals are latched and held, as are any enabled outputs.

All pin transitions are ignored until the PD pin is brought low. When the power-down feature is enabled, the PD1 or PD2 pin cannot be used as a logic input or output. However, the pin's macrocell may still be used to generate buried foldback and cascade logic signals.

All power-down AC characteristic parameters are computed from external input or I/O pins, with Reduced-power Bit turned on. For macrocells in reduced-power mode (Reduced-power bit turned on), the reduced-power adder, tRPA, must be added to the AC parameters, which include the data paths t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{ACH} and t_{SEXP}.

Each output also has individual slew rate control. This may be used to reduce system noise by slowing down outputs that do not need to operate at maximum speed. Outputs default to slow switching, and may be specified as fast switching in the design file.

ISP Programming Protection

The ATF1508AS has a special feature that locks the device and prevents the inputs and I/O from driving if the programming process is interrupted for any reason. The inputs and I/O default to high-Z state during such a condition. In addition the pin-keeper option preserves the former state during device programming.

All ATF1508AS devices are initially shipped in the erased state thereby making them ready to use for ISP.

Note: For more information refer to the “Designing for In-System Programmability with Atmel CPLDs” application note.

JTAG-BST Overview

The JTAG boundary-scan testing is controlled by the Test Access Port (TAP) controller in the ATF1508AS. The boundary-scan technique involves the inclusion of a shift-register stage (contained in a boundary-scan cell) adjacent to each component so that signals at component boundaries can be controlled and observed using scan testing principles. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary-scan testing. The ATF1508AS does not currently include a Test Reset (TRST) input pin because the TAP controller is automatically reset at power-up. The six JTAG BST modes supported include: SAMPLE/PRELOAD, EXTEST, BYPASS and IDCODE. BST on the ATF1508AS is implemented using the Boundary-scan Definition Language (BSDL) described in the JTAG specification (IEEE Standard 1149.1). Any third-party tool that supports the BSDL format can be used to perform BST on the ATF1508AS.

The ATF1508AS also has the option of using four JTAG-standard I/O pins for In-System programming (ISP). The ATF1508AS is programmable through the four JTAG pins using programming compatible with the IEEE JTAG Standard 1149.1. Programming is performed by using 5V TTL-level programming signals from the JTAG ISP interface. The JTAG feature is a programmable option. If JTAG (BST or ISP) is not needed, then the four JTAG control pins are available as I/O pins.

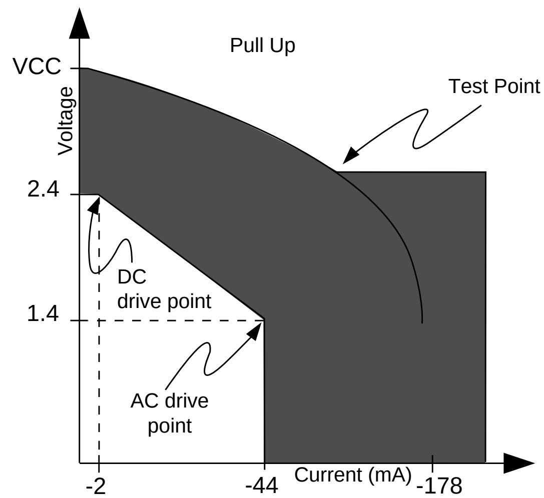
JTAG Boundary-scan Cell (BSC) Testing

The ATF1508AS contains up to 96 I/O pins and four input pins, depending on the device type and package type selected. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary-scan testing as described in detail by IEEE Standard 1149.1. A typical BSC consists of three capture registers or scan registers and up to two update registers. There are two types of BSCs, one for input or I/O pin, and one for the macrocells. The BSCs in the device are chained together through the (BST) capture registers. Input to the capture register chain is fed in from the TDI pin while the output is directed to the TDO pin. Capture registers are used to capture active device data signals, to shift data in and out of the device and to load data into the update registers. Control signals are generated internally by the JTAG TAP controller. The BSC configuration for the input and I/O pins and macrocells are shown below.

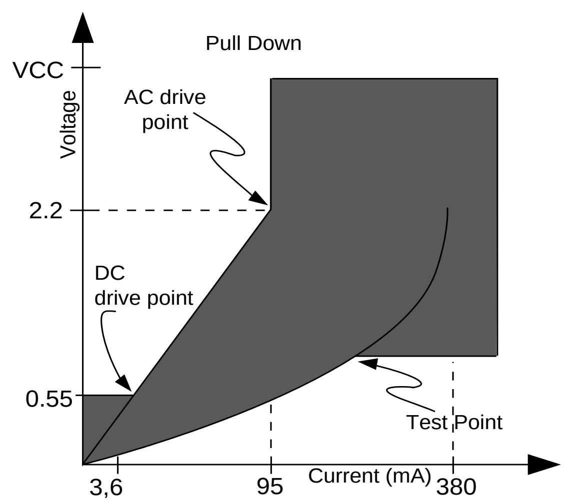
PCI Compliance

The ATF1508AS also supports the growing need in the industry to support the new Peripheral Component Interconnect (PCI) interface standard in PCI-based designs and specifications. The PCI interface calls for high current drivers, which are much larger than the traditional TTL drivers.

PCI Voltage-to-current Curves for +5V Signaling in Pull-up Mode



PCI Voltage-to-current Curves for +5V Signaling in Pull-down Mode



DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Ambient)	0°C - 70°C	-40°C - 85°C
V_{CCINT} or V_{CCIO} (5V) Power Supply	5V ± 5%	5V ± 10%
V_{CCIO} (3.3V) Power Supply	2.7V - 3.6V	2.7V - 3.6V

DC Characteristics[1]

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$V_{IN} = V_{CC}$				-2	-10	µA
I_{IH}	Input or I/O High Leakage Current					2	10	µA
I_{OZ}	Tri-state Output Off-state Current	$V_O = V_{CC}$ or GND			-40		40	µA
I_{CC1}	Power Supply Current, Standby	V_{CC} = Max $V_{IN} = 0, V_{CC}$	Std Mode	Com.		160		mA
				Ind.		180		mA
			"L" Mode	Com.		10		µA
				Ind.		10		µA
I_{CC2}	Power Supply Current, Power-down Mode	V_{CC} = Max $V_{IN} = 0, V_{CC}$	"PD" Mode			1	10	mA
I_{CC3}[2]	Reduced-power Mode Supply Current	V_{CC} = Max $V_{IN} = 0, V_{CC}$	Std Mode	Com.		65		mA
				Ind.		85		mA
V_{CCIO}	Supply Voltage	5.0V Device Output		Com.	4.75		5.25	V
				Ind.	4.5		5.5	V
V_{CCIO}	Supply Voltage	3.3V Device Output			3.0		3.6	V
V_{IL}	Input Low Voltage				-0.3		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CCIO} + 0.3	V
V_{OL}	Output Low Voltage (TTL)	$V_{IN} = V_{IH}$ or V_{IL} V_{CCIO} = MIN, I_{OL} = 12 mA		Com.			0.45	V
				Ind.			0.45	V
	Output Low Voltage (CMOS)	$V_{IN} = V_{IH}$ or V_{IL} V_{CC} = MIN, I_{OL} = 0.1 mA		Com.			0.2	V
				Ind.			0.2	V
V_{OH}	Output High Voltage (TTL)	$V_{IN} = V_{IH}$ or V_{IL} V_{CCIO} = MIN, I_{OH} = -4.0 mA			2.4			V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. I_{CC3} refers to the current in the reduced-power mode when macrocell reduced-power is turned ON.

Pin Capacitance[1]

	Typ	Max	Units	Conditions
C_{IN}	8	10	pF	V_{IN} = 0V; f = 1.0 MHz
$C_{I/O}$	8	10	pF	V_{OUT} = 0V; f = 1.0 MHz

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested. The OGI pin (high-voltage pin during programming) has a maximum capacitance of 12 pF.

Timing Model

Inte

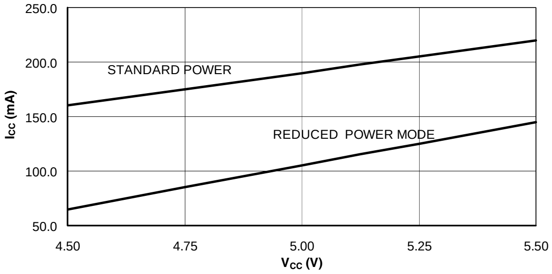
Input Test Wav easurement Levels

ns typical

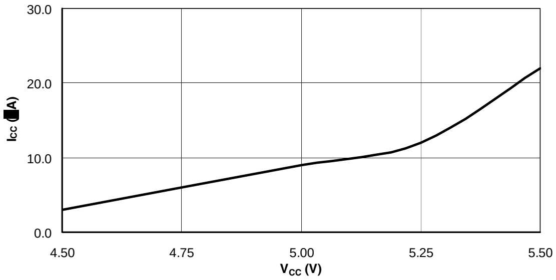
Output

Note: operating conditions (preliminary).

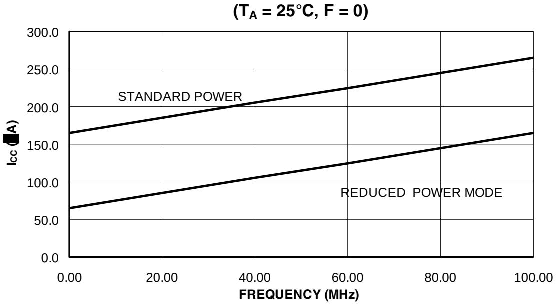
SUPPLY CURRENT VS. SUPPLY VOLTAGE
(T_A = 25°C, F = 0)



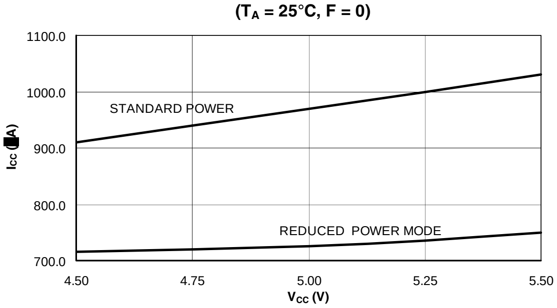
SUPPLY CURRENT VS. SUPPLY VOLTAGE
LOW-POWER ("L") VERSION
(T_A = 25°C, F = 0)



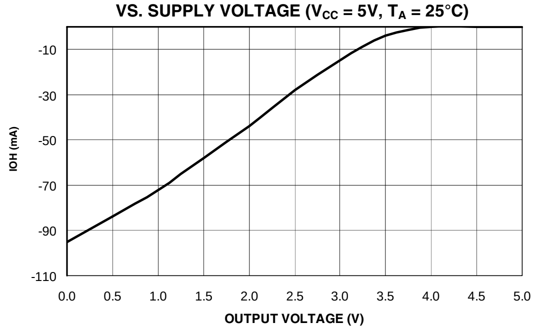
SUPPLY CURRENT VS. FREQUENCY
STANDARD POWER
(T_A = 25°C, F = 0)



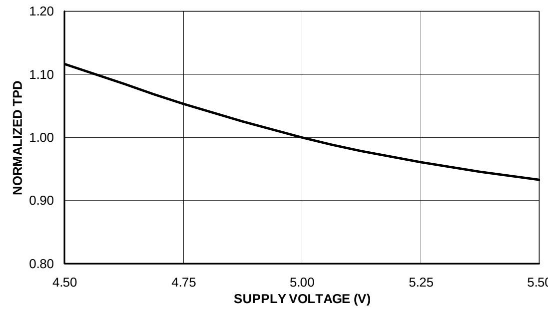
SUPPLY CURRENT VS. SUPPLY VOLTAGE
PIN-CONTROLLED POWER-DOWN MODE
(T_A = 25°C, F = 0)



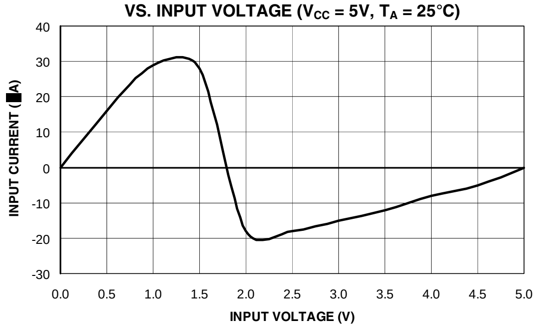
OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE (V_{CC} = 5V, T_A = 25°C)



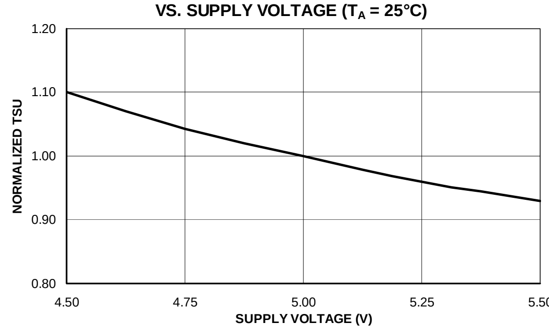
NORMALIZED TCO VS. SUPPLY VOLTAGE (T_A = 25°C)



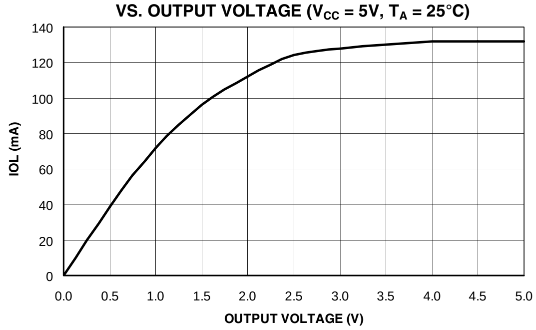
INPUT CURRENT VS. INPUT VOLTAGE (V_{CC} = 5V, T_A = 25°C)



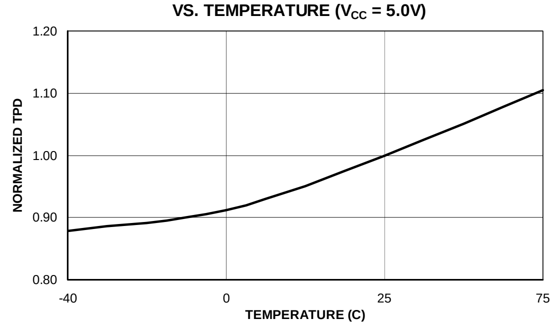
NORMALIZED TSU VS. SUPPLY VOLTAGE (T_A = 25°C)



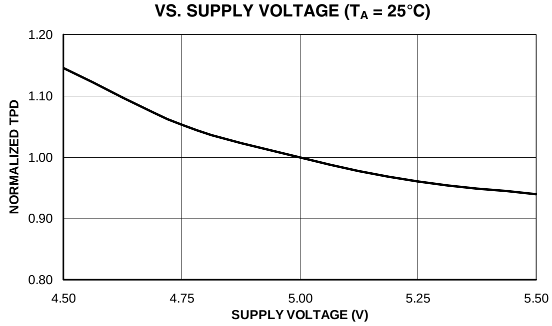
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5V, T_A = 25°C)



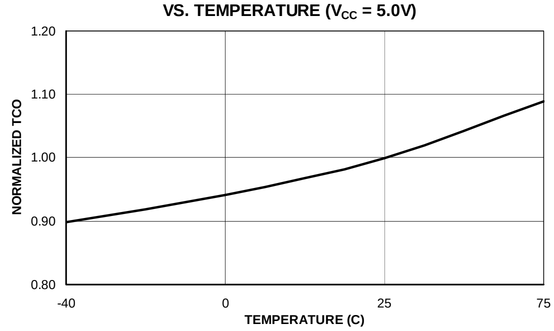
NORMALIZED TPD VS. TEMPERATURE (V_{CC} = 5.0V)



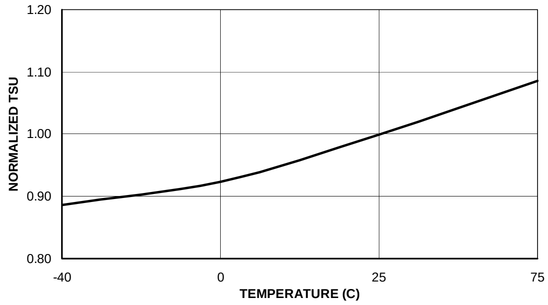
NORMALIZED TPD VS. SUPPLY VOLTAGE (T_A = 25°C)



NORMALIZED TCO VS. TEMPERATURE (V_{CC} = 5.0V)



NORMALIZED TSU
VS. TEMPERATURE (V_{CC} = 5.0V)



AC Characteristics [1]

Symbol	Parameter	-7 Min	-7 Max	-10 Min	-10 Max	-15 Min	-15 Max	-20 Min	-20 Max	-25 Min	-25 Max	Units
t_{PD1}	Input or Feedback to Non-registered Output		7.5		10	3	15		20		25	ns
t_{PD2}	I/O Input or Feedback to Non-registered Feedback		7		9	3	12		16		20	ns
t_{SU}	Global Clock Setup Time	6		7		11		16		20		ns
t_{H}	Global Clock Hold Time	0		0		0		0		0		ns
t_{FSU}	Global Clock Setup Time of Fast Input	3		3		3		3		3		ns
t_{FH}	Global Clock Hold Time of Fast Input	0.5		0.5		1.0		1.5		2		MHz
t_{COP}	Global Clock to Output Delay		4.5		5		8		10		13	ns
t_{CH}	Global Clock High Time	3		4		5		6		7		ns
t_{CL}	Global Clock Low Time	3		4		5		6		7		ns
t_{ASU}	Array Clock Setup Time	3		3		4		4		5		ns
t_{AH}	Array Clock Hold Time	2		3		4		5		6		ns
t_{ACOP}	Array Clock Output Delay		7.5		10		15		20		25	ns
t_{ACH}	Array Clock High Time	3		4		6		8		10		ns
t_{ACL}	Array Clock Low Time	3		4		6		8		10		ns
t_{CNT}	Minimum Clock Global Period		8		10		13		17		22	ns
f_{CNT}	Maximum Internal Global Clock Frequency	125		100		76.9		66		50		MHz
t_{ACNT}	Minimum Array Clock Period		8		10		13		17		22	ns
f_{ACNT}	Maximum Internal Array Clock Frequency	125		100		76.9		66		50		MHz
f_{MAX}	Maximum Clock Frequency	166.7		125		100		41.7		33.3		MHz
t_{IN}	Input Pad and Buffer Delay		0.5		0.5		2		2		2	ns
t_{IO}	I/O Input Pad and Buffer Delay		0.5		0.5		2		2		2	ns
t_{FIN}	Fast Input Delay		1		1		2		2		2	ns
t_{SEXP}	Foldback Term Delay		4		5		8		10		12	ns
t_{PEXP}	Cascade Logic Delay		0.8		0.8		1		1		1.2	ns
t_{LAD}	Logic Array Delay		3		5		6		7		8	ns
t_{LAC}	Logic Control Delay		3		5		6		7		8	ns
t_{IOE}	Internal Output Enable Delay		2		2		3		3		4	ns
t_{OD1}	Output Buffer and Pad Delay											

ATF1508AS I/O Pinouts

MC	PLB	84-lead J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP	MC	PLB	84-lead J-lead	100-lead PQFP	100-lead TQFP	160-lead PQFP
1	A	–	4	2	160	33	C	–	27	25	41
2	A	–	–	–	–	34	C	–	–	–	–
3	A/ **PD1**	12	3	1	159	35	C	31	26	24	33
4	A	–	–	–	158	36	C	–	–	–	32
5	A	11	2	100	153	37	C	30	25	23	31
6	A	10	1	99	152	38	C	29	24	22	30
7	A	–	–	–	–	39	C	–	–	–	–
8	A	9	100	98	151	40	C	28	23	21	29
9	A	–	99	97	150	41	C	–	22	20	28
10	A	–	–	–	–	42	C	–	–	–	–
11	A	8	98	96	149	43	C	27	21	19	27
12	A	–	–	–	147	44	C	–	–	–	25
13	A	6	96	94	146	45	C	25	19	17	24
14	A	5	95	93	145	46	C	24	18	16	23
15	A	–	–	–	–	47	C	–	–	–	–
16	A	4	94	92	144	48	C/ **TMS**	23	17	15	22
17	B	22	16	14	21	49	D	41	39	37	59
18	B	–	–	–	–	50	D	–	–	–	–
19	B	21	15	13	20	51	D	40	38	36	58
20	B	–	–	–	19	52	D	–	–	–	57
21	B	20	14	12	18	53	D	39	37	35	56
22	B	–	12	10	16	54	D	–	35	33	54
23	B	–	–	–	–	55	D	–	–	–	–
24	B	18	11	9	15	56	D	37	34	32	53
25	B	17	10	8	14	57	D	36	33	31	52
26	B	–	–	–	–	58	D	–	–	–	–
27	B	16	9	7	13	59	D	35	32	30	51
28	B	–	–	–	12	60	D	–	–	–	50
29	B	15	8	6	11	61	D	34	31	29	49
30	B	–	7	5	10	62	D	–	30	28	48
31	B	–	–	–	–	63	D	–	–	–	–
32	B/ **TDI**	14	6	4	9	64	D	33	29	27	43
65	E	44	42	40	62	97	G	63	65	63	100

ATF1508ASL Standard Package Options

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
20	12	83.3	ATF1508ASL-20 JC84	84J	Commercial (0°C to 70°C)
			ATF1508ASL-20 QC100	100Q1	
			ATF1508ASL-20 AC100	100A	
			ATF1508ASL-20 QC160	160Q1	
25	15	70	ATF1508ASL-25 JI84	84J	Industrial (-40°C to +85°C)
			ATF1508ASL-25 QI100	100Q1	
			ATF1508ASL-25 AI100	100A	
			ATF1508ASL-25 QI160	160Q1	

Note: 1. The last time buy is Sept. 30, 2005 for shaded parts.

Using "C" Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the "I" to the "C" device (7 ns "C" = 10 ns "I") and de-rate power by 30%.

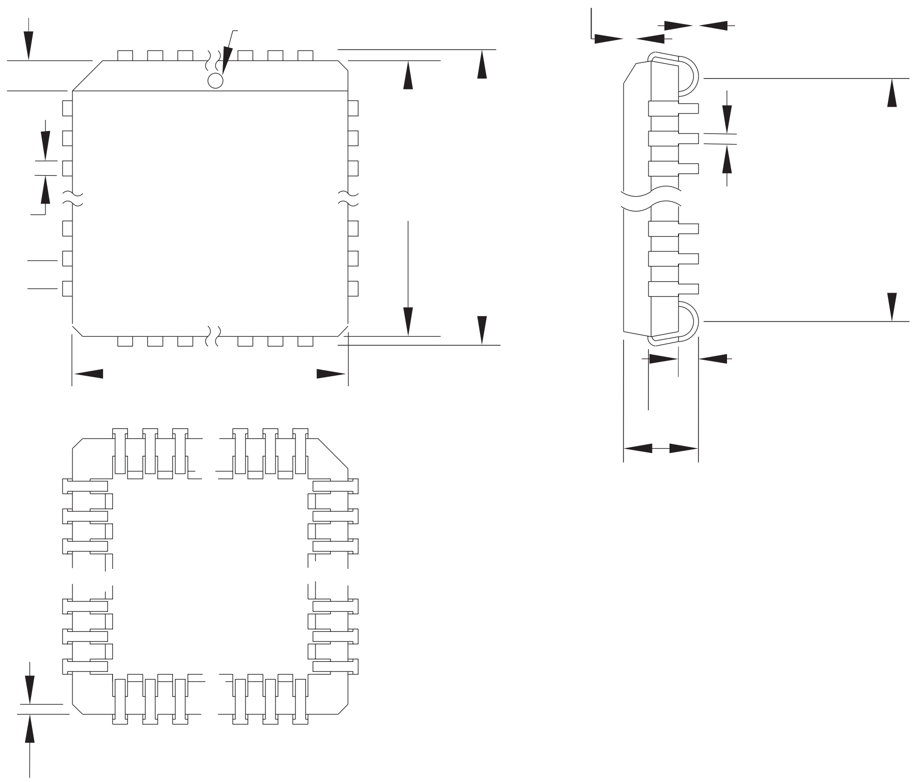
ATF1508ASL Green Package Options (Pb/Halide-free/RoHS Compliant)

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
25	15	70	ATF1508ASL-25 JU84 ATF1508ASL-25 AU100	84J 100A	Industrial (-40°C to +85°C)

Package Type	
84J	84-lead, Plastic J-leaded Chip Carrier (PLCC)
100Q1	100-lead, Plastic Quad Pin Flat Package (PQFP)
100A	100-lead, Very Thin Plastic Gull Wing Quad Flat Package (TQFP)
160Q1	160-lead, Plastic Quad Pin Flat Package (PQFP)

Package Information

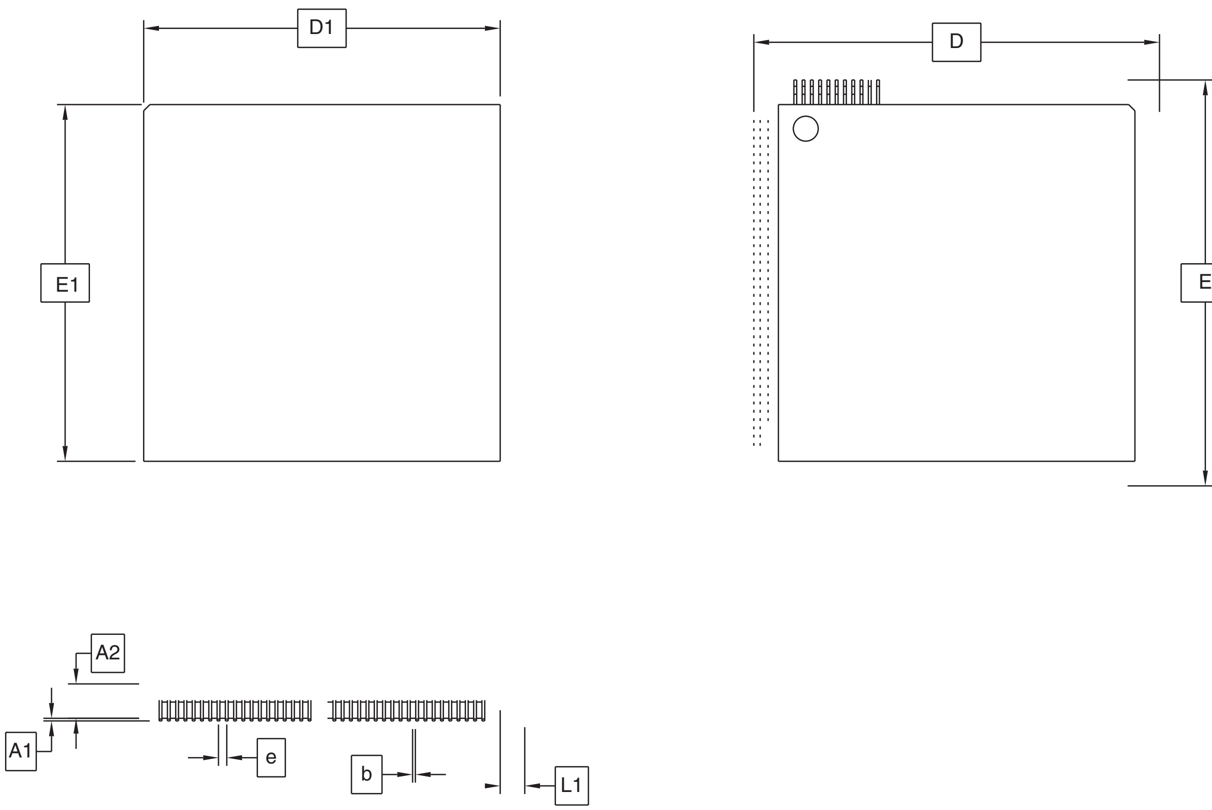
84J – PLCC



10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**84J**, 84-lead, Plastic J-leaded Chip Carrier (PLCC)	84J	B

160Q1 – PQFP



3/28/02

2325 Orchard Parkway San Jose, CA 95131	**TITLE** **160Q1,** 160-lead, 28 x 28 mm Body, 3.2 Form Opt., Plastic Quad Flat Pack (PQFP)	**DRAWING NO.** 160Q1	**REV.** A

Revision History

Revision	Comments
0784P	Green package options added.
0784O	The ATF1508ASL-25 commercial speed offering was obsoleted in 2002 and replaced by the ATF1508ASL-20 commercial speed grade.

Printed on recycled paper.

0784P–PLD–7/05 xM