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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	47
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 14x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-TQFP-64-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/fx164cm4f40faaxt

XC164CM

16-Bit Single-Chip Microcontroller
with C166SV2 Core

Microcontrollers



Never stop thinking

Summary of Features
Table 1 XC164CM Derivative Synopsis

Derivative ¹⁾	Temp. Range	Program Memory	On-Chip RAM	Interfaces
SAK-XC164CM-16F40F SAK-XC164CM-16F20F	-40 to 125 °C	128 Kbytes Flash	2 Kbytes DPRAM, 4 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1
SAF-XC164CM-16F40F SAF-XC164CM-16F20F	-40 to 85 °C	128 Kbytes Flash	2 Kbytes DPRAM, 4 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1
SAK-XC164CM-8F40F SAK-XC164CM-8F20F	-40 to 125 °C	64 Kbytes Flash	2 Kbytes DPRAM, 2 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1
SAF-XC164CM-8F40F SAF-XC164CM-8F20F	-40 to 85 °C	64 Kbytes Flash	2 Kbytes DPRAM, 2 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1
SAK-XC164CM-4F40F SAK-XC164CM-4F20F	-40 to 125 °C	32 Kbytes Flash	2 Kbytes DPRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1
SAF-XC164CM-4F40F SAF-XC164CM-4F20F	-40 to 85 °C	32 Kbytes Flash	2 Kbytes DPRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1

1) This Data Sheet is valid for:
 devices starting with and including design step BA for the -16F derivatives, and for
 devices starting with and including design step AA for -4F/8F derivatives.

General Device Information
Table 2 Pin Definitions and Functions (cont'd)

Sym- bol	Pin Num.	Input Outp.	Function
PORT1	1-6, 49-56	IO	PORT1 consists of one 8-bit and one 6-bit bidirectional I/O port P1L and P1H. Each pin can be programmed for input (output driver in high-impedance state) or output. The following PORT1 pins also serve for alt. functions:
P1L.0	49	I/O	CC60: [CAPCOM6] Input / Output of Channel 0
P1L.1	50	O	COUT60: [CAPCOM6] Output of Channel 0
P1L.2	51	I/O	CC61: [CAPCOM6] Input / Output of Channel 1
P1L.3	52	O	COUT61: [CAPCOM6] Output of Channel 1
P1L.4	53	I/O	CC62: [CAPCOM6] Input / Output of Channel 2
P1L.5	54	O	COUT62: [CAPCOM6] Output of Channel 2
P1L.6	55	O	COUT63: Output of 10-bit Compare Channel
P1L.7	56	I	CTRAP: [CAPCOM6] Trap Input CTRAP is an input pin with an internal pull-up resistor. A low level on this pin switches the CAPCOM6 compare outputs to the logic level defined by software (if enabled).
P1H.0	1	I/O I I	CC22IO: [CAPCOM2] CC22 Capture Inp./Compare Outp. CC6POS0: [CAPCOM6] Position 0 Input, EX0IN: [Fast External Interrupt 0] Input (default pin),
P1H.1	2	I/O I	CC23IO: [CAPCOM2] CC23 Capture Inp./Compare Outp. CC6POS1: [CAPCOM6] Position 1 Input,
P1H.2	3	I/O I	EX1IN: [Fast External Interrupt 1] Input (default pin), MRST1: [SSC1] Master-Receive/Slave-Transmit In/Out. CC6POS2: [CAPCOM6] Position 2 Input,
P1H.3	3	I/O I	EX2IN: [Fast External Interrupt 2] Input (default pin), MTSR1: [SSC1] Master-Transmit/Slave-Receive Out/Inp. T7IN: [CAPCOM2] Timer T7 Count Input,
P1H.4	5	I/O I	SCLK1: [SSC1] Master Clock Output / Slave Clock Input, EX3IN: [Fast External Interrupt 3] Input (default pin), CC24IO: [CAPCOM2] CC24 Capture Inp./Compare Outp.,
P1H.5	6	I/O I	EX4IN: [Fast External Interrupt 4] Input (default pin) CC25IO: [CAPCOM2] CC25 Capture Inp./Compare Outp., EX5IN: [Fast External Interrupt 5] Input (default pin)
			<i>Note: At the end of an external reset P1H.4 and P1H.5 also may input startup configuration values</i>

3 Functional Description

The architecture of the XC164CM combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a very well-balanced way. In addition, the on-chip memory blocks allow the design of compact systems-on-silicon with maximum performance (computing, control, communication).

The on-chip memory blocks (program code-memory and SRAM, dual-port RAM, data SRAM) and the set of generic peripherals are connected to the CPU via separate buses. Another bus, the LXBus, connects additional on-chip resources (see [Figure 3](#)).

This bus structure enhances the overall system performance by enabling the concurrent operation of several subsystems of the XC164CM.

The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the XC164CM.

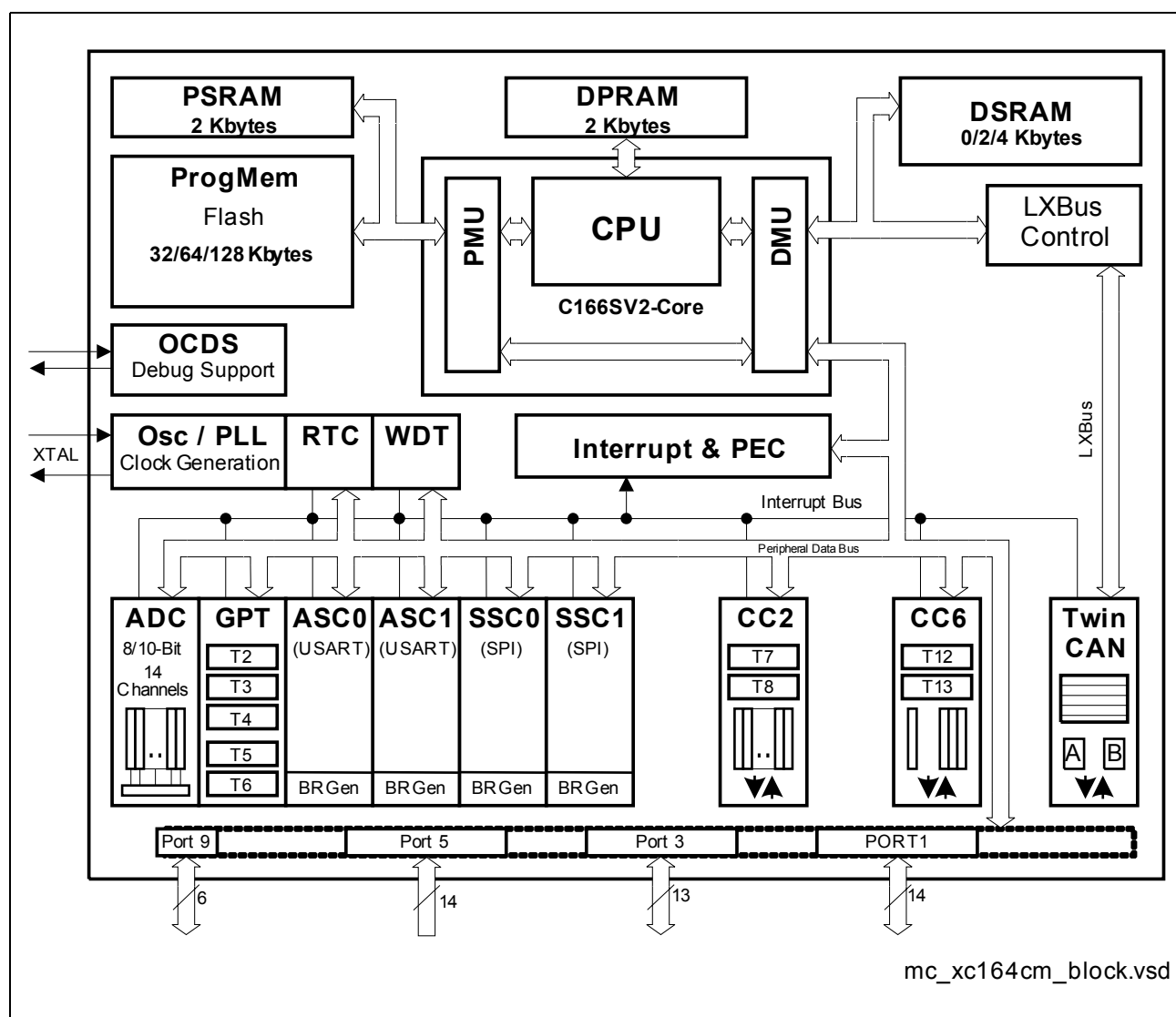


Figure 3 Block Diagram

3.3 Interrupt System

With an interrupt response time of typically 8 CPU clocks (in case of internal program execution), the XC164CM is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the XC164CM supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source, or the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The XC164CM has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bit field exists for each of the possible interrupt nodes. Via its related register, each node can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt nodes has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge, or both edges).

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

Table 4 shows all of the possible XC164CM interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not assigned to peripherals (unassigned nodes), may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).

Functional Description

The XC164CM also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called 'Hardware Traps'. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 5 shows all of the possible exceptions or error conditions that can arise during run-time:

Table 5 Hardware Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location ¹⁾	Trap Number	Trap Priority
Reset Functions: <ul style="list-style-type: none"> Hardware Reset Software Reset W-dog Timer Overflow 	—	RESET RESET RESET	xx'0000 _H xx'0000 _H xx'0000 _H	00 _H 00 _H 00 _H	III III III
Class A Hardware Traps: <ul style="list-style-type: none"> Non-Maskable Interrupt Stack Overflow Stack Underflow Software Break 	NMI STKOF STKUF SOFTBRK	NMITRAP STOTRAP STUTRAP SBRKTRAP	xx'0008 _H xx'0010 _H xx'0018 _H xx'0020 _H	02 _H 04 _H 06 _H 08 _H	II II II II
Class B Hardware Traps: <ul style="list-style-type: none"> Undefined Opcode PMI Access Error Protected Instruction Fault Illegal Word Operand Access 	UNDOPC PACER PRTFLT ILLOPA	BTRAP BTRAP BTRAP BTRAP	xx'0028 _H xx'0028 _H xx'0028 _H xx'0028 _H	0A _H 0A _H 0A _H 0A _H	I I I I
Reserved	—	—	[2C _H - 3C _H]	[0B _H - 0F _H]	—
Software Traps <ul style="list-style-type: none"> TRAP Instruction 	—	—	Any [xx'0000 _H - xx'01FC _H] in steps of 4 _H	Any [00 _H - 7F _H]	Current CPU Priority

1) Register VECSEG defines the segment where the vector table is located to.
 Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

Functional Description

register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

3.7 General Purpose Timer (GPT12E) Unit

The GPT12E unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e.g. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

3.8 Real Time Clock

The Real Time Clock (RTC) module of the XC164CM is directly clocked via a separate clock driver with the prescaled on-chip main oscillator frequency ($f_{\text{RTC}} = f_{\text{OSCM}}/32$). It is therefore independent from the selected clock generation mode of the XC164CM.

The RTC basically consists of a chain of divider blocks:

- A selectable 8:1 divider (on - off)
- The reloadable 16-bit timer T14
- The 32-bit RTC timer block (accessible via registers RTCH and RTCL), made of:
 - a reloadable 10-bit timer
 - a reloadable 6-bit timer
 - a reloadable 6-bit timer
 - a reloadable 10-bit timer

All timers count up. Each timer can generate an interrupt request. All requests are combined to a common node request.

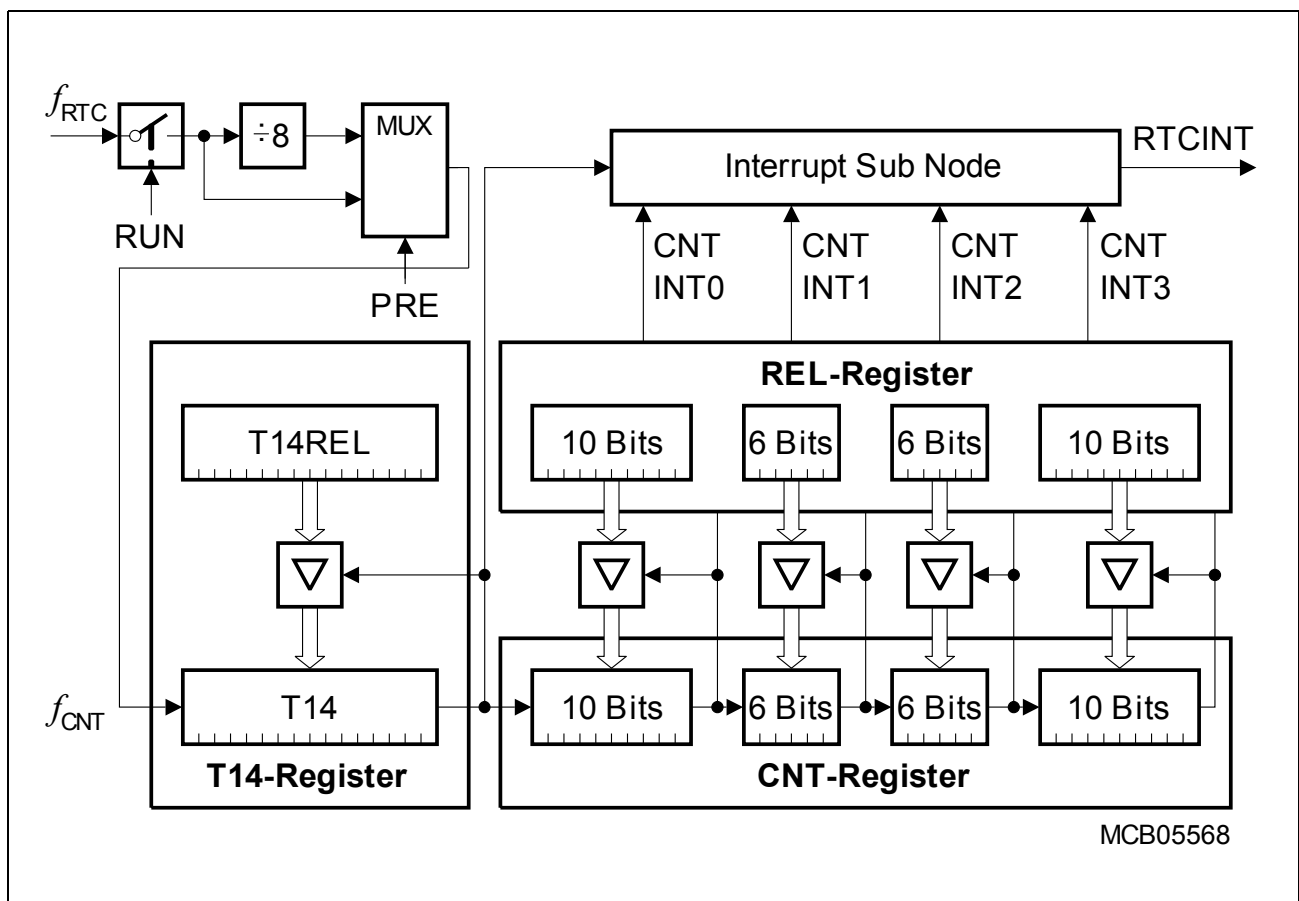


Figure 9 RTC Block Diagram

Note: The registers associated with the RTC are not affected by a reset in order to maintain the correct system time even when intermediate resets are executed.

3.10 Asynchronous/Synchronous Serial Interfaces (ASC0/ASC1)

The Asynchronous/Synchronous Serial Interfaces ASC0/ASC1 (USARTs) provide serial communication with other microcontrollers, processors, terminals or external peripheral components. They are upward compatible with the serial ports of the Infineon 8-bit microcontroller families and support full-duplex asynchronous communication and half-duplex synchronous communication. A dedicated baudrate generator with a fractional divider precisely generates all standard baud rates without oscillator tuning. For transmission, reception, error handling, and baud rate detection 5 separate interrupt vectors are provided.

In asynchronous mode, 8- or 9-bit data frames (with optional parity bit) are transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data plus wake-up bit mode). IrDA data transmissions up to 115.2 kbit/s with fixed or programmable IrDA pulse width are supported.

In synchronous mode, bytes (8 bits) are transmitted or received synchronously to a shift clock which is generated by the ASC0/1. The LSB is always shifted first.

In both modes, transmission and reception of data is FIFO-buffered. An autobaud detection unit allows to detect asynchronous data frames with its baudrate and mode with automatic initialization of the baudrate generator and the mode control bits.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. A parity bit can automatically be generated on transmission or be checked on reception. Framing error detection allows to recognize data frames with missing stop bits. An overrun error will be generated, if the last character received has not been read out of the receive buffer register at the time the reception of a new character is complete.

Summary of Features

- Full-duplex asynchronous operating modes
 - 8- or 9-bit data frames, LSB first, one or two stop bits, parity generation/checking
 - Baudrate from 2.5 Mbit/s to 0.6 bit/s (@ 40 MHz)
 - Multiprocessor mode for automatic address/data byte detection
 - Support for IrDA data transmission/reception up to max. 115.2 kbit/s (@ 40 MHz)
 - Auto baudrate detection
- Half-duplex 8-bit synchronous operating mode at 5 Mbit/s to 406.9 bit/s (@ 40 MHz)
- Buffered transmitter/receiver with FIFO support (8 entries per direction)
- Loop-back option available for testing purposes
- Interrupt generation on transmitter buffer empty condition, last bit transmitted condition, receive buffer full condition, error condition (frame, parity, overrun error), start and end of an autobaud detection

3.11 High Speed Synchronous Serial Channels (SSC0/SSC1)

The High Speed Synchronous Serial Channels SSC0/SSC1 support full-duplex and half-duplex synchronous communication. It may be configured so it interfaces with serially linked peripheral components, full SPI functionality is supported.

A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling three separate interrupt vectors are provided.

The SSC transmits or receives characters of 2 ... 16 bits length synchronously to a shift clock which can be generated by the SSC (master mode) or by an external master (slave mode). The SSC can start shifting with the LSB or with the MSB and allows the selection of shifting and latching clock edges as well as the clock polarity.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. Transmit error and receive error supervise the correct handling of the data buffer. Phase error and baudrate error detect incorrect serial data.

Summary of Features

- Master or Slave mode operation
- Full-duplex or Half-duplex transfers
- Baudrate generation from 20 Mbit/s to 305.18 bit/s (@ 40 MHz)
- Flexible data format
 - Programmable number of data bits: 2 to 16 bits
 - Programmable shift direction: LSB-first or MSB-first
 - Programmable clock polarity: idle low or idle high
 - Programmable clock/data phase: data shift with leading or trailing clock edge
- Loop back option available for testing purposes
- Interrupt generation on transmitter buffer empty condition, receive buffer full condition, error condition (receive, phase, baudrate, transmit error)
- Three pin interface with flexible SSC pin configuration

Summary of Features

- CAN functionality according to CAN specification V2.0 B active
- Data transfer rate up to 1 Mbit/s
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality and Basic CAN functionality for each message object
- 32 flexible message objects
 - Assignment to one of the two CAN nodes
 - Configuration as transmit object or receive object
 - Concatenation to a 2-, 4-, 8-, 16-, or 32-message buffer with FIFO algorithm
 - Handling of frames with 11-bit or 29-bit identifiers
 - Individual programmable acceptance mask register for filtering for each object
 - Monitoring via a frame counter
 - Configuration for Remote Monitoring Mode
- Up to eight individually programmable interrupt nodes can be used
- CAN Analyzer Mode for bus monitoring is implemented

3.13 LXBus Controller (EBC)

The EBC only controls accesses to resources connected to the on-chip LXBus. The LXBus is an internal representation of the external bus and allows accessing integrated peripherals and modules in the same way as external components.

The TwinCAN module is connected and accessed via the LXBus.

Functional Description
Table 8 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
ROL/ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2 / 4
MOVBS/Z	Move byte operand to word op. with sign/zero extension	2 / 4
JMPA/I/R	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
JB(C)	Jump relative if direct bit is set (and clear bit)	4
JNB(S)	Jump relative if direct bit is not set (and set bit)	4
CALLA/I/R	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH/POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET(P)	Return from intra-segment subroutine (and pop direct word register from system stack)	2
RETS	Return from inter-segment subroutine	2
RETI	Return from interrupt service subroutine	2
SBRK	Software Break	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Enter Power Down Mode (supposes $\overline{\text{NMI}}$ -pin being low)	4
SRVWDT	Service Watchdog Timer	4
DISWDT/ENWDT	Disable/Enable Watchdog Timer	4
EINIT	End-of-Initialization Register Lock	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2 / 4

Functional Description
Table 8 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
NOP	Null operation	2
CoMUL/CoMAC	Multiply (and accumulate)	4
CoADD/CoSUB	Add/Subtract	4
Co(A)SHR	(Arithmetic) Shift right	4
CoSHL	Shift left	4
CoLOAD/STORE	Load accumulator/Store MAC register	4
CoCMP	Compare	4
CoMAX/MIN	Maximum/Minimum	4
CoABS/CoRND	Absolute value/Round accumulator	4
CoMOV	Data move	4
CoNEG/NOP	Negate accumulator/Null operation	4

Electrical Parameters
Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XC164CM. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 10 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Digital supply voltage for the core	V_{DDI}	2.35	2.7	V	Active mode, $f_{CPU} = f_{CPUmax}^{1)}$
Digital supply voltage for IO pads	V_{DDP}	4.4	5.5	V	Active mode ²⁾³⁾
Supply Voltage Difference	ΔV_{DD}	-0.5	–	V	$V_{DDP} - V_{DDI}^{4)}$
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	-5	5	mA	Per IO pin ⁵⁾⁶⁾
		-2	5	mA	Per analog input pin ⁵⁾⁶⁾
Overload current coupling factor for analog inputs ⁷⁾	K_{OVA}	–	1.0×10^{-4}	–	$I_{OV} > 0$
		–	1.5×10^{-3}	–	$I_{OV} < 0$
Overload current coupling factor for digital I/O pins ⁷⁾	K_{OVD}	–	5.0×10^{-3}	–	$I_{OV} > 0$
		–	1.0×10^{-2}	–	$I_{OV} < 0$
Absolute sum of overload currents	$\Sigma I_{OV} $	–	50	mA	⁶⁾
External Load Capacitance	C_L	–	50	pF	Pin drivers in default mode ⁸⁾
Ambient temperature	T_A	0	70	°C	SAB-XC164...
		-40	85	°C	SAF-XC164...
		-40	125	°C	SAK-XC164...

1) $f_{CPUmax} = 40$ MHz for devices marked ... 40F, $f_{CPUmax} = 20$ MHz for devices marked ... 20F.

2) External circuitry must guarantee low-level at the \overline{RSTIN} pin at least until both power supply voltages have reached the operating range.

3) The specified voltage range is allowed for operation. The range limits may be reached under extreme operating conditions. However, specified parameters, such as leakage currents, refer to the standard operating voltage range of $V_{DDP} = 4.75$ V to 5.25 V.

4) This limitation must be fulfilled under all operating conditions including power-ramp-up, power-ramp-down, and power-save modes.

Electrical Parameters
4.2 DC Parameters

These parameters are static or average values, which may be exceeded during switching transitions (e.g. output current).

Table 11 DC Characteristics (Operating Conditions apply)¹⁾

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Input low voltage TTL (all except XTAL1)	V_{IL}	SR	-0.5	$0.2 \times V_{DDP} - 0.1$	V	—
Input low voltage XTAL1 ²⁾	V_{ILC}	SR	-0.5	$0.3 \times V_{DDI}$	V	—
Input low voltage (Special Threshold)	V_{ILS}	SR	-0.5	$0.45 \times V_{DDP}$	V	³⁾
Input high voltage TTL (all except XTAL1)	V_{IH}	SR	$0.2 \times V_{DDP} + 0.9$	$V_{DDP} + 0.5$	V	—
Input high voltage XTAL1 ²⁾	V_{IHC}	SR	$0.7 \times V_{DDI}$	$V_{DDI} + 0.5$	V	—
Input high voltage (Special Threshold)	V_{IHS}	SR	$0.8 \times V_{DDP} - 0.2$	$V_{DDP} + 0.5$	V	³⁾
Input Hysteresis (Special Threshold)	HYS		$0.04 \times V_{DDP}$	—	V	V_{DDP} in [V], Series resistance = 0Ω ³⁾
Output low voltage	V_{OL}	CC	—	1.0	V	$I_{OL} \leq I_{OLmax}$ ⁴⁾
			—	0.45	V	$I_{OL} \leq I_{OLnom}$ ⁴⁾⁵⁾
Output high voltage ⁶⁾	V_{OH}	CC	$V_{DDP} - 1.0$	—	V	$I_{OH} \geq I_{OHmax}$ ⁴⁾
			$V_{DDP} - 0.45$	—	V	$I_{OH} \geq I_{OHnom}$ ⁴⁾⁵⁾
Input leakage current (Port 5) ⁷⁾	I_{OZ1}	CC	—	± 300	nA	$0 V < V_{IN} < V_{DDP}$, $T_A \leq 125^\circ C$
				± 200	nA	$0 V < V_{IN} < V_{DDP}$, $T_A \leq 85^\circ C$ ¹²⁾
Input leakage current (all other ⁸⁾) ⁷⁾	I_{OZ2}	CC	—	± 500	nA	$0.45 V < V_{IN} < V_{DDP}$
Configuration pull-up current ⁹⁾	I_{CPUH} ¹⁰⁾		—	-10	μA	$V_{IN} = V_{IHmin}$
	I_{CPUL} ¹¹⁾		-100	—	μA	$V_{IN} = V_{ILmax}$

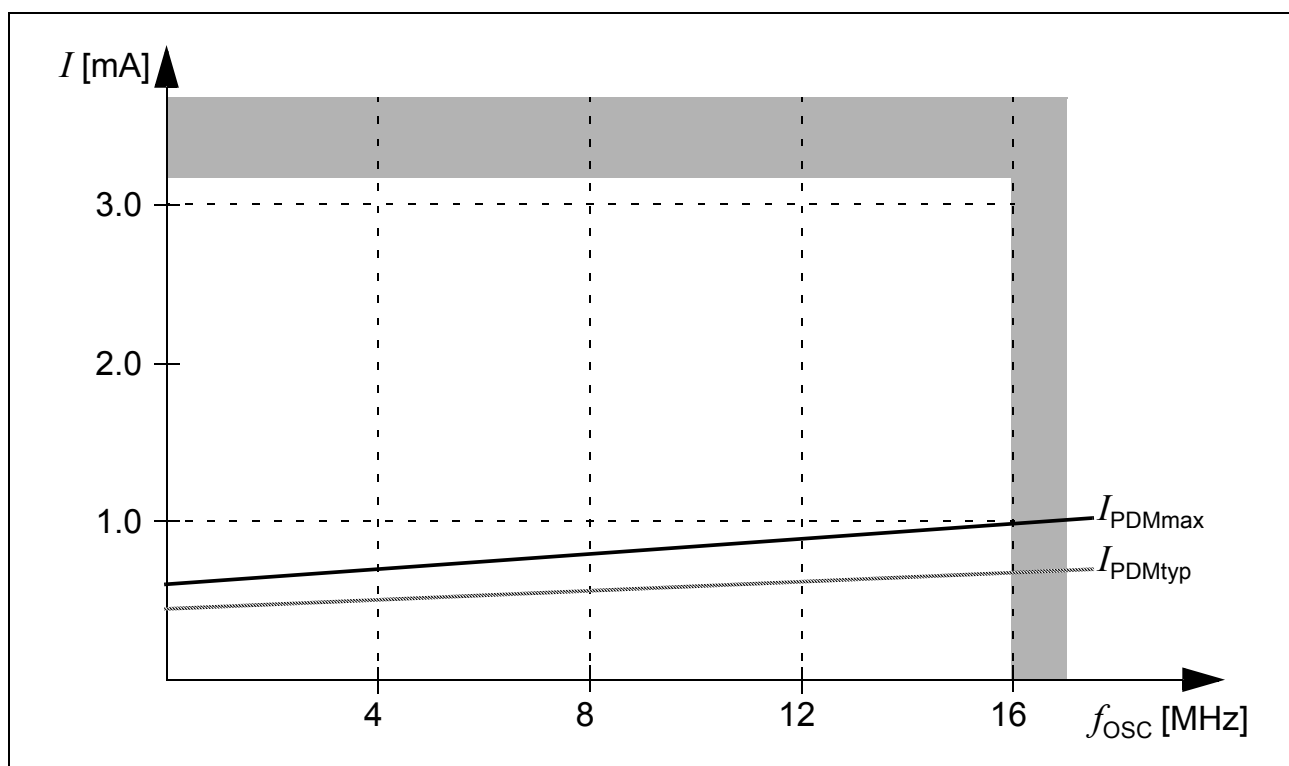


Figure 12 Sleep and Power Down Supply Current due to RTC and Oscillator Running, as a Function of Oscillator Frequency

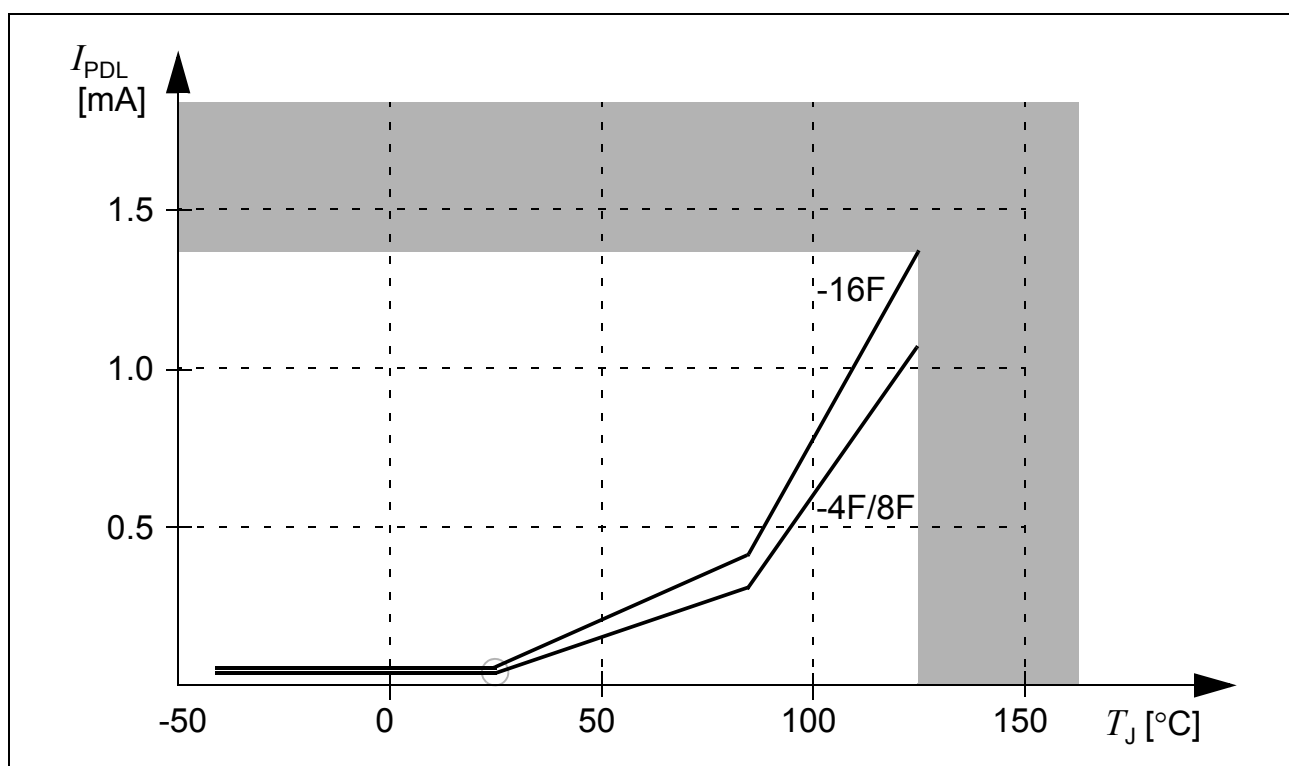


Figure 13 Sleep and Power Down Leakage Supply Current as a Function of Temperature

Electrical Parameters

- 2) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.
- 3) The limit values for f_{BC} must not be exceeded when selecting the peripheral frequency and the ADCTC setting.
- 4) This parameter includes the sample time t_S , the time for determining the digital result and the time to load the result register with the conversion result ($t_{SYS} = 1/f_{SYS}$).
Values for the basic clock t_{BC} depend on programming and can be taken from [Table 15](#).
When the post-calibration is switched off, the conversion time is reduced by $12 \times t_{BC}$.
- 5) The actual duration of the reset calibration depends on the noise on the reference signal. Conversions executed during the reset calibration increase the calibration time. The TUE for those conversions may be increased.
- 6) Not subject to production test - verified by design/characterization.
The given parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) reduced values can be used for calculations. At room temperature and nominal supply voltage the following typical values can be used:
 $C_{AINTyp} = 12 \text{ pF}$, $C_{AINStyp} = 7 \text{ pF}$, $R_{AINTyp} = 1.5 \text{ k}\Omega$, $C_{AREFTyp} = 15 \text{ pF}$, $C_{AREFStyp} = 13 \text{ pF}$, $R_{AREFTyp} = 0.7 \text{ k}\Omega$.

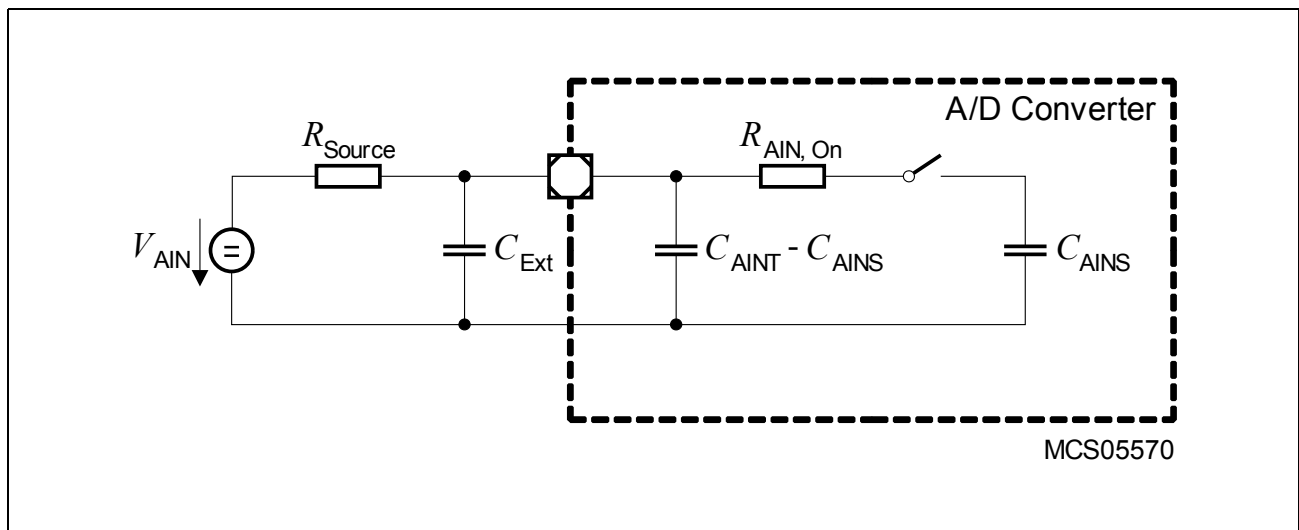


Figure 14 Equivalent Circuitry for Analog Inputs

Electrical Parameters

This is especially important for bus cycles using waitstates and e.g. for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler ($K = \text{PLLODIV} + 1$) to generate the master clock signal f_{MC} . Therefore, the number of VCO cycles can be represented as $K \times N$, where N is the number of consecutive f_{MC} cycles (TCM).

For a period of $N \times \text{TCM}$ the accumulated PLL jitter is defined by the deviation D_N :

$$D_N [\text{ns}] = \pm(1.5 + 6.32 \times N / f_{MC}); f_{MC} \text{ in [MHz]}, N = \text{number of consecutive TCMs.}$$

So, for a period of 3 TCMs @ 20 MHz and $K = 12$: $D_3 = \pm(1.5 + 6.32 \times 3 / 20) = 2.448 \text{ ns}$.

This formula is applicable for $K \times N < 95$. For longer periods the $K \times N = 95$ value can be used. This steady value can be approximated by: $D_{N_{\max}} [\text{ns}] = \pm(1.5 + 600 / (K \times f_{MC}))$.

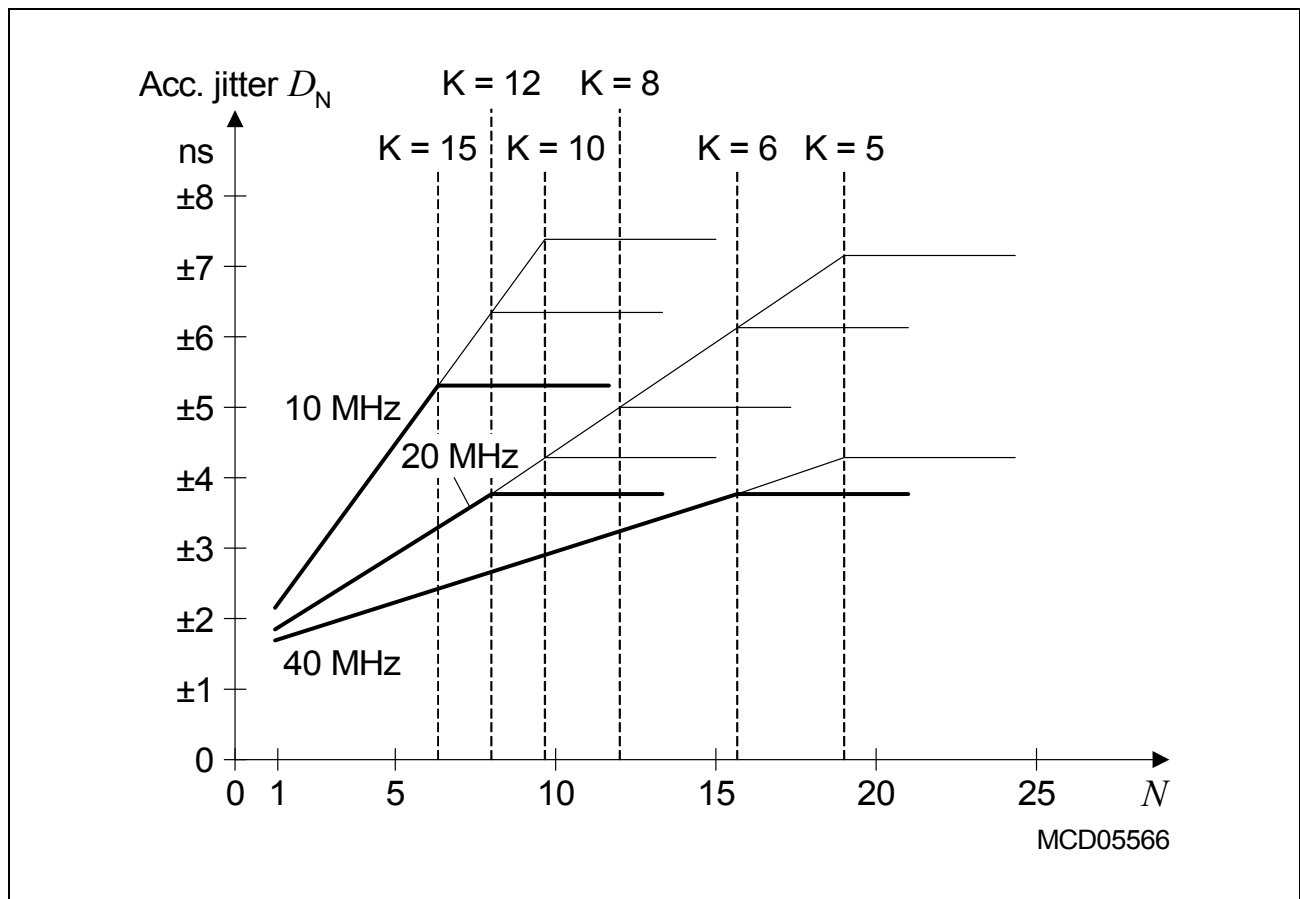


Figure 16 **Approximated Accumulated PLL Jitter**

Note: The bold lines indicate the minimum accumulated jitter which can be achieved by selecting the maximum possible output prescaler factor K.

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