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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Last Time Buy
Core Processor	C166SV2
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	47
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 14x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-LQFP-64-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc164cm16f40fbakxqma1

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Summary of Features

- Idle, Sleep, and Power Down Modes with Flexible Power Management
- Programmable Watchdog Timer and Oscillator Watchdog
- Up to 47 General Purpose I/O Lines, partly with Selectable Input Thresholds and Hysteresis
- On-Chip Bootstrap Loader
- On-Chip Debug Support via JTAG Interface
- 64-Pin Green LQFP Package for the -16F derivatives, 0.5 mm (19.7 mil) pitch (RoHS compliant)
- 64-Pin TQFP Package for the -4F/8F derivatives, 0.5 mm (19.7 mil) pitch (RoHS compliant)

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the XC164CM please refer to your responsible sales representative or your local distributor.

This document describes several derivatives of the XC164CM group. [Table 1](#) enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

For simplicity all versions are referred to by the term **XC164CM** throughout this document.

Summary of Features
Table 1 XC164CM Derivative Synopsis

Derivative ¹⁾	Temp. Range	Program Memory	On-Chip RAM	Interfaces
SAK-XC164CM-16F40F SAK-XC164CM-16F20F	-40 to 125 °C	128 Kbytes Flash	2 Kbytes DPRAM, 4 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1
SAF-XC164CM-16F40F SAF-XC164CM-16F20F	-40 to 85 °C	128 Kbytes Flash	2 Kbytes DPRAM, 4 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1
SAK-XC164CM-8F40F SAK-XC164CM-8F20F	-40 to 125 °C	64 Kbytes Flash	2 Kbytes DPRAM, 2 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1
SAF-XC164CM-8F40F SAF-XC164CM-8F20F	-40 to 85 °C	64 Kbytes Flash	2 Kbytes DPRAM, 2 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1
SAK-XC164CM-4F40F SAK-XC164CM-4F20F	-40 to 125 °C	32 Kbytes Flash	2 Kbytes DPRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1
SAF-XC164CM-4F40F SAF-XC164CM-4F20F	-40 to 85 °C	32 Kbytes Flash	2 Kbytes DPRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1

1) This Data Sheet is valid for:
 devices starting with and including design step BA for the -16F derivatives, and for
 devices starting with and including design step AA for -4F/8F derivatives.

3 Functional Description

The architecture of the XC164CM combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a very well-balanced way. In addition, the on-chip memory blocks allow the design of compact systems-on-silicon with maximum performance (computing, control, communication).

The on-chip memory blocks (program code-memory and SRAM, dual-port RAM, data SRAM) and the set of generic peripherals are connected to the CPU via separate buses. Another bus, the LxBus, connects additional on-chip resources (see [Figure 3](#)).

This bus structure enhances the overall system performance by enabling the concurrent operation of several subsystems of the XC164CM.

The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the XC164CM.

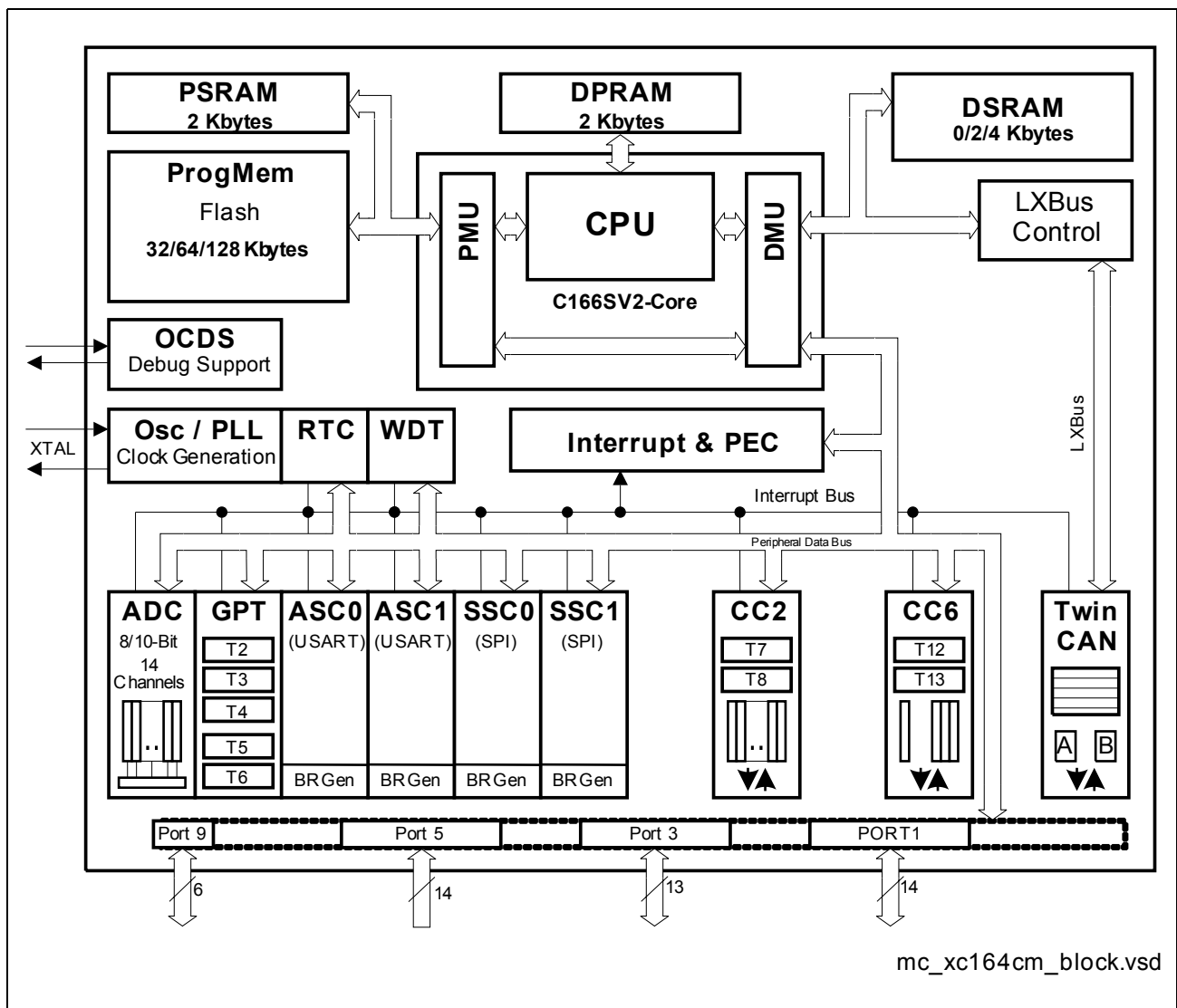


Figure 3 Block Diagram

Functional Description

- 2) Not defined register locations return a trap code (1E9B_H).
- 3) Depends on the respective derivative. See [Table 1 “XC164CM Derivative Synopsis” on Page 6](#).

Functional Description

example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. Also multiplication and most MAC instructions execute in one single cycle. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: for example, a 32-/16-bit division is started within 4 cycles, while the remaining 15 cycles are executed in the background. Another pipeline optimization, the branch target prediction, allows eliminating the execution time of branch instructions if the prediction was correct.

The CPU has a register context consisting of up to three register banks with 16 word wide GPRs each at its disposal. One of these register banks is physically allocated within the on-chip DPRAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at any time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 32 Kwords is provided as a storage for temporary data. The system stack can be allocated to any location within the address space (preferably in the on-chip RAM area), and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient XC164CM instruction set which includes the following instruction classes:

- Standard Arithmetic Instructions
- DSP-Oriented Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

Functional Description
Table 4 XC164CM Interrupt Nodes

Source of Interrupt or PEC Service Request	Control Register	Vector Location ¹⁾	Trap Number
EX0IN	CC1_CC8IC	xx'0060 _H	18 _H / 24 _D
EX1IN	CC1_CC9IC	xx'0064 _H	19 _H / 25 _D
EX2IN	CC1_CC10IC	xx'0068 _H	1A _H / 26 _D
EX3IN	CC1_CC11IC	xx'006C _H	1B _H / 27 _D
EX4IN	CC1_CC12IC	xx'0070 _H	1C _H / 28 _D
EX5IN	CC1_CC13IC	xx'0074 _H	1D _H / 29 _D
CAPCOM Register 16	CC2_CC16IC	xx'00C0 _H	30 _H / 48 _D
CAPCOM Register 17	CC2_CC17IC	xx'00C4 _H	31 _H / 49 _D
CAPCOM Register 18	CC2_CC18IC	xx'00C8 _H	32 _H / 50 _D
CAPCOM Register 19	CC2_CC19IC	xx'00CC _H	33 _H / 51 _D
CAPCOM Register 20	CC2_CC20IC	xx'00D0 _H	34 _H / 52 _D
CAPCOM Register 21	CC2_CC21IC	xx'00D4 _H	35 _H / 53 _D
CAPCOM Register 22	CC2_CC22IC	xx'00D8 _H	36 _H / 54 _D
CAPCOM Register 23	CC2_CC23IC	xx'00DC _H	37 _H / 55 _D
CAPCOM Register 24	CC2_CC24IC	xx'00E0 _H	38 _H / 56 _D
CAPCOM Register 25	CC2_CC25IC	xx'00E4 _H	39 _H / 57 _D
CAPCOM Register 26	CC2_CC26IC	xx'00E8 _H	3A _H / 58 _D
CAPCOM Register 27	CC2_CC27IC	xx'00EC _H	3B _H / 59 _D
CAPCOM Register 28	CC2_CC28IC	xx'00F0 _H	3C _H / 60 _D
CAPCOM Register 29	CC2_CC29IC	xx'0110 _H	44 _H / 68 _D
CAPCOM Register 30	CC2_CC30IC	xx'0114 _H	45 _H / 69 _D
CAPCOM Register 31	CC2_CC31IC	xx'0118 _H	46 _H / 70 _D
CAPCOM Timer 7	CC2_T7IC	xx'00F4 _H	3D _H / 61 _D
CAPCOM Timer 8	CC2_T8IC	xx'00F8 _H	3E _H / 62 _D
GPT1 Timer 2	GPT12E_T2IC	xx'0088 _H	22 _H / 34 _D
GPT1 Timer 3	GPT12E_T3IC	xx'008C _H	23 _H / 35 _D
GPT1 Timer 4	GPT12E_T4IC	xx'0090 _H	24 _H / 36 _D
GPT2 Timer 5	GPT12E_T5IC	xx'0094 _H	25 _H / 37 _D
GPT2 Timer 6	GPT12E_T6IC	xx'0098 _H	26 _H / 38 _D

3.4 On-Chip Debug Support (OCDS)

The On-Chip Debug Support system provides a broad range of debug and emulation features built into the XC164CM. The user software running on the XC164CM can thus be debugged within the target system environment.

The OCDS is controlled by an external debugging device via the debug interface, consisting of the IEEE-1149-conforming JTAG port and a break interface. The debugger controls the OCDS via a set of dedicated registers accessible via the JTAG interface. Additionally, the OCDS system can be controlled by the CPU, e.g. by a monitor program. An injection interface allows the execution of OCDS-generated instructions by the CPU.

Multiple breakpoints can be triggered by on-chip hardware, by software, or by an external trigger input. Single stepping is supported as well as the injection of arbitrary instructions and read/write access to the complete internal address space. A breakpoint trigger can be answered with a CPU-halt, a monitor call, a data transfer, or/and the activation of an external signal.

Tracing data can be obtained via the JTAG interface.

The debug interface uses a set of 6 interface signals (4 JTAG lines, 2 break lines) to communicate with external circuitry. These interface signals are realized as alternate functions on Port 3 pins.

Functional Description

register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

3.6 The Capture/Compare Unit CAPCOM6

The CAPCOM6 unit supports generation and control of timing sequences on up to three 16-bit capture/compare channels plus one independent 10-bit compare channel.

In compare mode the CAPCOM6 unit provides two output signals per channel which have inverted polarity and non-overlapping pulse transitions (deadtime control). The compare channel can generate a single PWM output signal and is further used to modulate the capture/compare output signals.

In capture mode the contents of compare timer T12 is stored in the capture registers upon a signal transition at pins CCx.

Compare timers T12 (16-bit) and T13 (10-bit) are free running timers which are clocked by the prescaled system clock.

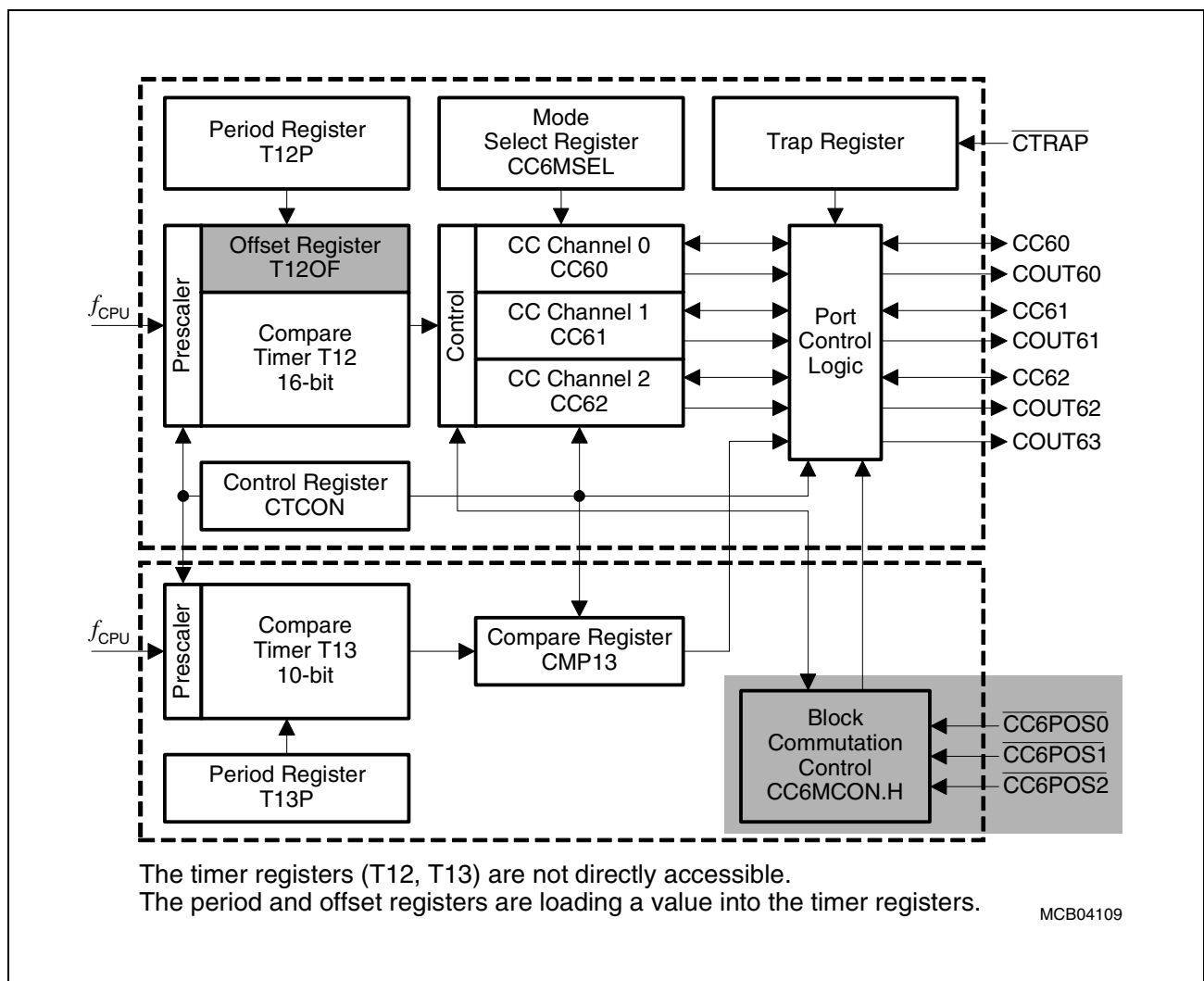


Figure 6 CAPCOM6 Block Diagram

For motor control applications both subunits may generate versatile multichannel PWM signals which are basically either controlled by compare timer T12 or by a typical hall sensor pattern at the interrupt inputs (block commutation).

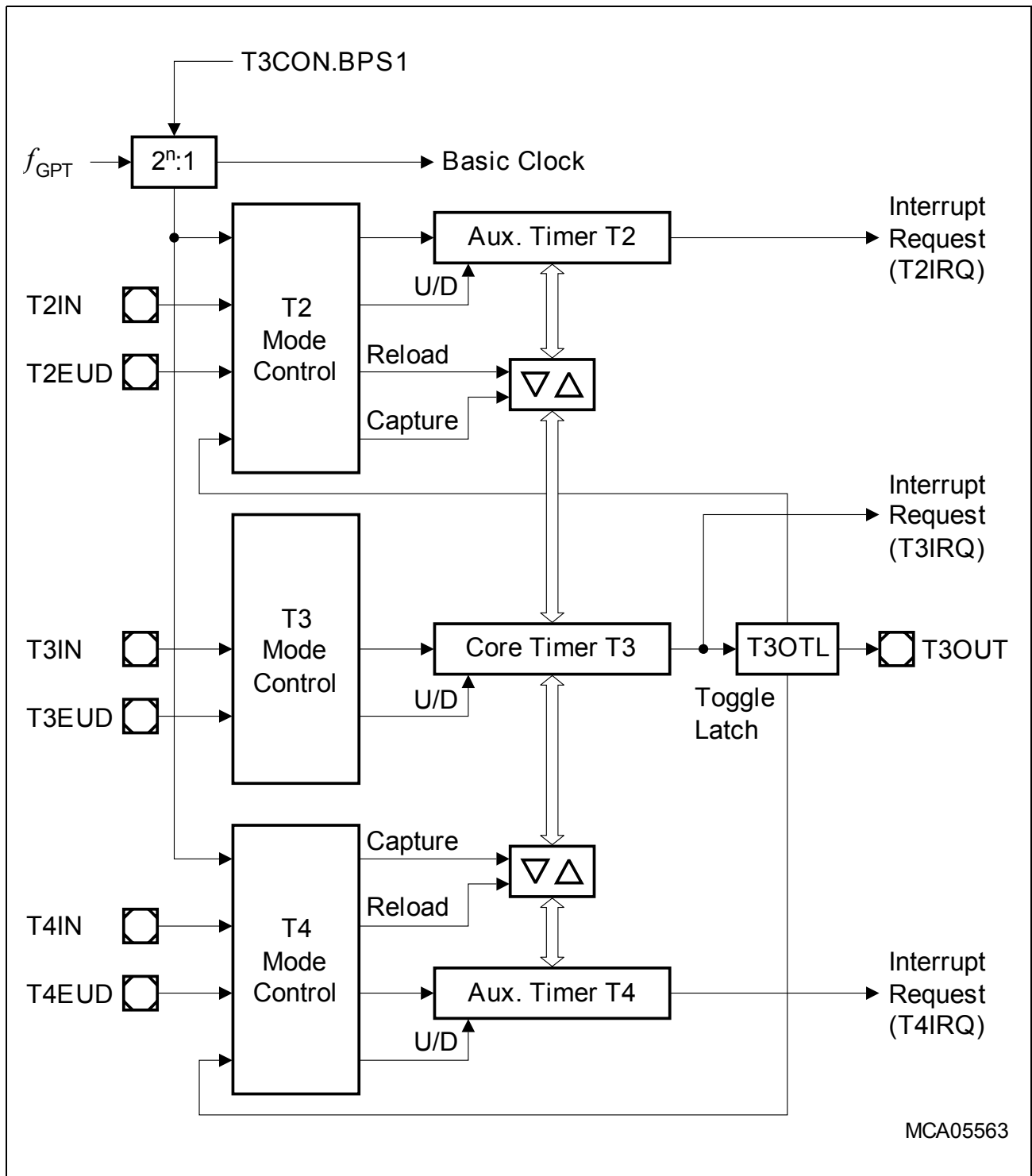


Figure 7 Block Diagram of GPT1

With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The

Functional Description

The RTC module can be used for different purposes:

- System clock to determine the current time and date, optionally during idle mode, sleep mode, and power down mode
- Cyclic time based interrupt, to provide a system time tick independent of CPU frequency and other resources, e.g. to wake up regularly from idle mode
- 48-bit timer for long term measurements (maximum timespan is > 100 years)
- Alarm interrupt for wake-up on a defined time

3.9 A/D Converter

For analog signal measurement, a 10-bit A/D converter with 14 multiplexed input channels and a sample and hold circuit has been integrated on-chip. It uses the method of successive approximation. The sample time (for loading the capacitors) and the conversion time is programmable (in two modes) and can thus be adjusted to the external circuitry. The A/D converter can also operate in 8-bit conversion mode, where the conversion time is further reduced.

Overrun error detection/protection is provided for the conversion result register (ADDAT): either an interrupt request will be generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended in such a case until the previous result has been read.

For applications which require less analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converter of the XC164CM supports four different conversion modes. In the standard Single Channel conversion mode, the analog level on a specified channel is sampled once and converted to a digital result. In the Single Channel Continuous mode, the analog level on a specified channel is repeatedly sampled and converted without software intervention. In the Auto Scan mode, the analog levels on a prespecified number of channels are sequentially sampled and converted. In the Auto Scan Continuous mode, the prespecified channels are repeatedly sampled and converted. In addition, the conversion of a specific channel can be inserted (injected) into a running sequence without disturbing this sequence. This is called Channel Injection Mode.

The Peripheral Event Controller (PEC) may be used to automatically store the conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer.

After each reset and also during normal operation the ADC automatically performs calibration cycles. This automatic self-calibration constantly adjusts the converter to changing operating conditions (e.g. temperature) and compensates process variations.

These calibration cycles are part of the conversion cycle, so they do not affect the normal operation of the A/D converter.

In order to decouple analog inputs from digital noise and to avoid input trigger noise those pins used for analog input can be disconnected from the digital input stages under software control. This can be selected for each pin separately via register P5DIDIS (Port 5 Digital Input Disable).

The Auto-Power-Down feature of the A/D converter minimizes the power consumption when no conversion is in progress.

Summary of Features

- CAN functionality according to CAN specification V2.0 B active
- Data transfer rate up to 1 Mbit/s
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality and Basic CAN functionality for each message object
- 32 flexible message objects
 - Assignment to one of the two CAN nodes
 - Configuration as transmit object or receive object
 - Concatenation to a 2-, 4-, 8-, 16-, or 32-message buffer with FIFO algorithm
 - Handling of frames with 11-bit or 29-bit identifiers
 - Individual programmable acceptance mask register for filtering for each object
 - Monitoring via a frame counter
 - Configuration for Remote Monitoring Mode
- Up to eight individually programmable interrupt nodes can be used
- CAN Analyzer Mode for bus monitoring is implemented

3.13 LXBus Controller (EBC)

The EBC only controls accesses to resources connected to the on-chip LXBus. The LXBus is an internal representation of the external bus and allows accessing integrated peripherals and modules in the same way as external components.

The TwinCAN module is connected and accessed via the LXBus.

3.16 Parallel Ports

The XC164CM provides up to 47 I/O lines which are organized into three input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of some I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

The edge characteristics (shape) and driver characteristics (output current) of the port drivers can be selected via registers POCONx.

The input threshold of some ports is selectable (TTL or CMOS like), where the special CMOS like input threshold reduces noise sensitivity due to the input hysteresis. The input threshold may be selected individually for each byte of the respective ports.

All port lines have programmable alternate input or output functions associated with them. All port lines that are not used for these alternate functions may be used as general purpose IO lines.

Table 7 Summary of the XC164CM's Parallel Ports

Port	Control	Alternate Functions
PORT1	Pad drivers	Capture inputs or compare outputs, Serial interface lines
Port 3	Pad drivers, Open drain, Input threshold	Timer control signals, serial interface lines, System clock output CLKOUT (or FOUT)
Port 5	–	Analog input channels to the A/D converter, Timer control signals
Port 9	Pad drivers, Open drain, Input threshold	Capture inputs or compare outputs
		CAN interface lines ¹⁾

1) Can be assigned by software.

4 Electrical Parameters

The operating range for the XC164CM is defined by its electrical parameters. For proper operation the indicated limitations must be respected when designing a system.

4.1 General Parameters

These parameters are valid for all subsequent descriptions, unless otherwise noted.

Table 9 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Storage temperature	T_{ST}	-65	150	°C	1)
Junction temperature	T_J	-40	150	°C	Under bias
Voltage on V_{DDI} pins with respect to ground (V_{SS})	V_{DDI}	-0.5	3.25	V	–
Voltage on V_{DDP} pins with respect to ground (V_{SS})	V_{DDP}	-0.5	6.2	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	$V_{DDP} + 0.5$	V	2)
Input current on any pin during overload condition	–	-10	10	mA	–
Absolute sum of all input currents during overload condition	–	–	100	mA	–

1) Moisture Sensitivity Level (MSL) 3, conforming to Jedec J-STD-020C for 260 °C.

2) Input pin XTAL1 belongs to the core voltage domain. Therefore, input voltages must be within the range defined for VDDI.

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Electrical Parameters

- 2) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.
- 3) The limit values for f_{BC} must not be exceeded when selecting the peripheral frequency and the ADCTC setting.
- 4) This parameter includes the sample time t_S , the time for determining the digital result and the time to load the result register with the conversion result ($t_{SYS} = 1/f_{SYS}$).
Values for the basic clock t_{BC} depend on programming and can be taken from [Table 15](#).
When the post-calibration is switched off, the conversion time is reduced by $12 \times t_{BC}$.
- 5) The actual duration of the reset calibration depends on the noise on the reference signal. Conversions executed during the reset calibration increase the calibration time. The TUE for those conversions may be increased.
- 6) Not subject to production test - verified by design/characterization.
The given parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) reduced values can be used for calculations. At room temperature and nominal supply voltage the following typical values can be used:
 $C_{AINTyp} = 12 \text{ pF}$, $C_{AINStyp} = 7 \text{ pF}$, $R_{AINTyp} = 1.5 \text{ k}\Omega$, $C_{AREFTyp} = 15 \text{ pF}$, $C_{AREFStyp} = 13 \text{ pF}$, $R_{AREFTyp} = 0.7 \text{ k}\Omega$.

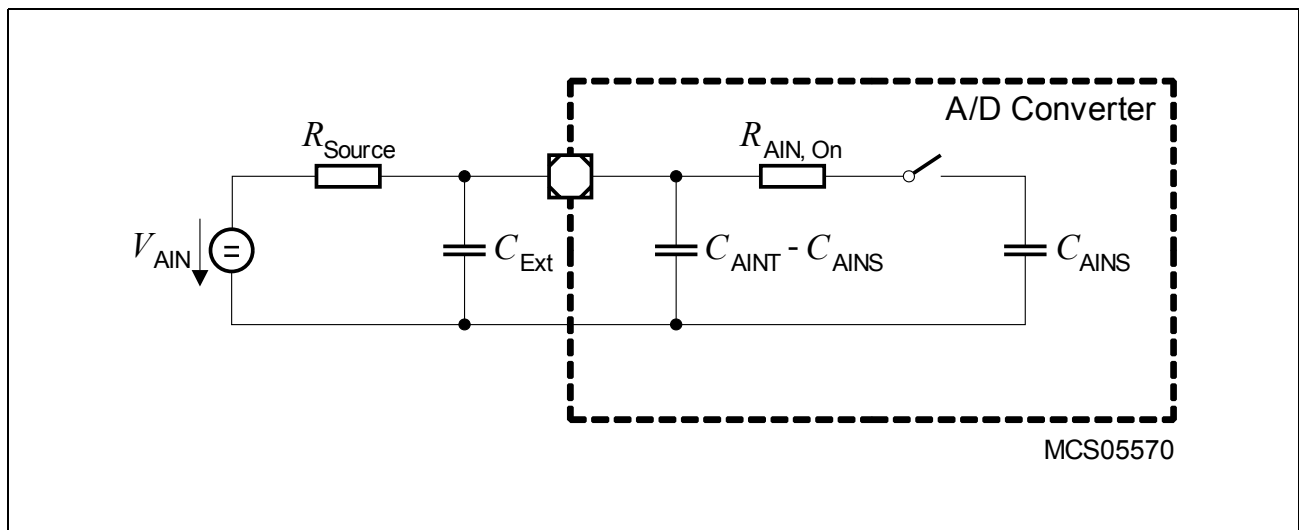


Figure 14 **Equivalent Circuitry for Analog Inputs**

Electrical Parameters

The used mechanism to generate the master clock is selected by register PLLCON.

CPU and EBC are clocked with the CPU clock signal f_{CPU} . The CPU clock can have the same frequency as the master clock ($f_{\text{CPU}} = f_{\text{MC}}$) or can be the master clock divided by two: $f_{\text{CPU}} = f_{\text{MC}} / 2$. This factor is selected by bit CPSYS in register SYSCON1.

The specification of the external timing (AC Characteristics) depends on the period of the CPU clock, called "TCP".

The other peripherals are supplied with the system clock signal f_{SYS} which has the same frequency as the CPU clock signal f_{CPU} .

Bypass Operation

When bypass operation is configured (PLLCTRL = 0x_B) the master clock is derived from the internal oscillator (input clock signal XTAL1) through the input- and output-prescalers:

$$f_{\text{MC}} = f_{\text{OSC}} / ((\text{PLLIDIV} + 1) \times (\text{PLLODIV} + 1)).$$

If both divider factors are selected as '1' (PLLIDIV = PLLODIV = '0') the frequency of f_{MC} directly follows the frequency of f_{OSC} so the high and low time of f_{MC} is defined by the duty cycle of the input clock f_{OSC} .

The lowest master clock frequency is achieved by selecting the maximum values for both divider factors:

$$f_{\text{MC}} = f_{\text{OSC}} / ((3 + 1) \times (14 + 1)) = f_{\text{OSC}} / 60.$$

Phase Locked Loop (PLL)

When PLL operation is configured (PLLCTRL = 11_B) the on-chip phase locked loop is enabled and provides the master clock. The PLL multiplies the input frequency by the factor **F** ($f_{\text{MC}} = f_{\text{OSC}} \times \mathbf{F}$) which results from the input divider, the multiplication factor, and the output divider ($\mathbf{F} = \text{PLLMUL} + 1 / (\text{PLLIDIV} + 1 \times \text{PLLODIV} + 1)$). The PLL circuit synchronizes the master clock to the input clock. This synchronization is done smoothly, i.e. the master clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{MC} is constantly adjusted so it is locked to f_{OSC} . The slight variation causes a jitter of f_{MC} which also affects the duration of individual TCMs.

The timing listed in the AC Characteristics refers to TCPs. Because f_{CPU} is derived from f_{MC} , the timing must be calculated using the minimum TCP possible under the respective circumstances.

The actual minimum value for TCP depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so it corresponds to the applied input frequency (crystal or oscillator) the relative deviation for periods of more than one TCP is lower than for one single TCP (see formula and [Figure 16](#)).

5.2 Flash Memory Parameters

The data retention time of the XC164CM's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Table 21 Flash Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Data retention time	t_{RET}	15	–	years	10^3 erase/program cycles
Flash Erase Endurance	N_{ER}	20×10^3	–	cycles	Data retention time 5 years