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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Last Time Buy
Core Processor	C166SV2
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	47
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 14x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-LQFP-64-4
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/xc164cm16f40fbakxuma1">https://www.e-xfl.com/product-detail/infineon-technologies/xc164cm16f40fbakxuma1</a>

# XC164CM

16-Bit Single-Chip Microcontroller  
with C166SV2 Core

Microcontrollers



Never stop thinking

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**Summary of Features**

- Idle, Sleep, and Power Down Modes with Flexible Power Management
- Programmable Watchdog Timer and Oscillator Watchdog
- Up to 47 General Purpose I/O Lines, partly with Selectable Input Thresholds and Hysteresis
- On-Chip Bootstrap Loader
- On-Chip Debug Support via JTAG Interface
- 64-Pin Green LQFP Package for the -16F derivatives, 0.5 mm (19.7 mil) pitch (RoHS compliant)
- 64-Pin TQFP Package for the -4F/8F derivatives, 0.5 mm (19.7 mil) pitch (RoHS compliant)

**Ordering Information**

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the XC164CM please refer to your responsible sales representative or your local distributor.

This document describes several derivatives of the XC164CM group. [Table 1](#) enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

For simplicity all versions are referred to by the term **XC164CM** throughout this document.

**Summary of Features**
**Table 1 XC164CM Derivative Synopsis**

Derivative <sup>1)</sup>	Temp. Range	Program Memory	On-Chip RAM	Interfaces
SAK-XC164CM-16F40F SAK-XC164CM-16F20F	-40 to 125 °C	128 Kbytes Flash	2 Kbytes DPRAM, 4 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1
SAF-XC164CM-16F40F SAF-XC164CM-16F20F	-40 to 85 °C	128 Kbytes Flash	2 Kbytes DPRAM, 4 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1
SAK-XC164CM-8F40F SAK-XC164CM-8F20F	-40 to 125 °C	64 Kbytes Flash	2 Kbytes DPRAM, 2 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1
SAF-XC164CM-8F40F SAF-XC164CM-8F20F	-40 to 85 °C	64 Kbytes Flash	2 Kbytes DPRAM, 2 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1
SAK-XC164CM-4F40F SAK-XC164CM-4F20F	-40 to 125 °C	32 Kbytes Flash	2 Kbytes DPRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1
SAF-XC164CM-4F40F SAF-XC164CM-4F20F	-40 to 85 °C	32 Kbytes Flash	2 Kbytes DPRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1

1) This Data Sheet is valid for:  
 devices starting with and including design step BA for the -16F derivatives, and for  
 devices starting with and including design step AA for -4F/8F derivatives.

**General Device Information**
**Table 2 Pin Definitions and Functions**

Sym- bol	Pin Num.	Input Outp.	Function
<u>RSTIN</u>	63	I	Reset Input with Schmitt-Trigger characteristics. A low-level at this pin while the oscillator is running resets the XC164CM. A spike filter suppresses input pulses < 10 ns. Input pulses > 100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles. <i>Note: The reset duration must be sufficient to let the hardware configuration signals settle. External circuitry must guarantee low-level at the <u>RSTIN</u> pin at least until both power supply voltages have reached the operating range.</i>
<u>NMI</u>	64	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the <u>NMI</u> pin must be low in order to force the XC164CM into power down mode. If <u>NMI</u> is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin <u>NMI</u> should be pulled high externally.
<b>Port 9</b>	43-48	IO	Port 9 is a 6-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 9 is selectable (standard or special). The following Port 9 pins also serve for alternate functions:
P9.0	43	I/O I	CC16IO: (CAPCOM2) CC16 Capture Inp./Compare Outp., CAN2_RxD: (CAN Node 2) Receive Data Input <sup>1)</sup> , EX5IN: (Fast External Interrupt 5) Input (alternate pin A)
P9.1	44	I/O O	CC17IO: (CAPCOM2) CC17 Capture Inp./Compare Outp., CAN2_TxD: (CAN Node 2) Transmit Data Output,
P9.2	45	I/O I	CC18IO: (CAPCOM2) CC18 Capture Inp./Compare Outp., CAN1_RxD: (CAN Node 1) Receive Data Input <sup>1)</sup> , EX4IN: (Fast External Interrupt 4) Input (alternate pin A)
P9.3	46	I/O O	CC19IO: (CAPCOM2) CC19 Capture Inp./Compare Outp., CAN1_TxD: (CAN Node 1) Transmit Data Output,
P9.4	47	I/O	CC20IO: (CAPCOM2) CC20 Capture Inp./Compare Outp.
P9.5	48	I/O	CC21IO: (CAPCOM2) CC21 Capture Inp./Compare Outp. <i>Note: At the end of an external reset P9.4 and P9.5 also may input startup configuration values.</i>

**General Device Information**
**Table 2 Pin Definitions and Functions (cont'd)**

Sym- bol	Pin Num.	Input Outp.	Function
<b>PORT1</b>	1-6, 49-56	IO	PORT1 consists of one 8-bit and one 6-bit bidirectional I/O port P1L and P1H. Each pin can be programmed for input (output driver in high-impedance state) or output. The following PORT1 pins also serve for alt. functions:
P1L.0	49	I/O	CC60: [CAPCOM6] Input / Output of Channel 0
P1L.1	50	O	COUT60: [CAPCOM6] Output of Channel 0
P1L.2	51	I/O	CC61: [CAPCOM6] Input / Output of Channel 1
P1L.3	52	O	COUT61: [CAPCOM6] Output of Channel 1
P1L.4	53	I/O	CC62: [CAPCOM6] Input / Output of Channel 2
P1L.5	54	O	COUT62: [CAPCOM6] Output of Channel 2
P1L.6	55	O	COUT63: Output of 10-bit Compare Channel
P1L.7	56	I	CTRAP: [CAPCOM6] Trap Input CTRAP is an input pin with an internal pull-up resistor. A low level on this pin switches the CAPCOM6 compare outputs to the logic level defined by software (if enabled).
P1H.0	1	I/O I I	CC22IO: [CAPCOM2] CC22 Capture Inp./Compare Outp. CC6POS0: [CAPCOM6] Position 0 Input, EX0IN: [Fast External Interrupt 0] Input (default pin),
P1H.1	2	I/O I	CC23IO: [CAPCOM2] CC23 Capture Inp./Compare Outp. CC6POS1: [CAPCOM6] Position 1 Input,
P1H.2	3	I I	EX1IN: [Fast External Interrupt 1] Input (default pin), MRST1: [SSC1] Master-Receive/Slave-Transmit In/Out.
P1H.3	3	I/O I	CC6POS2: [CAPCOM6] Position 2 Input, EX2IN: [Fast External Interrupt 2] Input (default pin), MTSR1: [SSC1] Master-Transmit/Slave-Receive Out/Inp.
P1H.4	5	I/O I	T7IN: [CAPCOM2] Timer T7 Count Input, SCLK1: [SSC1] Master Clock Output / Slave Clock Input, EX3IN: [Fast External Interrupt 3] Input (default pin),
P1H.5	6	I/O I	CC24IO: [CAPCOM2] CC24 Capture Inp./Compare Outp., EX4IN: [Fast External Interrupt 4] Input (default pin) CC25IO: [CAPCOM2] CC25 Capture Inp./Compare Outp., EX5IN: [Fast External Interrupt 5] Input (default pin)
			<i>Note: At the end of an external reset P1H.4 and P1H.5 also may input startup configuration values</i>

### **3.3 Interrupt System**

With an interrupt response time of typically 8 CPU clocks (in case of internal program execution), the XC164CM is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the XC164CM supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source, or the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The XC164CM has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bit field exists for each of the possible interrupt nodes. Via its related register, each node can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt nodes has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge, or both edges).

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

**Table 4** shows all of the possible XC164CM interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

*Note: Interrupt nodes which are not assigned to peripherals (unassigned nodes), may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).*



**Functional Description**
**Table 4 XC164CM Interrupt Nodes**

Source of Interrupt or PEC Service Request	Control Register	Vector Location <sup>1)</sup>	Trap Number
EX0IN	CC1_CC8IC	xx'0060 <sub>H</sub>	18 <sub>H</sub> / 24 <sub>D</sub>
EX1IN	CC1_CC9IC	xx'0064 <sub>H</sub>	19 <sub>H</sub> / 25 <sub>D</sub>
EX2IN	CC1_CC10IC	xx'0068 <sub>H</sub>	1A <sub>H</sub> / 26 <sub>D</sub>
EX3IN	CC1_CC11IC	xx'006C <sub>H</sub>	1B <sub>H</sub> / 27 <sub>D</sub>
EX4IN	CC1_CC12IC	xx'0070 <sub>H</sub>	1C <sub>H</sub> / 28 <sub>D</sub>
EX5IN	CC1_CC13IC	xx'0074 <sub>H</sub>	1D <sub>H</sub> / 29 <sub>D</sub>
CAPCOM Register 16	CC2_CC16IC	xx'00C0 <sub>H</sub>	30 <sub>H</sub> / 48 <sub>D</sub>
CAPCOM Register 17	CC2_CC17IC	xx'00C4 <sub>H</sub>	31 <sub>H</sub> / 49 <sub>D</sub>
CAPCOM Register 18	CC2_CC18IC	xx'00C8 <sub>H</sub>	32 <sub>H</sub> / 50 <sub>D</sub>
CAPCOM Register 19	CC2_CC19IC	xx'00CC <sub>H</sub>	33 <sub>H</sub> / 51 <sub>D</sub>
CAPCOM Register 20	CC2_CC20IC	xx'00D0 <sub>H</sub>	34 <sub>H</sub> / 52 <sub>D</sub>
CAPCOM Register 21	CC2_CC21IC	xx'00D4 <sub>H</sub>	35 <sub>H</sub> / 53 <sub>D</sub>
CAPCOM Register 22	CC2_CC22IC	xx'00D8 <sub>H</sub>	36 <sub>H</sub> / 54 <sub>D</sub>
CAPCOM Register 23	CC2_CC23IC	xx'00DC <sub>H</sub>	37 <sub>H</sub> / 55 <sub>D</sub>
CAPCOM Register 24	CC2_CC24IC	xx'00E0 <sub>H</sub>	38 <sub>H</sub> / 56 <sub>D</sub>
CAPCOM Register 25	CC2_CC25IC	xx'00E4 <sub>H</sub>	39 <sub>H</sub> / 57 <sub>D</sub>
CAPCOM Register 26	CC2_CC26IC	xx'00E8 <sub>H</sub>	3A <sub>H</sub> / 58 <sub>D</sub>
CAPCOM Register 27	CC2_CC27IC	xx'00EC <sub>H</sub>	3B <sub>H</sub> / 59 <sub>D</sub>
CAPCOM Register 28	CC2_CC28IC	xx'00F0 <sub>H</sub>	3C <sub>H</sub> / 60 <sub>D</sub>
CAPCOM Register 29	CC2_CC29IC	xx'0110 <sub>H</sub>	44 <sub>H</sub> / 68 <sub>D</sub>
CAPCOM Register 30	CC2_CC30IC	xx'0114 <sub>H</sub>	45 <sub>H</sub> / 69 <sub>D</sub>
CAPCOM Register 31	CC2_CC31IC	xx'0118 <sub>H</sub>	46 <sub>H</sub> / 70 <sub>D</sub>
CAPCOM Timer 7	CC2_T7IC	xx'00F4 <sub>H</sub>	3D <sub>H</sub> / 61 <sub>D</sub>
CAPCOM Timer 8	CC2_T8IC	xx'00F8 <sub>H</sub>	3E <sub>H</sub> / 62 <sub>D</sub>
GPT1 Timer 2	GPT12E_T2IC	xx'0088 <sub>H</sub>	22 <sub>H</sub> / 34 <sub>D</sub>
GPT1 Timer 3	GPT12E_T3IC	xx'008C <sub>H</sub>	23 <sub>H</sub> / 35 <sub>D</sub>
GPT1 Timer 4	GPT12E_T4IC	xx'0090 <sub>H</sub>	24 <sub>H</sub> / 36 <sub>D</sub>
GPT2 Timer 5	GPT12E_T5IC	xx'0094 <sub>H</sub>	25 <sub>H</sub> / 37 <sub>D</sub>
GPT2 Timer 6	GPT12E_T6IC	xx'0098 <sub>H</sub>	26 <sub>H</sub> / 38 <sub>D</sub>

---

**Functional Description**

register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

### **3.9 A/D Converter**

For analog signal measurement, a 10-bit A/D converter with 14 multiplexed input channels and a sample and hold circuit has been integrated on-chip. It uses the method of successive approximation. The sample time (for loading the capacitors) and the conversion time is programmable (in two modes) and can thus be adjusted to the external circuitry. The A/D converter can also operate in 8-bit conversion mode, where the conversion time is further reduced.

Overrun error detection/protection is provided for the conversion result register (ADDAT): either an interrupt request will be generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended in such a case until the previous result has been read.

For applications which require less analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converter of the XC164CM supports four different conversion modes. In the standard Single Channel conversion mode, the analog level on a specified channel is sampled once and converted to a digital result. In the Single Channel Continuous mode, the analog level on a specified channel is repeatedly sampled and converted without software intervention. In the Auto Scan mode, the analog levels on a prespecified number of channels are sequentially sampled and converted. In the Auto Scan Continuous mode, the prespecified channels are repeatedly sampled and converted. In addition, the conversion of a specific channel can be inserted (injected) into a running sequence without disturbing this sequence. This is called Channel Injection Mode.

The Peripheral Event Controller (PEC) may be used to automatically store the conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer.

After each reset and also during normal operation the ADC automatically performs calibration cycles. This automatic self-calibration constantly adjusts the converter to changing operating conditions (e.g. temperature) and compensates process variations.

These calibration cycles are part of the conversion cycle, so they do not affect the normal operation of the A/D converter.

In order to decouple analog inputs from digital noise and to avoid input trigger noise those pins used for analog input can be disconnected from the digital input stages under software control. This can be selected for each pin separately via register P5DIDIS (Port 5 Digital Input Disable).

The Auto-Power-Down feature of the A/D converter minimizes the power consumption when no conversion is in progress.

### **3.14 Watchdog Timer**

The Watchdog Timer represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after a reset of the chip, and can be disabled until the EINIT instruction has been executed (compatible mode), or it can be disabled and enabled at any time by executing instructions DISWDT and ENWDT (enhanced mode). Thus, the chip's start-up procedure is always monitored. The software has to be designed to restart the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and generates an internal hardware reset.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided by 2/4/128/256. The high byte of the Watchdog Timer register can be set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded and the low byte is cleared. Thus, time intervals between 13  $\mu$ s and 419 ms can be monitored (@ 40 MHz).

The default Watchdog Timer interval after reset is 3.28 ms (@ 40 MHz).

### 3.18 Instruction Set Summary

**Table 8** lists the instructions of the XC164CM in a condensed way.

The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the “**Instruction Set Manual**”.

This document also provides a detailed description of each instruction.

**Table 8 Instruction Set Summary**

<b>Mnemonic</b>	<b>Description</b>	<b>Bytes</b>
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- × 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2 / 4
BCLR/BSET	Clear/Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL/SHR	Shift left/right direct word GPR	2

**Functional Description**
**Table 8 Instruction Set Summary (cont'd)**

<b>Mnemonic</b>	<b>Description</b>	<b>Bytes</b>
ROL/ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2 / 4
MOVBS/Z	Move byte operand to word op. with sign/zero extension	2 / 4
JMPA/I/R	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
JB(C)	Jump relative if direct bit is set (and clear bit)	4
JNB(S)	Jump relative if direct bit is not set (and set bit)	4
CALLA/I/R	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH/POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET(P)	Return from intra-segment subroutine (and pop direct word register from system stack)	2
RETS	Return from inter-segment subroutine	2
RETI	Return from interrupt service subroutine	2
SBRK	Software Break	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Enter Power Down Mode (supposes $\overline{\text{NMI}}$ -pin being low)	4
SRVWDT	Service Watchdog Timer	4
DISWDT/ENWDT	Disable/Enable Watchdog Timer	4
EINIT	End-of-Initialization Register Lock	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2 / 4

**Electrical Parameters**
**Operating Conditions**

The following operating conditions must not be exceeded to ensure correct operation of the XC164CM. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

**Table 10 Operating Condition Parameters**

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Digital supply voltage for the core	$V_{DDI}$	2.35	2.7	V	Active mode, $f_{CPU} = f_{CPUmax}^{1)}$
Digital supply voltage for IO pads	$V_{DDP}$	4.4	5.5	V	Active mode <sup>2)3)</sup>
Supply Voltage Difference	$\Delta V_{DD}$	-0.5	–	V	$V_{DDP} - V_{DDI}^{4)}$
Digital ground voltage	$V_{SS}$	0		V	Reference voltage
Overload current	$I_{OV}$	-5	5	mA	Per IO pin <sup>5)6)</sup>
		-2	5	mA	Per analog input pin <sup>5)6)</sup>
Overload current coupling factor for analog inputs <sup>7)</sup>	$K_{OVA}$	–	$1.0 \times 10^{-4}$	–	$I_{OV} > 0$
		–	$1.5 \times 10^{-3}$	–	$I_{OV} < 0$
Overload current coupling factor for digital I/O pins <sup>7)</sup>	$K_{OVD}$	–	$5.0 \times 10^{-3}$	–	$I_{OV} > 0$
		–	$1.0 \times 10^{-2}$	–	$I_{OV} < 0$
Absolute sum of overload currents	$\Sigma  I_{OV} $	–	50	mA	<sup>6)</sup>
External Load Capacitance	$C_L$	–	50	pF	Pin drivers in <b>default</b> mode <sup>8)</sup>
Ambient temperature	$T_A$	0	70	°C	SAB-XC164...
		-40	85	°C	SAF-XC164...
		-40	125	°C	SAK-XC164...

1)  $f_{CPUmax} = 40$  MHz for devices marked ... 40F,  $f_{CPUmax} = 20$  MHz for devices marked ... 20F.

2) External circuitry must guarantee low-level at the  $\overline{RSTIN}$  pin at least until both power supply voltages have reached the operating range.

3) The specified voltage range is allowed for operation. The range limits may be reached under extreme operating conditions. However, specified parameters, such as leakage currents, refer to the standard operating voltage range of  $V_{DDP} = 4.75$  V to 5.25 V.

4) This limitation must be fulfilled under all operating conditions including power-ramp-up, power-ramp-down, and power-save modes.

## Electrical Parameters

- 5) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range:  $V_{OV} > V_{DDP} + 0.5 \text{ V}$  ( $I_{OV} > 0$ ) or  $V_{OV} < V_{SS} - 0.5 \text{ V}$  ( $I_{OV} < 0$ ). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltages must remain within the specified limits.  
Proper operation is not guaranteed if overload conditions occur on functional pins such as XTAL1.
- 6) Not subject to production test - verified by design/characterization.
- 7) An overload current ( $I_{OV}$ ) through a pin injects a certain error current ( $I_{INJ}$ ) into the adjacent pins. This error current adds to the respective pin's leakage current ( $I_{OZ}$ ). The amount of error current depends on the overload current and is defined by the overload coupling factor  $K_{OV}$ . The polarity of the injected error current is inverse compared to the polarity of the overload current that produces it.  
The total current through a pin is  $|I_{TOT}| = |I_{OZ}| + (|I_{OV}| \times K_{OV})$ . The additional error current may distort the input voltage on analog inputs.
- 8) The timing is valid for pin drivers operating in default current mode (selected after reset). Reducing the output current may lead to increased delays or reduced driving capability ( $C_L$ ).

## Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the XC164CM and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column "Symbol":

### **CC** (Controller **C**haracteristics):

The logic of the XC164CM will provide signals with the respective characteristics.

### **SR** (System **R**equirement):

The external system must provide signals with the respective characteristics to the XC164CM.



**Electrical Parameters**
**4.2 DC Parameters**

These parameters are static or average values, which may be exceeded during switching transitions (e.g. output current).

**Table 11 DC Characteristics (Operating Conditions apply)<sup>1)</sup>**

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Input low voltage TTL (all except XTAL1)	$V_{IL}$	SR	-0.5	$0.2 \times V_{DDP} - 0.1$	V	—
Input low voltage XTAL1 <sup>2)</sup>	$V_{ILC}$	SR	-0.5	$0.3 \times V_{DDI}$	V	—
Input low voltage (Special Threshold)	$V_{ILS}$	SR	-0.5	$0.45 \times V_{DDP}$	V	<sup>3)</sup>
Input high voltage TTL (all except XTAL1)	$V_{IH}$	SR	$0.2 \times V_{DDP} + 0.9$	$V_{DDP} + 0.5$	V	—
Input high voltage XTAL1 <sup>2)</sup>	$V_{IHC}$	SR	$0.7 \times V_{DDI}$	$V_{DDI} + 0.5$	V	—
Input high voltage (Special Threshold)	$V_{IHS}$	SR	$0.8 \times V_{DDP} - 0.2$	$V_{DDP} + 0.5$	V	<sup>3)</sup>
Input Hysteresis (Special Threshold)	HYS		$0.04 \times V_{DDP}$	—	V	$V_{DDP}$ in [V], Series resistance = $0 \Omega$ <sup>3)</sup>
Output low voltage	$V_{OL}$	CC	—	1.0	V	$I_{OL} \leq I_{OLmax}$ <sup>4)</sup>
			—	0.45	V	$I_{OL} \leq I_{OLnom}$ <sup>4)5)</sup>
Output high voltage <sup>6)</sup>	$V_{OH}$	CC	$V_{DDP} - 1.0$	—	V	$I_{OH} \geq I_{OHmax}$ <sup>4)</sup>
			$V_{DDP} - 0.45$	—	V	$I_{OH} \geq I_{OHnom}$ <sup>4)5)</sup>
Input leakage current (Port 5) <sup>7)</sup>	$I_{OZ1}$	CC	—	$\pm 300$	nA	$0 V < V_{IN} < V_{DDP}$ , $T_A \leq 125^\circ C$
				$\pm 200$	nA	$0 V < V_{IN} < V_{DDP}$ , $T_A \leq 85^\circ C$ <sup>12)</sup>
Input leakage current (all other <sup>8)</sup> ) <sup>7)</sup>	$I_{OZ2}$	CC	—	$\pm 500$	nA	$0.45 V < V_{IN} < V_{DDP}$
Configuration pull-up current <sup>9)</sup>	$I_{CPUH}$ <sup>10)</sup>		—	-10	$\mu A$	$V_{IN} = V_{IHmin}$
	$I_{CPUL}$ <sup>11)</sup>		-100	—	$\mu A$	$V_{IN} = V_{ILmax}$

**Electrical Parameters**
**Table 11 DC Characteristics (Operating Conditions apply)<sup>1)</sup> (cont'd)**

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
XTAL1 input current	$I_{IL}$	CC	–	±20	μA	$0\text{ V} < V_{IN} < V_{DDI}$
Pin capacitance <sup>12)</sup> (digital inputs/outputs)	$C_{IO}$	CC	–	10	pF	–

- 1) Keeping signal levels within the limits specified in this table, ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current  $I_{OV}$ .
- 2) If XTAL1 is driven by a crystal, reaching an amplitude (peak to peak) of  $0.4 \times V_{DDI}$  is sufficient.
- 3) This parameter is tested for P3, P9.
- 4) The maximum deliverable output current of a port driver depends on the selected output driver mode, see [Table 12, Current Limits for Port Output Drivers](#). The limit for pin groups must be respected.
- 5) As a rule, with decreasing output current the output levels approach the respective supply level ( $V_{OL} \rightarrow V_{SS}$ ,  $V_{OH} \rightarrow V_{DDP}$ ). However, only the levels for nominal output currents are guaranteed.
- 6) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.
- 7) An additional error current ( $I_{INJ}$ ) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor  $K_{OV}$ .
- 8) The driver of P3.15 is designed for faster switching, because this pin can deliver the system clock (CLKOUT). The maximum leakage current for P3.15 is, therefore, increased to 1 μA.
- 9) During a hardware reset this specification is valid for configuration on P1H.4, P1H.5, P9.4 and P9.5. After a hardware reset this specification is valid for NMI.
- 10) The maximum current may be drawn while the respective signal line remains inactive.
- 11) The minimum current must be drawn to drive the respective signal line active.
- 12) Not subject to production test - verified by design/characterization.

**Table 12 Current Limits for Port Output Drivers**

Port Output Driver Mode	Maximum Output Current ( $I_{OLmax}$ , $-I_{OHmax}$ ) <sup>1)</sup>	Nominal Output Current ( $I_{OLnom}$ , $-I_{OHnom}$ )
<b>Strong driver</b>	10 mA	2.5 mA
<b>Medium driver</b>	4.0 mA	1.0 mA
<b>Weak driver</b>	0.5 mA	0.1 mA

- 1) An output current above  $|I_{OXnom}|$  may be drawn from up to three pins at the same time. For any group of 16 neighboring port output pins the total output current in each direction ( $\Sigma I_{OL}$  and  $\Sigma -I_{OH}$ ) must remain below 50 mA.

## Electrical Parameters

The used mechanism to generate the master clock is selected by register PLLCON.

CPU and EBC are clocked with the CPU clock signal  $f_{\text{CPU}}$ . The CPU clock can have the same frequency as the master clock ( $f_{\text{CPU}} = f_{\text{MC}}$ ) or can be the master clock divided by two:  $f_{\text{CPU}} = f_{\text{MC}} / 2$ . This factor is selected by bit CPSYS in register SYSCON1.

The specification of the external timing (AC Characteristics) depends on the period of the CPU clock, called "TCP".

The other peripherals are supplied with the system clock signal  $f_{\text{SYS}}$  which has the same frequency as the CPU clock signal  $f_{\text{CPU}}$ .

### Bypass Operation

When bypass operation is configured (PLLCTRL = 0x<sub>B</sub>) the master clock is derived from the internal oscillator (input clock signal XTAL1) through the input- and output-prescalers:

$$f_{\text{MC}} = f_{\text{OSC}} / ((\text{PLLIDIV} + 1) \times (\text{PLLODIV} + 1)).$$

If both divider factors are selected as '1' (PLLIDIV = PLLODIV = '0') the frequency of  $f_{\text{MC}}$  directly follows the frequency of  $f_{\text{OSC}}$  so the high and low time of  $f_{\text{MC}}$  is defined by the duty cycle of the input clock  $f_{\text{OSC}}$ .

The lowest master clock frequency is achieved by selecting the maximum values for both divider factors:

$$f_{\text{MC}} = f_{\text{OSC}} / ((3 + 1) \times (14 + 1)) = f_{\text{OSC}} / 60.$$

### Phase Locked Loop (PLL)

When PLL operation is configured (PLLCTRL = 11<sub>B</sub>) the on-chip phase locked loop is enabled and provides the master clock. The PLL multiplies the input frequency by the factor **F** ( $f_{\text{MC}} = f_{\text{OSC}} \times \mathbf{F}$ ) which results from the input divider, the multiplication factor, and the output divider ( $\mathbf{F} = \text{PLLMUL} + 1 / (\text{PLLIDIV} + 1 \times \text{PLLODIV} + 1)$ ). The PLL circuit synchronizes the master clock to the input clock. This synchronization is done smoothly, i.e. the master clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of  $f_{\text{MC}}$  is constantly adjusted so it is locked to  $f_{\text{OSC}}$ . The slight variation causes a jitter of  $f_{\text{MC}}$  which also affects the duration of individual TCMs.

The timing listed in the AC Characteristics refers to TCPs. Because  $f_{\text{CPU}}$  is derived from  $f_{\text{MC}}$ , the timing must be calculated using the minimum TCP possible under the respective circumstances.

The actual minimum value for TCP depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so it corresponds to the applied input frequency (crystal or oscillator) the relative deviation for periods of more than one TCP is lower than for one single TCP (see formula and [Figure 16](#)).

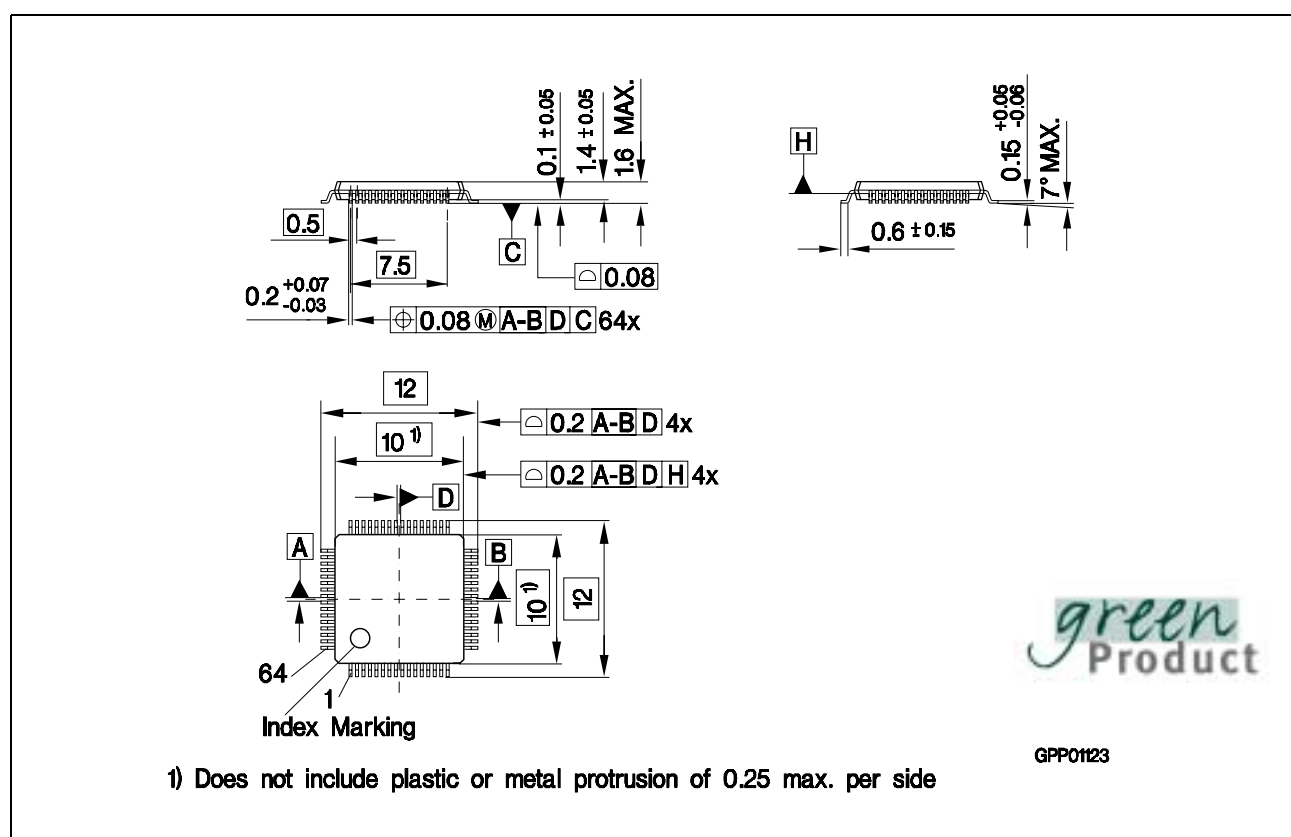
## 5 Package and Reliability

In addition to the electrical parameters, the following information ensures proper integration of the XC164CM into the target system.

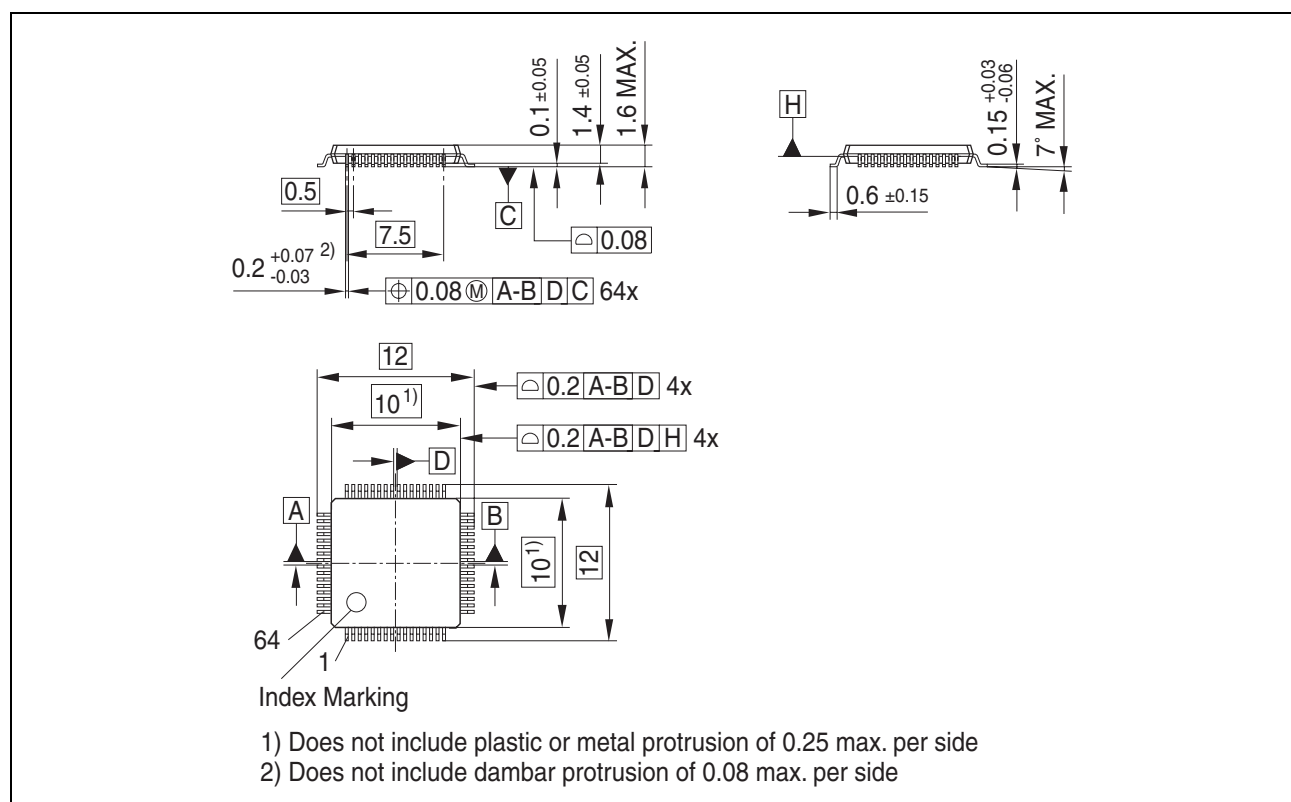
### 5.1 Packaging

These parameters describe the housing rather than the silicon.

#### Package Outlines



**Figure 18** PG-LQFP-64-4 (Plastic Green Low profile Quad Flat Package), valid for the -16F derivatives



**Figure 19** **PG-TQFP-64-8** (Plastic Thin Quad Flat Package), valid for the -4F/8F derivatives

You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": <http://www.infineon.com/products>

Dimensions in mm.

### Table 20 Package Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
PG-LQFP-64-4					
Thermal resistance junction to case	$R_{\Theta JC}$	—	8	K/W	—
Thermal resistance junction to leads	$R_{\Theta JL}$	—	23	K/W	—
PG-TQFP-64-8					
Thermal resistance junction to case	$R_{\Theta JC}$	—	9	K/W	—
Thermal resistance junction to leads	$R_{\Theta JL}$	—	19	K/W	—