



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Last Time Buy
Core Processor	C166SV2
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	47
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 14x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc164cm8f40faafxqma1

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Summary of Features

- Idle, Sleep, and Power Down Modes with Flexible Power Management
- Programmable Watchdog Timer and Oscillator Watchdog
- Up to 47 General Purpose I/O Lines, partly with Selectable Input Thresholds and Hysteresis
- On-Chip Bootstrap Loader
- On-Chip Debug Support via JTAG Interface
- 64-Pin Green LQFP Package for the -16F derivatives, 0.5 mm (19.7 mil) pitch (RoHS compliant)
- 64-Pin TQFP Package for the -4F/8F derivatives, 0.5 mm (19.7 mil) pitch (RoHS compliant)

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the XC164CM please refer to your responsible sales representative or your local distributor.

This document describes several derivatives of the XC164CM group. **Table 1** enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

For simplicity all versions are referred to by the term **XC164CM** throughout this document.



Summary of Features

Table 1 XC164CM Derivative Synopsis

Derivative ¹⁾	Temp. Range	Program Memory	On-Chip RAM	Interfaces
SAK-XC164CM-16F40F SAK-XC164CM-16F20F	-40 to 125 °C	128 Kbytes Flash	2 Kbytes DPRAM, 4 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1
SAF-XC164CM-16F40F SAF-XC164CM-16F20F	-40 to 85 °C	128 Kbytes Flash	2 Kbytes DPRAM, 4 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1
SAK-XC164CM-8F40F SAK-XC164CM-8F20F	-40 to 125 °C	64 Kbytes Flash	2 Kbytes DPRAM, 2 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1
SAF-XC164CM-8F40F SAF-XC164CM-8F20F	-40 to 85 °C	64 Kbytes Flash	2 Kbytes DPRAM, 2 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1
SAK-XC164CM-4F40F SAK-XC164CM-4F20F	-40 to 125 °C	32 Kbytes Flash	2 Kbytes DPRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1
SAF-XC164CM-4F40F SAF-XC164CM-4F20F	-40 to 85 °C	32 Kbytes Flash	2 Kbytes DPRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1

1) This Data Sheet is valid for:

devices starting with and including design step BA for the -16F derivatives, and for devices starting with and including design step AA for -4F/8F derivatives.



General Device Information

Table 2	Pin Definitions and Functions (cont'd)			
Sym-	Pin	Input	Function	
bol	Num.	Outp.		
Port 5	9-18, 21-24	I	Port 5 is a 14-bit input-only port. The pins of Port 5 also serve as analog input channels for the A/D converter, or they serve as timer inputs:	
P5.0	9		AN0	
P5.1	10		AN1	
P5.2	11		AN2	
P5.3	12		AN3	
P5.4	13		AN4	
P5.5 P5.10	14 15	 	AN5 AN10 (T6EUD): GPT2 Timer T6 Ext. Up/Down Ctrl. Inp.	
P5.11	16	1	AN11 (T5EUD): GPT2 Timer T5 Ext. Up/Down Ctrl. Inp.	
P5.6	17		AN6	
P5.7	18		AN7	
P5.12	21		AN12 (T6IN): GPT2 Timer T6 Count/Gate Input	
P5.13	22		AN13 (T5IN): GPT2 Timer T5 Count/Gate Input	
P5.14	23		AN14 (T4EUD): GPT1 Timer T4 Ext. Up/Down Ctrl. Inp.	
P5.15	24		AN15 (T2EUD): GPT1 Timer T2 Ext. Up/Down Ctrl. Inp.	
TRST	62	1	Test-System Reset Input. For normal system operation, pin TRST should be held low. A high level at this pin at the rising edge of RSTIN enables the hardware configuration and activates the XC164CM's debug system. In this case, pin TRST must be driven low once to reset the debug system.	



3 Functional Description

The architecture of the XC164CM combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a very well-balanced way. In addition, the on-chip memory blocks allow the design of compact systems-on-silicon with maximum performance (computing, control, communication).

The on-chip memory blocks (program code-memory and SRAM, dual-port RAM, data SRAM) and the set of generic peripherals are connected to the CPU via separate buses. Another bus, the LXBus, connects additional on-chip resources (see **Figure 3**).

This bus structure enhances the overall system performance by enabling the concurrent operation of several subsystems of the XC164CM.

The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the XC164CM.



Figure 3 Block Diagram



- 2) Not defined register locations return a trap code ($1E9B_H$).
- 3) Depends on the respective derivative. See Table 1 "XC164CM Derivative Synopsis" on Page 6.



example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. Also multiplication and most MAC instructions execute in one single cycle. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: for example, a 32-/16-bit division is started within 4 cycles, while the remaining 15 cycles are executed in the background. Another pipeline optimization, the branch target prediction, allows eliminating the execution time of branch instructions if the prediction was correct.

The CPU has a register context consisting of up to three register banks with 16 word wide GPRs each at its disposal. One of these register banks is physically allocated within the on-chip DPRAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at any time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 32 Kwords is provided as a storage for temporary data. The system stack can be allocated to any location within the address space (preferably in the on-chip RAM area), and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient XC164CM instruction set which includes the following instruction classes:

- Standard Arithmetic Instructions
- DSP-Oriented Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.



3.3 Interrupt System

With an interrupt response time of typically 8 CPU clocks (in case of internal program execution), the XC164CM is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the XC164CM supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source, or the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The XC164CM has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bit field exists for each of the possible interrupt nodes. Via its related register, each node can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt nodes has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge, or both edges).

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

Table 4 shows all of the possible XC164CM interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not assigned to peripherals (unassigned nodes), may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).



Table 4XC164CM Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location ¹⁾	Trap Number
GPT2 CAPREL Register	GPT12E_CRIC	xx'009C _H	27 _H / 39 _D
A/D Conversion Complete	ADC_CIC	xx'00A0 _H	28 _H / 40 _D
A/D Overrun Error	ADC_EIC	xx'00A4 _H	29 _H / 41 _D
ASC0 Transmit	ASC0_TIC	xx'00A8 _H	2A _H / 42 _D
ASC0 Transmit Buffer	ASC0_TBIC	xx'011C _H	47 _H / 71 _D
ASC0 Receive	ASC0_RIC	xx'00AC _H	2B _H / 43 _D
ASC0 Error	ASC0_EIC	xx'00B0 _H	2C _H / 44 _D
ASC0 Autobaud	ASC0_ABIC	xx'017C _H	5F _H / 95 _D
SSC0 Transmit	SSC0_TIC	xx'00B4 _H	2D _H / 45 _D
SSC0 Receive	SSC0_RIC	xx'00B8 _H	2E _H / 46 _D
SSC0 Error	SSC0_EIC	xx'00BC _H	2F _H / 47 _D
PLL/OWD	PLLIC	xx'010C _H	43 _H / 67 _D
ASC1 Transmit	ASC1_TIC	xx'0120 _H	48 _H / 72 _D
ASC1 Transmit Buffer	ASC1_TBIC	xx'0178 _H	5E _H / 94 _D
ASC1 Receive	ASC1_RIC	xx'0124 _H	49 _H / 73 _D
ASC1 Error	ASC1_EIC	xx'0128 _H	4A _H / 74 _D
ASC1 Autobaud	ASC1_ABIC	xx'0108 _H	42 _H / 66 _D
End of PEC Subchannel	EOPIC	xx'0130 _H	4C _H / 76 _D
CAPCOM6 Timer T12	CCU6_T12IC	xx'0134 _H	4D _H / 77 _D
CAPCOM6 Timer T13	CCU6_T13IC	xx'0138 _H	4E _H / 78 _D
CAPCOM6 Emergency	CCU6_EIC	xx'013C _H	4F _H / 79 _D
CAPCOM6	CCU6_IC	xx'0140 _H	50 _H / 80 _D
SSC1 Transmit	SSC1_TIC	xx'0144 _H	51 _H / 81 _D
SSC1 Receive	SSC1_RIC	xx'0148 _H	52 _H / 82 _D
SSC1 Error	SSC1_EIC	xx'014C _H	53 _H / 83 _D
CAN0	CAN_0IC	xx'0150 _H	54 _H / 84 _D
CAN1	CAN_1IC	xx'0154 _H	55 _H / 85 _D
CAN2	CAN_2IC	xx'0158 _H	56 _H / 86 _D
CAN3	CAN_3IC	xx'015C _H	57 _H / 87 _D
CAN4	CAN_4IC	xx'0164 _H	59 _H / 89 _D



3.5 Capture/Compare Unit (CAPCOM2)

The CAPCOM unit supports generation and control of timing sequences on up to 16 channels with a maximum resolution of 1 system clock cycle (8 cycles in staggered mode). The CAPCOM unit is typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PWM), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Two 16-bit timers (T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustments to the application specific requirements. In addition, an external count input for CAPCOM timer T7 allows event scheduling for the capture/compare registers relative to external events.

The capture/compare register array contains 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer (T7 or T8, respectively), and programmed for capture or compare function.

10 registers of the CAPCOM2 module have each one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

Compare Modes	Function
Mode 0	Interrupt-only compare mode; Several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; Several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; Only one compare interrupt per timer period is generated
Mode 3	Pin set '1' on match; pin reset '0' on compare timer overflow; Only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; Pin toggles on each compare match; Several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; Can be used with any compare mode

Table 6	Compare	Modes	(CAPCOM2)
			(······/

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched ('captured') into the capture/compare









3.10 Asynchronous/Synchronous Serial Interfaces (ASC0/ASC1)

The Asynchronous/Synchronous Serial Interfaces ASC0/ASC1 (USARTs) provide serial communication with other microcontrollers, processors, terminals or external peripheral components. They are upward compatible with the serial ports of the Infineon 8-bit microcontroller families and support full-duplex asynchronous communication and half-duplex synchronous communication. A dedicated baudrate generator with a fractional divider precisely generates all standard baud rates without oscillator tuning. For transmission, reception, error handling, and baud rate detection 5 separate interrupt vectors are provided.

In asynchronous mode, 8- or 9-bit data frames (with optional parity bit) are transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data plus wake-up bit mode). IrDA data transmissions up to 115.2 kbit/s with fixed or programmable IrDA pulse width are supported.

In synchronous mode, bytes (8 bits) are transmitted or received synchronously to a shift clock which is generated by the ASC0/1. The LSB is always shifted first.

In both modes, transmission and reception of data is FIFO-buffered. An autobaud detection unit allows to detect asynchronous data frames with its baudrate and mode with automatic initialization of the baudrate generator and the mode control bits.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. A parity bit can automatically be generated on transmission or be checked on reception. Framing error detection allows to recognize data frames with missing stop bits. An overrun error will be generated, if the last character received has not been read out of the receive buffer register at the time the reception of a new character is complete.

Summary of Features

- Full-duplex asynchronous operating modes
 - 8- or 9-bit data frames, LSB first, one or two stop bits, parity generation/checking
 - Baudrate from 2.5 Mbit/s to 0.6 bit/s (@ 40 MHz)
 - Multiprocessor mode for automatic address/data byte detection
 - Support for IrDA data transmission/reception up to max. 115.2 kbit/s (@ 40 MHz)
 - Auto baudrate detection
- Half-duplex 8-bit synchronous operating mode at 5 Mbit/s to 406.9 bit/s (@ 40 MHz)
- Buffered transmitter/receiver with FIFO support (8 entries per direction)
- Loop-back option available for testing purposes
- Interrupt generation on transmitter buffer empty condition, last bit transmitted condition, receive buffer full condition, error condition (frame, parity, overrun error), start and end of an autobaud detection



3.11 High Speed Synchronous Serial Channels (SSC0/SSC1)

The High Speed Synchronous Serial Channels SSC0/SSC1 support full-duplex and halfduplex synchronous communication. It may be configured so it interfaces with serially linked peripheral components, full SPI functionality is supported.

A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling three separate interrupt vectors are provided.

The SSC transmits or receives characters of 2 ... 16 bits length synchronously to a shift clock which can be generated by the SSC (master mode) or by an external master (slave mode). The SSC can start shifting with the LSB or with the MSB and allows the selection of shifting and latching clock edges as well as the clock polarity.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. Transmit error and receive error supervise the correct handling of the data buffer. Phase error and baudrate error detect incorrect serial data.

Summary of Features

- Master or Slave mode operation
- Full-duplex or Half-duplex transfers
- Baudrate generation from 20 Mbit/s to 305.18 bit/s (@ 40 MHz)
- Flexible data format
 - Programmable number of data bits: 2 to 16 bits
 - Programmable shift direction: LSB-first or MSB-first
 - Programmable clock polarity: idle low or idle high
 - Programmable clock/data phase: data shift with leading or trailing clock edge
- Loop back option available for testing purposes
- Interrupt generation on transmitter buffer empty condition, receive buffer full condition, error condition (receive, phase, baudrate, transmit error)
- Three pin interface with flexible SSC pin configuration



3.12 TwinCAN Module

The integrated TwinCAN module handles the completely autonomous transmission and reception of CAN frames in accordance with the CAN specification V2.0 part B (active), i.e. the on-chip TwinCAN module can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

Two Full-CAN nodes share the TwinCAN module's resources to optimize the CAN bus traffic handling and to minimize the CPU load. The module provides up to 32 message objects, which can be assigned to one of the CAN nodes and can be combined to FIFO-structures. Each object provides separate masks for acceptance filtering.

The flexible combination of Full-CAN functionality and FIFO architecture reduces the efforts to fulfill the real-time requirements of complex embedded control applications. Improved CAN bus monitoring functionality as well as the number of message objects permit precise and comfortable CAN bus traffic handling.

Gateway functionality allows automatic data exchange between two separate CAN bus systems, which reduces CPU load and improves the real time behavior of the entire system.

The bit timing for both CAN nodes is derived from the master clock and is programmable up to a data rate of 1 Mbit/s. Each CAN node uses two pins of Port 9 to interface to an external bus transceiver. The interface pins are assigned via software.



Figure 10 TwinCAN Module Block Diagram



3.16 Parallel Ports

The XC164CM provides up to 47 I/O lines which are organized into three input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of some I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

The edge characteristics (shape) and driver characteristics (output current) of the port drivers can be selected via registers POCONx.

The input threshold of some ports is selectable (TTL or CMOS like), where the special CMOS like input threshold reduces noise sensitivity due to the input hysteresis. The input threshold may be selected individually for each byte of the respective ports.

All port lines have programmable alternate input or output functions associated with them. All port lines that are not used for these alternate functions may be used as general purpose IO lines.

Port	Control	Alternate Functions
PORT1	Pad drivers	Capture inputs or compare outputs, Serial interface lines
Port 3	Pad drivers, Open drain, Input threshold	Timer control signals, serial interface lines, System clock output CLKOUT (or FOUT)
Port 5	-	Analog input channels to the A/D converter, Timer control signals
Port 9	Pad drivers, Open drain,	Capture inputs or compare outputs CAN interface lines ¹⁾
	Input threshold	

Table 7Summary of the XC164CM's Parallel Ports

1) Can be assigned by software.



Table 8 In	struction Set Summary (cont'd)	
Mnemonic	Description	Bytes
ROL/ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2/4
MOVBS/Z	Move byte operand to word op. with sign/zero extension	2/4
JMPA/I/R	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
JB(C)	Jump relative if direct bit is set (and clear bit)	4
JNB(S)	Jump relative if direct bit is not set (and set bit)	4
CALLA/I/R	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH/POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET(P)	Return from intra-segment subroutine (and pop direct word register from system stack)	2
RETS	Return from inter-segment subroutine	2
RETI	Return from interrupt service subroutine	2
SBRK	Software Break	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Enter Power Down Mode (supposes NMI-pin being low)	4
SRVWDT	Service Watchdog Timer	4
DISWDT/ENWD	T Disable/Enable Watchdog Timer	4
EINIT	End-of-Initialization Register Lock	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2/4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2/4



5) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: $V_{OV} > V_{DDP} + 0.5 \vee (I_{OV} > 0)$ or $V_{OV} < V_{SS} - 0.5 \vee (I_{OV} < 0)$. The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltages must remain within the specified limits.

Proper operation is not guaranteed if overload conditions occur on functional pins such as XTAL1.

- 6) Not subject to production test verified by design/characterization.
- 7) An overload current (I_{OV}) through a pin injects a certain error current (I_{INJ}) into the adjacent pins. This error current adds to the respective pin's leakage current (I_{OZ}) . The amount of error current depends on the overload current and is defined by the overload coupling factor K_{OV} . The polarity of the injected error current is inverse compared to the polarity of the overload current that produces it.

The total current through a pin is $|I_{TOT}| = |I_{OZ}| + (|I_{OV}| \times K_{OV})$. The additional error current may distort the input voltage on analog inputs.

8) The timing is valid for pin drivers operating in default current mode (selected after reset). Reducing the output current may lead to increased delays or reduced driving capability (C_L).

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the XC164CM and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column "Symbol":

CC (Controller Characteristics):

The logic of the XC164CM will provide signals with the respective characteristics.

SR (System Requirement):

The external system must provide signals with the respective characteristics to the XC164CM.



- V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be X000_H or X3FF_H, respectively.
- 3) The limit values for f_{BC} must not be exceeded when selecting the peripheral frequency and the ADCTC setting.
- 4) This parameter includes the sample time t_S, the time for determining the digital result and the time to load the result register with the conversion result (t_{SYS} = 1/f_{SYS}). Values for the basic clock t_{BC} depend on programming and can be taken from Table 15.

When the post-calibration is switched off, the conversion time is reduced by $12 \times t_{BC}$.

- 5) The actual duration of the reset calibration depends on the noise on the reference signal. Conversions executed during the reset calibration increase the calibration time. The TUE for those conversions may be increased.
- 6) Not subject to production test verified by design/characterization. The given parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) reduced values can be used for calculations. At room temperature and nominal supply voltage the following typical values can be used:

 C_{AINTtyp} = 12 pF, C_{AINStyp} = 7 pF, R_{AINtyp} = 1.5 kΩ, C_{AREFTtyp} = 15 pF, C_{AREFStyp} = 13 pF, R_{AREFtyp} = 0.7 kΩ.



Figure 14 Equivalent Circuitry for Analog Inputs



This is especially important for bus cycles using waitstates and e.g. for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler (K = PLLODIV+1) to generate the master clock signal f_{MC} . Therefore, the number of VCO cycles can be represented as K × N, where N is the number of consecutive f_{MC} cycles (TCM).

For a period of $\mathbf{N} \times \text{TCM}$ the accumulated PLL jitter is defined by the deviation D_N :

 D_N [ns] = ±(1.5 + 6.32 × N / f_{MC}); f_{MC} in [MHz], N = number of consecutive TCMs.

So, for a period of 3 TCMs @ 20 MHz and K = 12: $D_3 = \pm(1.5 + 6.32 \times 3 / 20) = 2.448$ ns. This formula is applicable for K × N < 95. For longer periods the K × N = 95 value can be

used. This steady value can be approximated by: D_{Nmax} [ns] = ±(1.5 + 600 / (K × f_{MC})).



Figure 16 Approximated Accumulated PLL Jitter

Note: The bold lines indicate the minimum accumulated jitter which can be achieved by selecting the maximum possible output prescaler factor K.



4.4.2 On-chip Flash Operation

The XC164CM's Flash module delivers data within a fixed access time (see Table 17).

Accesses to the Flash module are controlled by the PMI and take 1+WS clock cycles, where WS is the number of Flash access waitstates selected via bitfield WSFLASH in register IMBCTRL. The resulting duration of the access phase must cover the access time t_{ACC} of the Flash array. The required Flash waitstates depend on the actual system frequency.

The Flash access waitstates only affect non-sequential accesses. Due to prefetching mechanisms, the performance for sequential accesses (depending on the software structure) is only partially influenced by waitstates.

In typical applications, eliminating one waitstate increases the average performance by 5% ... 15%.

Parameter		ool	Limit Values			Unit
			Min.	Тур.	Max.	
Flash module access time	<i>t</i> _{ACC}	CC	-	-	50 ¹⁾	ns
Programming time per 128-byte block	t _{PR}	CC	_	2 ²⁾	5	ms
Erase time per sector	t _{ER}	CC	_	200 ²⁾	500	ms

Table 17 Flash Characteristics	(Operating Conditions apply)
--------------------------------	------------------------------

1) The actual access time is influenced by the system frequency, see Table 18.

2) Programming and erase time depends on the system frequency. Typical values are valid for 40 MHz.

Example: For an operating frequency of 40 MHz (clock cycle = 25 ns), the Flash accesses must be executed with 1 waitstate: $((1+1) \times 25 \text{ ns}) \ge 50 \text{ ns}$.

 Table 18 indicates the interrelation of waitstates and system frequency.

Table 18Flash Access Waitstates

Required Waitstates	Frequency Range
0 WS (WSFLASH = 00 _B)	$f_{\rm CPU} \le 20 \ { m MHz}$
1 WS (WSFLASH = 01 _B)	$f_{\rm CPU} \le 40 \ { m MHz}$

Note: The maximum achievable system frequency is limited by the properties of the respective derivative, i.e. 40 MHz (or 20 MHz for XC164CM-xF20F devices).



Package and Reliability

5 Package and Reliability

In addition to the electrical parameters, the following information ensures proper integration of the XC164CM into the target system.

5.1 Packaging

These parameters describe the housing rather than the silicon.

Package Outlines



Figure 18PG-LQFP-64-4 (Plastic Green Low profile Quad Flat Package),
valid for the -16F derivatives