Infeon Technologies - XC164CM8F40FAAFXUMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	C166SV2
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	47
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 14x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-TQFP-64-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc164cm8f40faafxuma1

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XC164CM
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Previous Version(s):
V1.3, 2006-08
V1.2, 2006-03
V1.1, 2005-11 (intermediate version)
V1.0, 2005-05

Page	Subjects (major changes since last revision)
6	Design steps of the derivatives differentiated.
53	Power consumption of the derivatives differentiated.
54	Figure 11 adapted.
55	Figure 13 adapted.
65	Packages of the derivatives differentiated.
66	Thermal resistances of the derivatives differentiated.
all	“Preliminary” removed

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2 General Device Information

The XC164CM derivatives are high-performance members of the Infineon XC166 Family of full featured single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 40 million instructions per second) with high peripheral functionality and enhanced IO-capabilities. They also provide clock generation via PLL and various on-chip memory modules such as program Flash, program RAM, and data RAM.

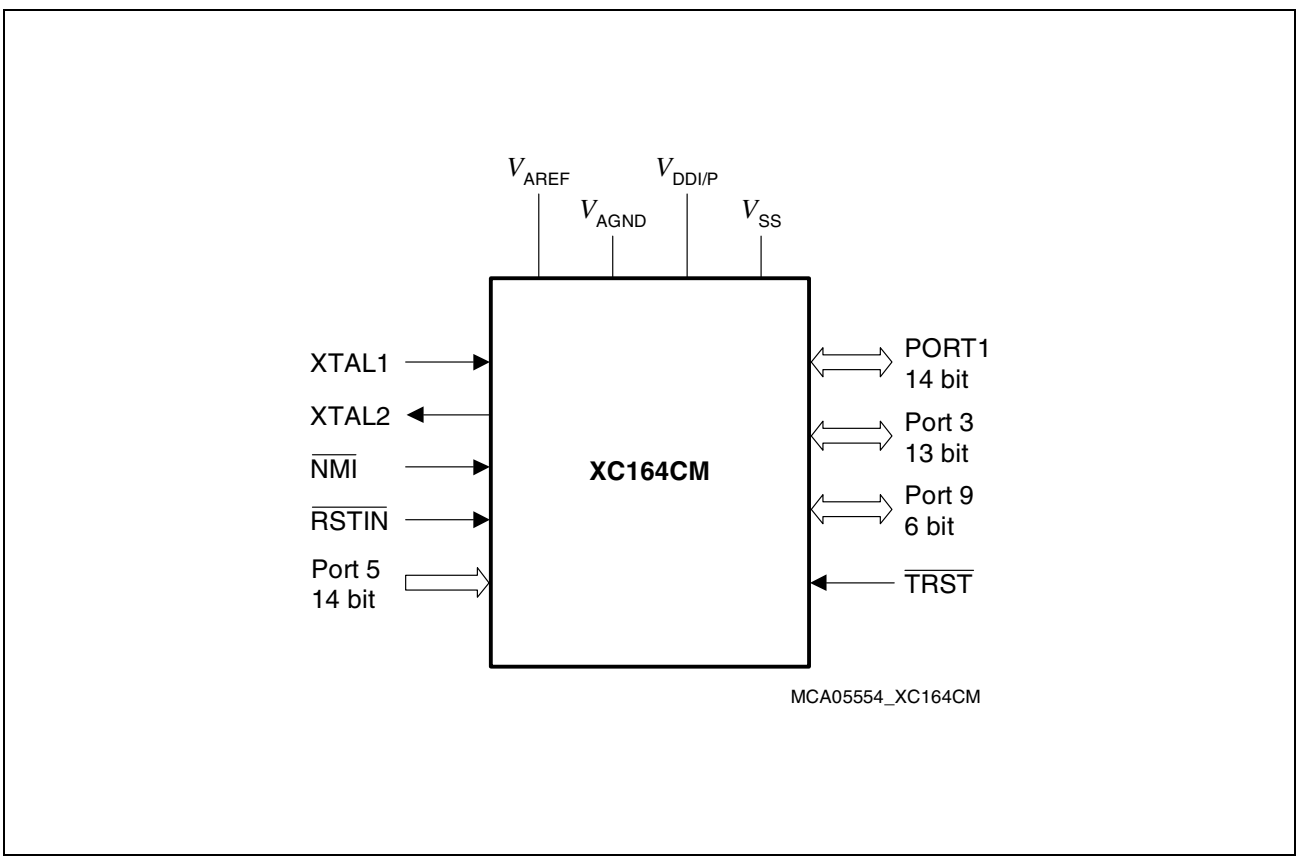

Figure 1 Logic Symbol

2.1 Pin Configuration and Definition

The pins of the XC164CM are described in detail in **Table 2**, including all their alternate functions. **Figure 2** summarizes all pins in a condensed way, showing their location on the 4 sides of the package. E* marks pins to be used as alternate external interrupt inputs.

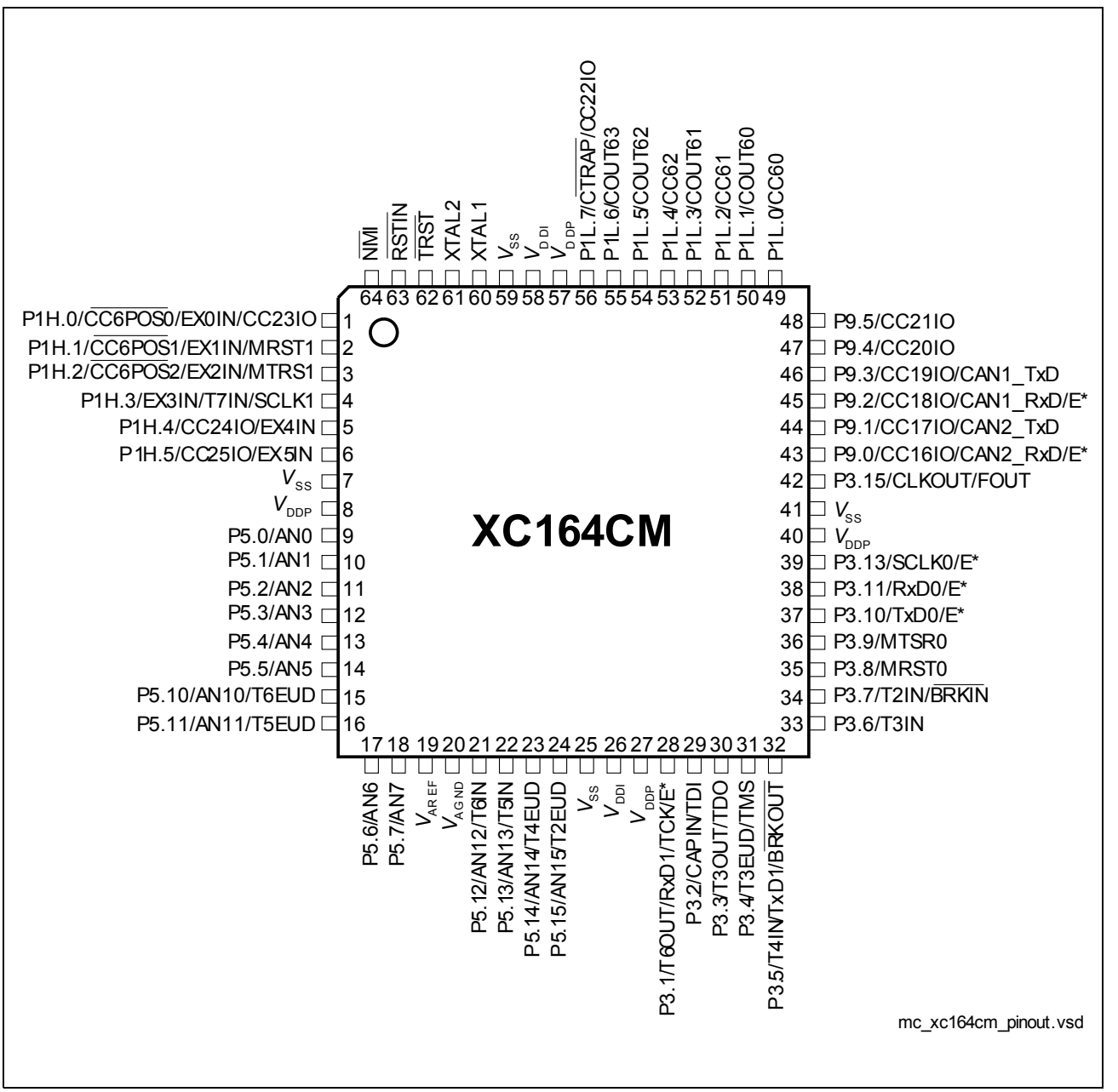

Figure 2 Pin Configuration (top view)

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
PORT1	1-6, 49-56	IO	PORT1 consists of one 8-bit and one 6-bit bidirectional I/O port P1L and P1H. Each pin can be programmed for input (output driver in high-impedance state) or output. The following PORT1 pins also serve for alt. functions:
P1L.0	49	I/O	CC60: [CAPCOM6] Input / Output of Channel 0
P1L.1	50	O	COUT60: [CAPCOM6] Output of Channel 0
P1L.2	51	I/O	CC61: [CAPCOM6] Input / Output of Channel 1
P1L.3	52	O	COUT61: [CAPCOM6] Output of Channel 1
P1L.4	53	I/O	CC62: [CAPCOM6] Input / Output of Channel 2
P1L.5	54	O	COUT62: [CAPCOM6] Output of Channel 2
P1L.6	55	O	COUT63: Output of 10-bit Compare Channel
P1L.7	56	I	CTRAP: [CAPCOM6] Trap Input CTRAP is an input pin with an internal pull-up resistor. A low level on this pin switches the CAPCOM6 compare outputs to the logic level defined by software (if enabled).
		I/O	CC22IO: [CAPCOM2] CC22 Capture Inp./Compare Outp.
P1H.0	1	I	CC6POS0: [CAPCOM6] Position 0 Input,
		I	EX0IN: [Fast External Interrupt 0] Input (default pin),
		I/O	CC23IO: [CAPCOM2] CC23 Capture Inp./Compare Outp.
P1H.1	2	I	CC6POS1: [CAPCOM6] Position 1 Input,
		I	EX1IN: [Fast External Interrupt 1] Input (default pin),
		I/O	MRST1: [SSC1] Master-Receive/Slave-Transmit In/Out.
P1H.2	3	I	CC6POS2: [CAPCOM6] Position 2 Input,
		I	EX2IN: [Fast External Interrupt 2] Input (default pin),
		I/O	MTSR1: [SSC1] Master-Transmit/Slave-Receive Out/Inp.
P1H.3	3	I	T7IN: [CAPCOM2] Timer T7 Count Input,
		I/O	SCLK1: [SSC1] Master Clock Output / Slave Clock Input,
		I	EX3IN: [Fast External Interrupt 3] Input (default pin),
P1H.4	5	I/O	CC24IO: [CAPCOM2] CC24 Capture Inp./Compare Outp.,
		I	EX4IN: [Fast External Interrupt 4] Input (default pin)
P1H.5	6	I/O	CC25IO: [CAPCOM2] CC25 Capture Inp./Compare Outp.,
		I	EX5IN: [Fast External Interrupt 5] Input (default pin)
			Note: At the end of an external reset P1H.4 and P1H.5 also may input startup configuration values

3.1 Memory Subsystem and Organization

The memory space of the XC164CM is configured in a von Neumann architecture, which means that all internal and external resources, such as code memory, data memory, registers and I/O ports, are organized within the same linear address space. This common memory space includes 16 Mbytes and is arranged as 256 segments of 64 Kbytes each, where each segment consists of four data pages of 16 Kbytes each. The entire memory space can be accessed byte wise or word wise. Portions of the on-chip DPRAM and the register spaces (E/SFR) have additionally been made directly bit addressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls accesses to the program memories, such as Flash memory and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls accesses to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected via the high-speed system bus to exchange data. This is required if operands are read from program memory, code or data is written to the PSRAM, or data is read from or written to peripherals on the LXBus (such as TwinCAN). The system bus allows concurrent two-way communication for maximum transfer performance.

32/64/128 Kbytes of on-chip Flash memory[1] store code or constant data. The on-chip Flash memory is organized as four 8-Kbyte sectors and up to three 32-Kbyte sectors. Each sector can be separately write protected[2], erased and programmed (in blocks of 128 Bytes). The complete Flash area can be read-protected. A password sequence temporarily unlocks protected areas. The Flash module combines very fast 64-bit one-cycle read accesses with protected and efficient writing algorithms for programming and erasing. Thus, program execution out of the internal Flash results in maximum performance. Dynamic error correction provides extremely high read data security for all read accesses.
Programming typically takes 2 ms per 128-byte block (5 ms max.), erasing a sector typically takes 200 ms (500 ms max.).

2 Kbytes of on-chip Program SRAM (PSRAM) are provided to store user code or data. The PSRAM is accessed via the PMU and is therefore optimized for code fetches.

0/2/4 Kbytes[1] of on-chip Data SRAM (DSRAM) are provided as a storage for general user data. The DSRAM is accessed via the DMU and is therefore optimized for data accesses. DSRAM is not available in the XC164CM-4F derivatives.

1) Depends on the respective derivative. See **Table 1 “XC164CM Derivative Synopsis” on Page 6**.

2) Each two 8-Kbyte sectors are combined for write-protection purposes.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) are provided as a storage for user defined variables, for the system stack, general purpose register banks. A register bank can consist of up to 16 word wide (R0 to R15) and/or byte wide (RL0, RH0, …, RL7, RH7) so-called General Purpose Registers (GPRs).
The upper 256 bytes of the DPRAM are directly bit addressable. When used by a GPR, any location in the DPRAM is bit addressable.

1024 bytes (2 × 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word wide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XC166 Family. Therefore, they should either not be accessed, or written with zeros, to ensure upward compatibility.

Table 3 XC164CM Memory Map

Address Area	Start Loc.	End Loc.	Area Size[1)]	Notes
Flash register space	$FF'F000_H$	$FF'FFFF_H$	4 Kbytes	[2)]
Reserved (Acc. trap)	$F8'0000_H$	$FF'FFFF_H$	508 Kbytes	–
Reserved for PSRAM	$E0'0800_H$	$F7'FFFF_H$	< 1.5 Mbytes	Minus PSRAM
Program SRAM	$E0'0000_H$	$E0'07FF_H$	2 Kbytes	–
Reserved for pr. mem.	$C2'0000_H$	$DF'FFFF_H$	< 2 Mbytes	Minus Flash
Program Flash	$C0'0000_H$	$C1'FFFF_H$	128 Kbytes	XC164CM-16F
	$C0'0000_H$	$C0'FFFF_H$	64 Kbytes	XC164CM-8F
	$C0'0000_H$	$C0'7FFF_H$	32 Kbytes	XC164CM-4F
Reserved	$20'0800_H$	$BF'FFFF_H$	< 10 Mbytes	Minus TwinCAN
TwinCAN registers	$20'0000_H$	$20'07FF_H$	2 Kbytes	Accessed via EBC
Reserved	$01'0000_H$	$1F'FFFF_H$	< 2 Mbytes	Minus segment 0
SFR area	$00'FE00_H$	$00'FFFF_H$	0.5 Kbyte	–
Dual-Port RAM	$00'F600_H$	$00'FDFF_H$	2 Kbytes	–
Reserved for DPRAM	$00'F200_H$	$00'F5FF_H$	1 Kbyte	–
ESFR area	$00'F000_H$	$00'F1FF_H$	0.5 Kbyte	–
XSFR area	$00'E000_H$	$00'EFFF_H$	4 Kbytes	–
Reserved	$00'D000_H$	$00'DFFF_H$	6 Kbytes	–
Data SRAM	$00'C000_H$	$00'CFFF_H$	4 Kbytes	[3)]
Reserved for DSRAM	$00'8000_H$	$00'BFFF_H$	16 Kbytes	–
Reserved	$00'0000_H$	$00'7FFF_H$	32 Kbytes	–

1) The areas marked with “<” are slightly smaller than indicated, see column “Notes”.

example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. Also multiplication and most MAC instructions execute in one single cycle. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: for example, a 32-/16-bit division is started within 4 cycles, while the remaining 15 cycles are executed in the background. Another pipeline optimization, the branch target prediction, allows eliminating the execution time of branch instructions if the prediction was correct.

The CPU has a register context consisting of up to three register banks with 16 word wide GPRs each at its disposal. One of these register banks is physically allocated within the on-chip DPRAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at any time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 32 Kwords is provided as a storage for temporary data. The system stack can be allocated to any location within the address space (preferably in the on-chip RAM area), and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient XC164CM instruction set which includes the following instruction classes:

- Standard Arithmetic Instructions
- DSP-Oriented Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

3.3 Interrupt System

With an interrupt response time of typically 8 CPU clocks (in case of internal program execution), the XC164CM is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the XC164CM supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source, or the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The XC164CM has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bit field exists for each of the possible interrupt nodes. Via its related register, each node can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt nodes has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge, or both edges).

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

Table 4 shows all of the possible XC164CM interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not assigned to peripherals (unassigned nodes), may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).

Table 4 XC164CM Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
GPT2 CAPREL Register	GPT12E_CRIC	xx'009C$_H$	27$_H$ / 39$_D$
A/D Conversion Complete	ADC_CIC	xx'00A0$_H$	28$_H$ / 40$_D$
A/D Overrun Error	ADC_EIC	xx'00A4$_H$	29$_H$ / 41$_D$
ASC0 Transmit	ASC0_TIC	xx'00A8$_H$	2A$_H$ / 42$_D$
ASC0 Transmit Buffer	ASC0_TBIC	xx'011C$_H$	47$_H$ / 71$_D$
ASC0 Receive	ASC0_RIC	xx'00AC$_H$	2B$_H$ / 43$_D$
ASC0 Error	ASC0_EIC	xx'00B0$_H$	2C$_H$ / 44$_D$
ASC0 Autobaud	ASC0_ABIC	xx'017C$_H$	5F$_H$ / 95$_D$
SSC0 Transmit	SSC0_TIC	xx'00B4$_H$	2D$_H$ / 45$_D$
SSC0 Receive	SSC0_RIC	xx'00B8$_H$	2E$_H$ / 46$_D$
SSC0 Error	SSC0_EIC	xx'00BC$_H$	2F$_H$ / 47$_D$
PLL/OWD	PLLIC	xx'010C$_H$	43$_H$ / 67$_D$
ASC1 Transmit	ASC1_TIC	xx'0120$_H$	48$_H$ / 72$_D$
ASC1 Transmit Buffer	ASC1_TBIC	xx'0178$_H$	5E$_H$ / 94$_D$
ASC1 Receive	ASC1_RIC	xx'0124$_H$	49$_H$ / 73$_D$
ASC1 Error	ASC1_EIC	xx'0128$_H$	4A$_H$ / 74$_D$
ASC1 Autobaud	ASC1_ABIC	xx'0108$_H$	42$_H$ / 66$_D$
End of PEC Subchannel	EOPIC	xx'0130$_H$	4C$_H$ / 76$_D$
CAPCOM6 Timer T12	CCU6_T12IC	xx'0134$_H$	4D$_H$ / 77$_D$
CAPCOM6 Timer T13	CCU6_T13IC	xx'0138$_H$	4E$_H$ / 78$_D$
CAPCOM6 Emergency	CCU6_EIC	xx'013C$_H$	4F$_H$ / 79$_D$
CAPCOM6	CCU6_IC	xx'0140$_H$	50$_H$ / 80$_D$
SSC1 Transmit	SSC1_TIC	xx'0144$_H$	51$_H$ / 81$_D$
SSC1 Receive	SSC1_RIC	xx'0148$_H$	52$_H$ / 82$_D$
SSC1 Error	SSC1_EIC	xx'014C$_H$	53$_H$ / 83$_D$
CAN0	CAN_0IC	xx'0150$_H$	54$_H$ / 84$_D$
CAN1	CAN_1IC	xx'0154$_H$	55$_H$ / 85$_D$
CAN2	CAN_2IC	xx'0158$_H$	56$_H$ / 86$_D$
CAN3	CAN_3IC	xx'015C$_H$	57$_H$ / 87$_D$
CAN4	CAN_4IC	xx'0164$_H$	59$_H$ / 89$_D$

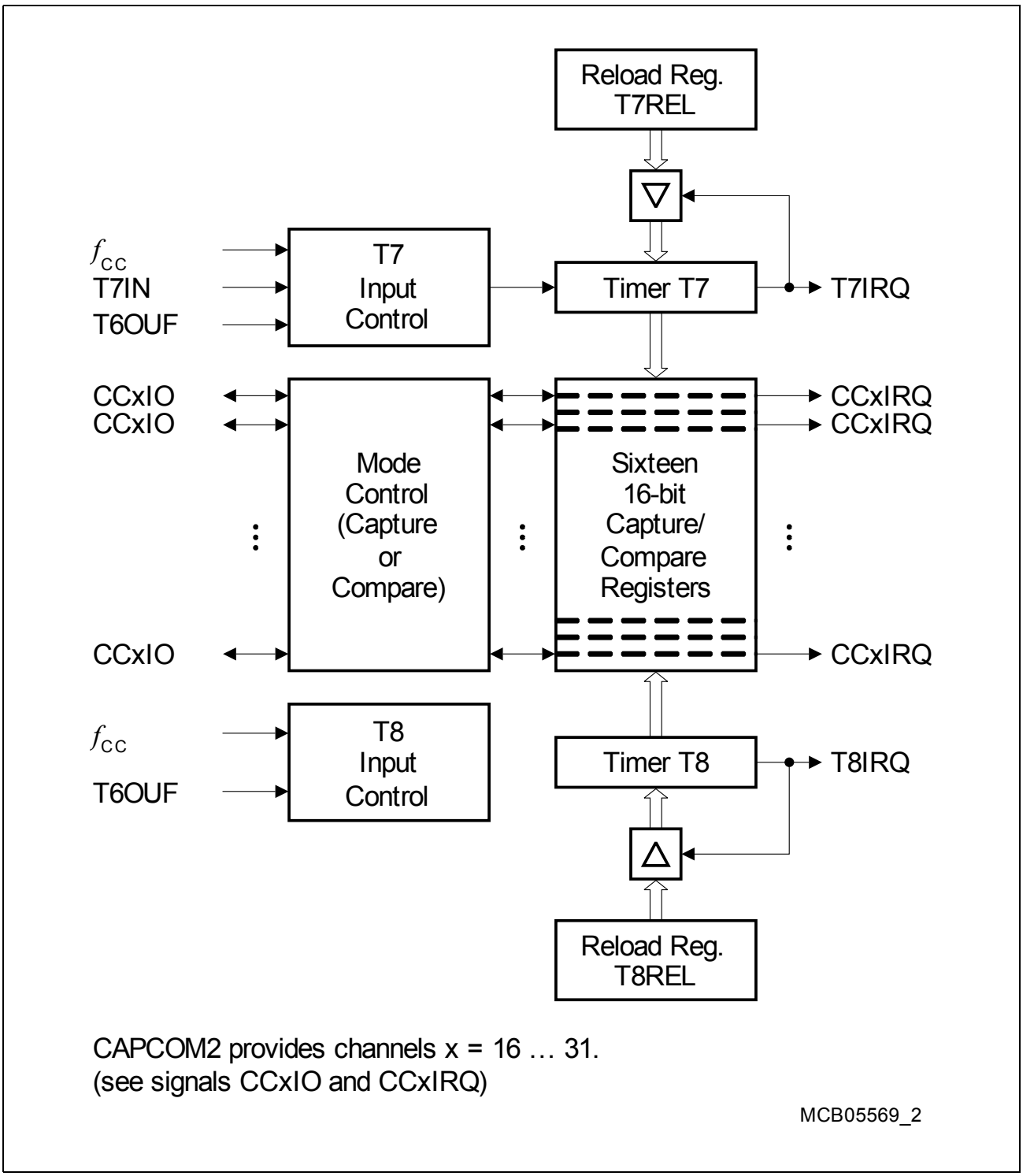

Figure 5 CAPCOM2 Unit Block Diagram

3.8 Real Time Clock

The Real Time Clock (RTC) module of the XC164CM is directly clocked via a separate clock driver with the prescaled on-chip main oscillator frequency ($f_{RTC} = f_{OSCm}/32$). It is therefore independent from the selected clock generation mode of the XC164CM.

The RTC basically consists of a chain of divider blocks:

- A selectable 8:1 divider (on - off)
- The reloadable 16-bit timer T14
- The 32-bit RTC timer block (accessible via registers RTCH and RTCL), made of:
  - a reloadable 10-bit timer
  - a reloadable 6-bit timer
  - a reloadable 6-bit timer
  - a reloadable 10-bit timer

All timers count up. Each timer can generate an interrupt request. All requests are combined to a common node request.

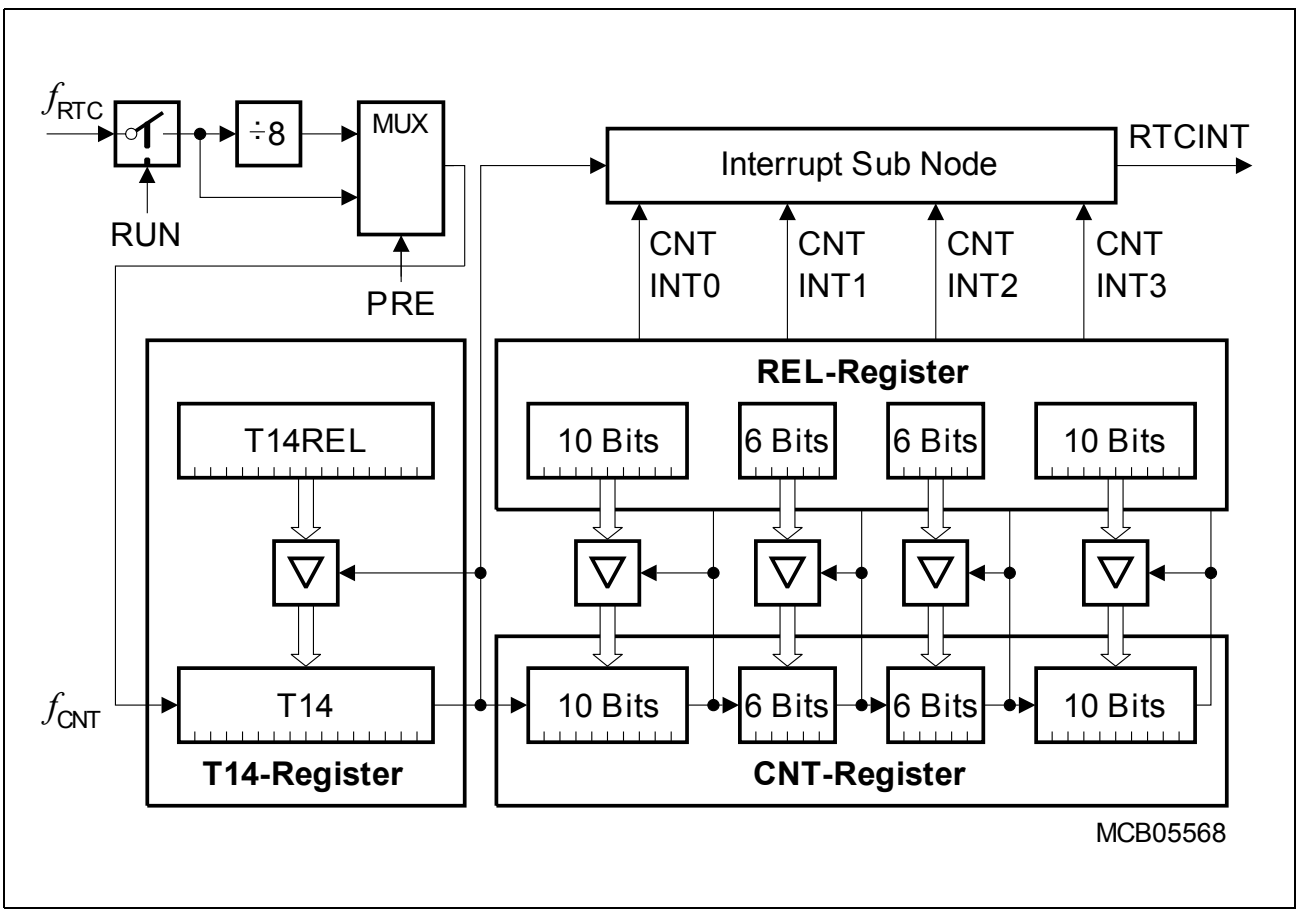

Figure 9 RTC Block Diagram

Note: The registers associated with the RTC are not affected by a reset in order to maintain the correct system time even when intermediate resets are executed.

3.12 TwinCAN Module

The integrated TwinCAN module handles the completely autonomous transmission and reception of CAN frames in accordance with the CAN specification V2.0 part B (active), i.e. the on-chip TwinCAN module can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

Two Full-CAN nodes share the TwinCAN module's resources to optimize the CAN bus traffic handling and to minimize the CPU load. The module provides up to 32 message objects, which can be assigned to one of the CAN nodes and can be combined to FIFO-structures. Each object provides separate masks for acceptance filtering.

The flexible combination of Full-CAN functionality and FIFO architecture reduces the efforts to fulfill the real-time requirements of complex embedded control applications. Improved CAN bus monitoring functionality as well as the number of message objects permit precise and comfortable CAN bus traffic handling.

Gateway functionality allows automatic data exchange between two separate CAN bus systems, which reduces CPU load and improves the real time behavior of the entire system.

The bit timing for both CAN nodes is derived from the master clock and is programmable up to a data rate of 1 Mbit/s. Each CAN node uses two pins of Port 9 to interface to an external bus transceiver. The interface pins are assigned via software.

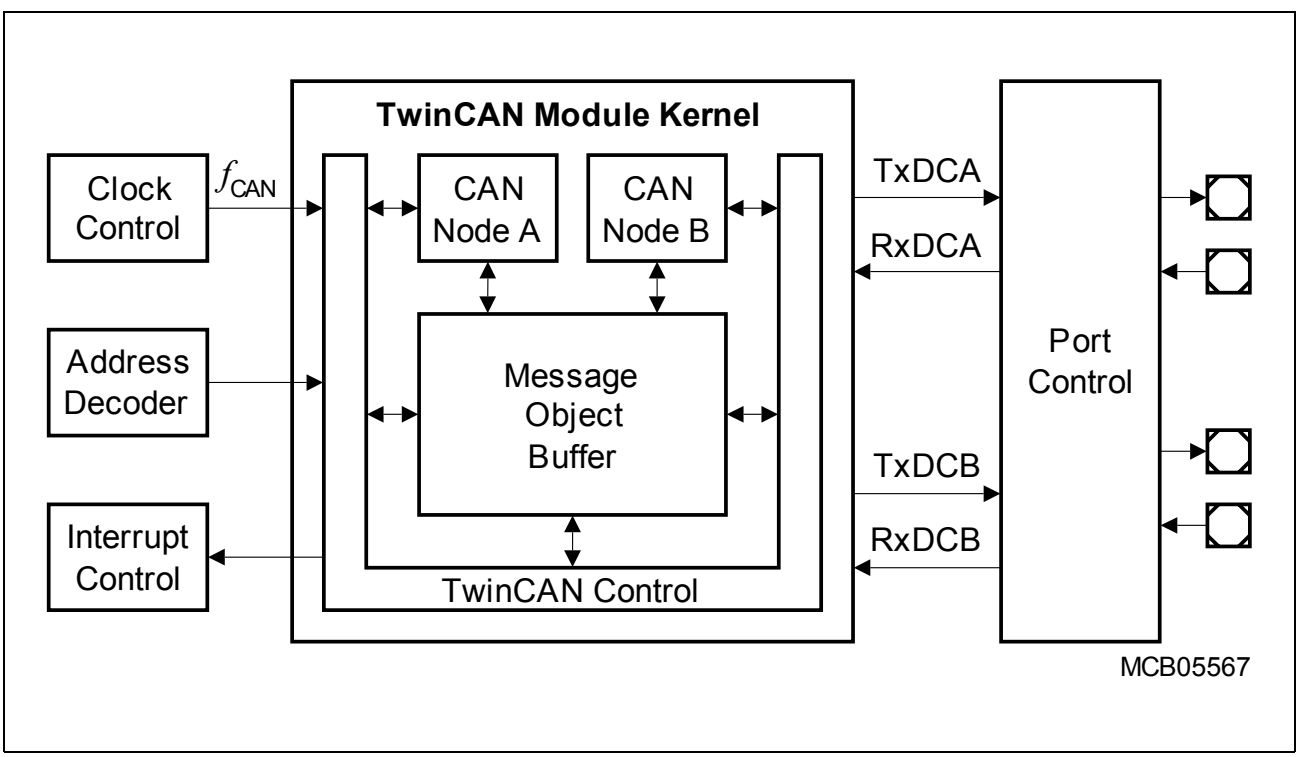

Figure 10 TwinCAN Module Block Diagram

Summary of Features

- CAN functionality according to CAN specification V2.0 B active
- Data transfer rate up to 1 Mbit/s
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality and Basic CAN functionality for each message object
- 32 flexible message objects
  - Assignment to one of the two CAN nodes
  - Configuration as transmit object or receive object
  - Concatenation to a 2-, 4-, 8-, 16-, or 32-message buffer with FIFO algorithm
  - Handling of frames with 11-bit or 29-bit identifiers
  - Individual programmable acceptance mask register for filtering for each object
  - Monitoring via a frame counter
  - Configuration for Remote Monitoring Mode
- Up to eight individually programmable interrupt nodes can be used
- CAN Analyzer Mode for bus monitoring is implemented

3.13 LXBus Controller (EBC)

The EBC only controls accesses to resources connected to the on-chip LXBus. The LXBus is an internal representation of the external bus and allows accessing integrated peripherals and modules in the same way as external components.

The TwinCAN module is connected and accessed via the LXBus.

4 Electrical Parameters

The operating range for the XC164CM is defined by its electrical parameters. For proper operation the indicated limitations must be respected when designing a system.

4.1 General Parameters

These parameters are valid for all subsequent descriptions, unless otherwise noted.

Table 9 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Storage temperature	T_{ST}	-65	150	°C	1)
Junction temperature	T_J	-40	150	°C	Under bias
Voltage on V_{DDI} pins with respect to ground (V_{SS})	V_{DDI}	-0.5	3.25	V	–
Voltage on V_{DDP} pins with respect to ground (V_{SS})	V_{DDP}	-0.5	6.2	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	V_{DDP} + 0.5	V	2)
Input current on any pin during overload condition	–	-10	10	mA	–
Absolute sum of all input currents during overload condition	–	–	|100|	mA	–

1) Moisture Sensitivity Level (MSL) 3, conforming to Jedec J-STD-020C for 260 °C.

2) Input pin XTAL1 belongs to the core voltage domain. Therefore, input voltages must be within the range defined for VDDI.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XC164CM. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 10 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Digital supply voltage for the core	V_{DDI}	2.35	2.7	V	Active mode, $f_{CPU} = f_{CPUmax}$ 1)
Digital supply voltage for IO pads	V_{DDP}	4.4	5.5	V	Active mode 2)3)
Supply Voltage Difference	ΔV_{DD}	-0.5	–	V	V_{DDP} - V_{DDI} 4)
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	-5	5	mA	Per IO pin 5)6)
		-2	5	mA	Per analog input pin 5)6)
Overload current coupling factor for analog inputs 7)	K_{OVA}	–	1.0×10^{-4}	–	$I_{OV} > 0$
		–	1.5×10^{-3}	–	$I_{OV} < 0$
Overload current coupling factor for digital I/O pins 7)	K_{OVD}	–	5.0×10^{-3}	–	$I_{OV} > 0$
		–	1.0×10^{-2}	–	$I_{OV} < 0$
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	–	50	mA	6)
External Load Capacitance	C_L	–	50	pF	Pin drivers in **default** mode 8)
Ambient temperature	T_A	0	70	°C	SAB-XC164…
		-40	85	°C	SAF-XC164…
		-40	125	°C	SAK-XC164…

1) f_{CPUmax} = 40 MHz for devices marked … 40F, f_{CPUmax} = 20 MHz for devices marked … 20F.

2) External circuitry must guarantee low-level at the $\overline{\text{RSTIN}}$ pin at least until both power supply voltages have reached the operating range.

3) The specified voltage range is allowed for operation. The range limits may be reached under extreme operating conditions. However, specified parameters, such as leakage currents, refer to the standard operating voltage range of V_{DDP} = 4.75 V to 5.25 V.

4) This limitation must be fulfilled under all operating conditions including power-ramp-up, power-ramp-down, and power-save modes.

5) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: $V_{OV} > V_{DDP} + 0.5$ V ($I_{OV} > 0$) or $V_{OV} < V_{SS} - 0.5$ V ($I_{OV} < 0$). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltages must remain within the specified limits.
   Proper operation is not guaranteed if overload conditions occur on functional pins such as XTAL1.
6) Not subject to production test - verified by design/characterization.
7) An overload current (I_{OV}) through a pin injects a certain error current (I_{INJ}) into the adjacent pins. This error current adds to the respective pin's leakage current (I_{OZ}). The amount of error current depends on the overload current and is defined by the overload coupling factor K_{OV}. The polarity of the injected error current is inverse compared to the polarity of the overload current that produces it.
   The total current through a pin is $|I_{TOT}| = |I_{OZ}| + (|I_{OV}| \times K_{OV})$. The additional error current may distort the input voltage on analog inputs.
8) The timing is valid for pin drivers operating in default current mode (selected after reset). Reducing the output current may lead to increased delays or reduced driving capability (C_L).

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the XC164CM and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the XC164CM will provide signals with the respective characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the respective characteristics to the XC164CM.

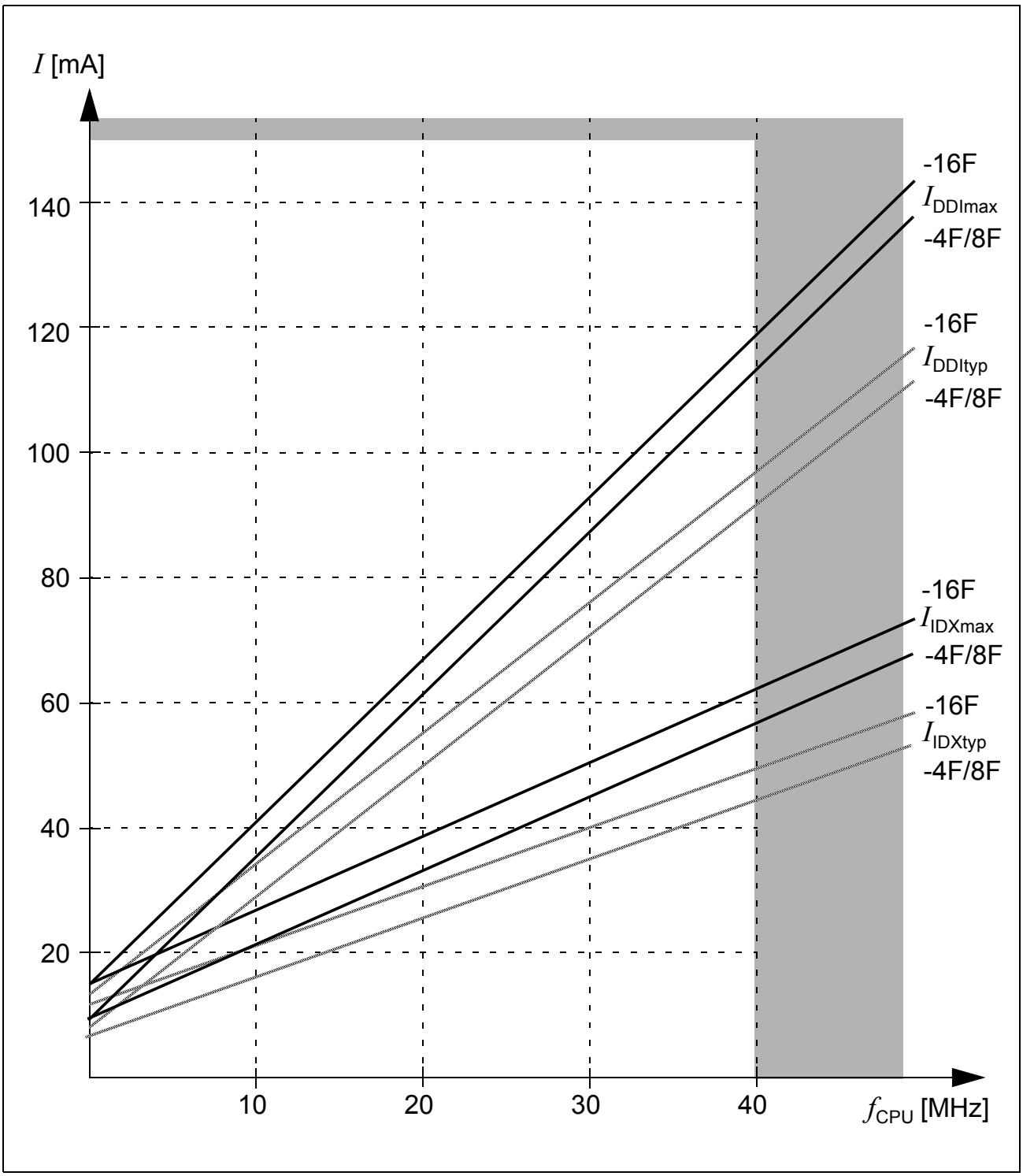

Figure 11 Supply/Idle Current as a Function of Operating Frequency

5 Package and Reliability

In addition to the electrical parameters, the following information ensures proper integration of the XC164CM into the target system.

5.1 Packaging

These parameters describe the housing rather than the silicon.

Package Outlines

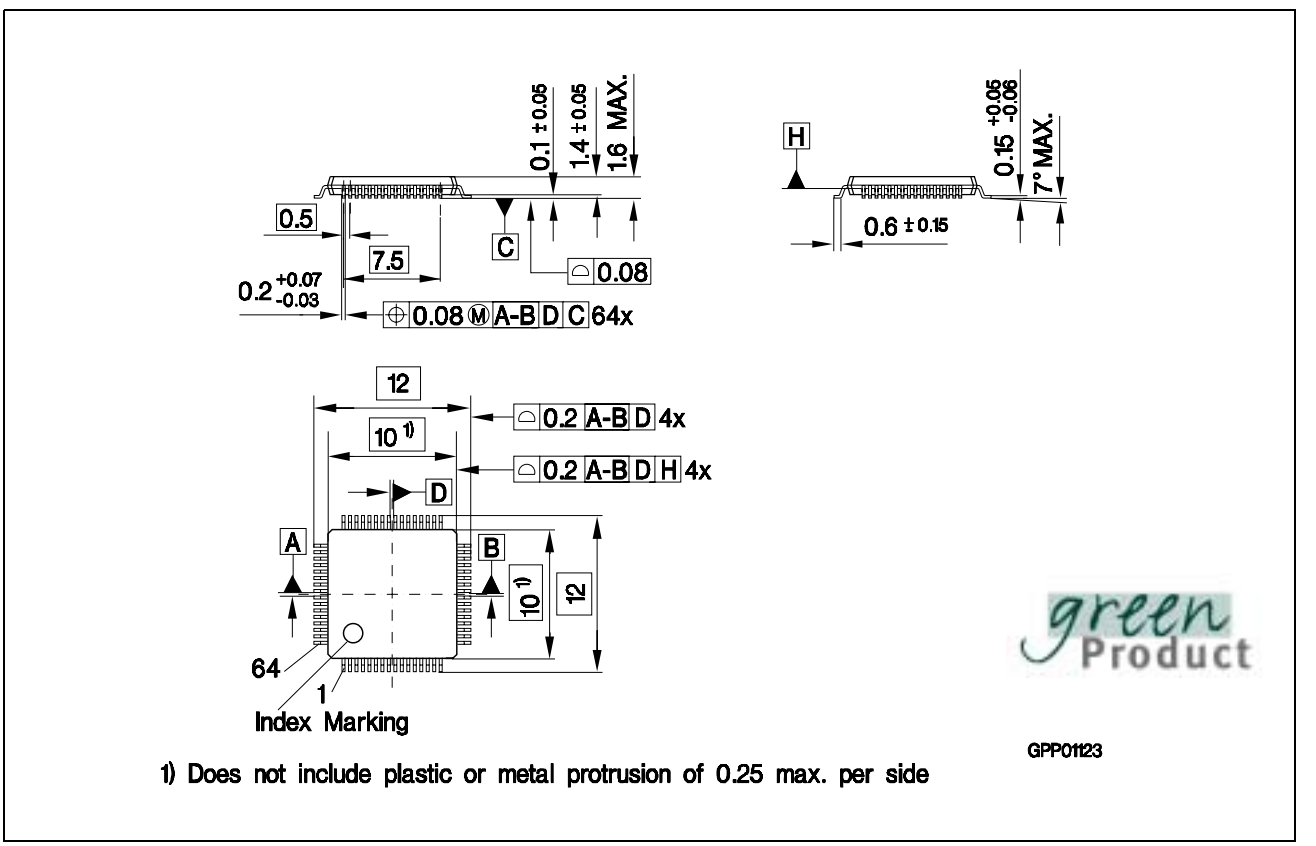

Figure 18 **PG-LQFP-64-4** (Plastic Green Low profile Quad Flat Package), valid for the -16F derivatives

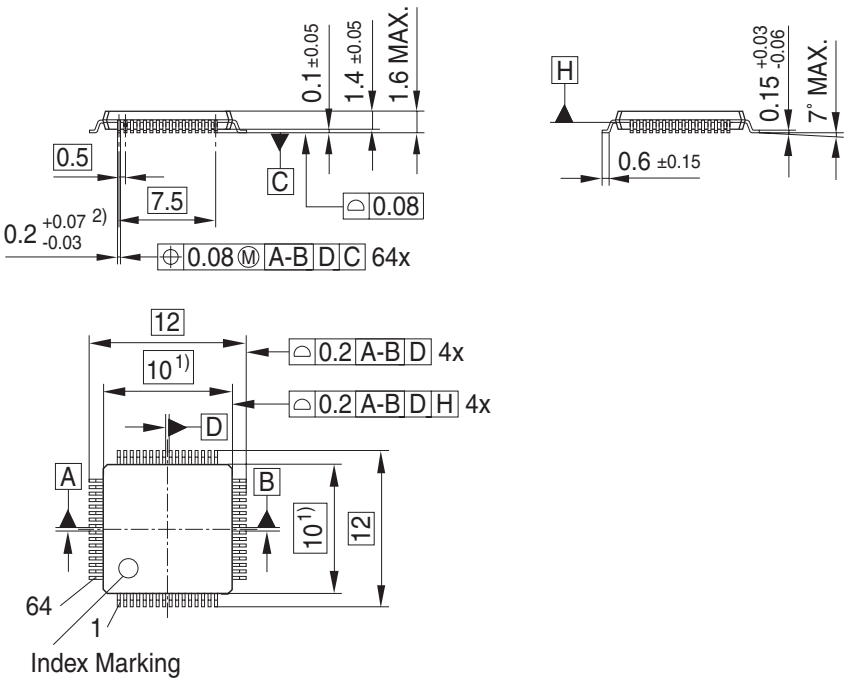

Figure 19 **PG-TQFP-64-8** (Plastic Thin Quad Flat Package), valid for the -4F/8F derivatives

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**

Dimensions in mm.

Table 20 Package Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
PG-LQFP-64-4					
Thermal resistance junction to case	$R_{\Theta JC}$	–	8	K/W	–
Thermal resistance junction to leads	$R_{\Theta JL}$	–	23	K/W	–
PG-TQFP-64-8					
Thermal resistance junction to case	$R_{\Theta JC}$	–	9	K/W	–
Thermal resistance junction to leads	$R_{\Theta JL}$	–	19	K/W	–