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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Last Time Buy
Core Processor	C166SV2
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	47
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6К х 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 14x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-TQFP-64
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc164cm8f40faakxuma1

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

XC164CM

16-Bit Single-Chip Microcontroller with C166SV2 Core

Microcontrollers



Never stop thinking



General Device Information

2.1 Pin Configuration and Definition

The pins of the XC164CM are described in detail in **Table 2**, including all their alternate functions. **Figure 2** summarizes all pins in a condensed way, showing their location on the 4 sides of the package. E* marks pins to be used as alternate external interrupt inputs.







General Device Information

Table 2	ble 2 Pin Definitions and Functions (cont'd)						
Sym- bol	Pin Num.	Input Outp.	Function				
Port 3	28-39,	10	Port 3 is a 13-bit bidirectional I/O port. Each pin can be				
	42		programmed for input (output driver in high-impedance state)				
			or output (configurable as push/pull or open drain driver). The				
			input threshold of Port 3 is selectable (standard or				
			special). The following Port 3 pins also serve for alternate				
			functions:				
P3.1	28	0	T6OUT: [GPT2] Timer T6 Toggle Latch Output,				
		I/O	RxD1: [ASC1] Data Input (Async.) or Inp./Outp. (Sync.),				
		1	EX1IN: [Fast External Interrupt 1] Input (alternate pin A),				
		1	TCK: [Debug System] JTAG Clock Input				
P3.2	29	1	CAPIN: [GPT2] Register CAPREL Capture Input,				
		1	TDI: [Debug System] JTAG Data In				
P3.3	30	0	T3OUT: [GPT1] Timer T3 Toggle Latch Output,				
		0	TDO: [Debug System] JTAG Data Out				
P3.4	31	1	T3EUD: [GPT1] Timer T3 External Up/Down Control Input,				
			TMS: [Debug System] JTAG Test Mode Selection				
P3.5	32		T4IN: [GPT1] Timer T4 Count/Gate/Reload/Capture Inp.				
		0	TxD1: [ASC0] Clock/Data Output (Async./Sync.),				
		0	BRKOUT: [Debug System] Break Out				
P3.6	33		T3IN: [GPT1] Timer T3 Count/Gate Input				
P3.7	34		T2IN: [GPT1] Timer T2 Count/Gate/Reload/Capture Inp.				
	0.5		BRKIN: [Debug System] Break In				
P3.8	35	1/0	MRS10: [SSC0] Master-Receive/Slave-Transmit In/Out.				
P3.9	36	1/0	MISRO: [SSC0] Master-Transmit/Slave-Receive Out/In.				
P3.10	37	0	TXD0: [ASC0] Clock/Data Output (Async./Sync.),				
	00		EX2IN: [Fast External Interrupt 2] Input (alternate pin B)				
P3.11	38	1/0	RXDU: [ASCU] Data Input (Async.) or Inp./Outp. (Sync.),				
D0 40	20		EX2IN: [Fast External Interrupt 2] Input (alternate pin A)				
P3.13	39	1/0	SCLKU: [SSCU] Master Clock Output / Slave Clock Input.,				
	40		EX3IN: [Fast External Interrupt 3] Input (alternate pin A)				
P3.15	42	0	CLKOUT: System Clock Output (= CPU Clock),				
		U	FOUT: Programmable Frequency Output				



General Device Information

Table 2	Pin Definitions and Functions (cont'd)					
Sym- bol	Pin Num.	Input Outp.	Function			
XTAL2 XTAL1	61 60	0 I	XTAL2: Output of the oscillator amplifier circuit XTAL1: Input to the oscillator amplifier and input to the internal clock generator To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.			
			Note: Input pin XTAL1 belongs to the core voltage domain. Therefore, input voltages must be within the range defined for $V_{\rm DDI}$.			
V_{AREF}	19	-	Reference voltage for the A/D converter			
V_{AGND}	20	-	Reference ground for the A/D converter			
V _{DDI}	26, 58	_	Digital Core Supply Voltage (On-Chip Modules): +2.5 V during normal operation and idle mode. Please refer to the Operating Condition Parameters			
V _{DDP}	8, 27, 40, 57	_	Digital Pad Supply Voltage (Pin Output Drivers): +5 V during normal operation and idle mode. Please refer to the Operating Condition Parameters			
V _{SS}	7, 25, 41, 59	_	Digital Ground Connect decoupling capacitors to adjacent $V_{\rm DD}/V_{\rm SS}$ pin pairs as close as possible to the pins. All $V_{\rm SS}$ pins must be connected to the ground-line or ground- plane.			

1) The CAN interface lines are assigned to port P9 under software control.



3.1 Memory Subsystem and Organization

The memory space of the XC164CM is configured in a von Neumann architecture, which means that all internal and external resources, such as code memory, data memory, registers and I/O ports, are organized within the same linear address space. This common memory space includes 16 Mbytes and is arranged as 256 segments of 64 Kbytes each, where each segment consists of four data pages of 16 Kbytes each. The entire memory space can be accessed byte wise or word wise. Portions of the on-chip DPRAM and the register spaces (E/SFR) have additionally been made directly bit addressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls accesses to the program memories, such as Flash memory and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls accesses to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected via the high-speed system bus to exchange data. This is required if operands are read from program memory, code or data is written to the PSRAM, or data is read from or written to peripherals on the LXBus (such as TwinCAN). The system bus allows concurrent two-way communication for maximum transfer performance.

32/64/128 Kbytes of on-chip Flash memory¹⁾ store code or constant data. The on-chip Flash memory is organized as four 8-Kbyte sectors and up to three 32-Kbyte sectors. Each sector can be separately write protected²⁾, erased and programmed (in blocks of 128 Bytes). The complete Flash area can be read-protected. A password sequence temporarily unlocks protected areas. The Flash module combines very fast 64-bit one-cycle read accesses with protected and efficient writing algorithms for programming and erasing. Thus, program execution out of the internal Flash results in maximum performance. Dynamic error correction provides extremely high read data security for all read accesses.

Programming typically takes 2 ms per 128-byte block (5 ms max.), erasing a sector typically takes 200 ms (500 ms max.).

2 Kbytes of on-chip Program SRAM (PSRAM) are provided to store user code or data. The PSRAM is accessed via the PMU and is therefore optimized for code fetches.

0/2/4 Kbytes¹⁾ of on-chip Data SRAM (DSRAM) are provided as a storage for general user data. The DSRAM is accessed via the DMU and is therefore optimized for data accesses. DSRAM is not available in the XC164CM-4F derivatives.

¹⁾ Depends on the respective derivative. See Table 1 "XC164CM Derivative Synopsis" on Page 6.

²⁾ Each two 8-Kbyte sectors are combined for write-protection purposes.



2 Kbytes of on-chip Dual-Port RAM (DPRAM) are provided as a storage for user defined variables, for the system stack, general purpose register banks. A register bank can consist of up to 16 word wide (R0 to R15) and/or byte wide (RL0, RH0, ..., RL7, RH7) so-called General Purpose Registers (GPRs).

The upper 256 bytes of the DPRAM are directly bit addressable. When used by a GPR, any location in the DPRAM is bit addressable.

1024 bytes (2 \times **512 bytes)** of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word wide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XC166 Family. Therefore, they should either not be accessed, or written with zeros, to ensure upward compatibility.

Address Area	Start Loc.	End Loc.	Area Size ¹⁾	Notes
Flash register space	FF'F000 _H	FF'FFFF _H	4 Kbytes	2)
Reserved (Acc. trap)	F8'0000 _H	FF'FFFF _H	508 Kbytes	-
Reserved for PSRAM	E0'0800 _H	F7'FFFF _H	< 1.5 Mbytes	Minus PSRAM
Program SRAM	E0'0000 _H	E0'07FF _H	2 Kbytes	-
Reserved for pr. mem.	C2'0000 _H	DF'FFFF _H	< 2 Mbytes	Minus Flash
Program Flash	C0'000 _H	C1'FFFF _H	128 Kbytes	XC164CM-16F
	C0'000 _H	C0'FFFF _H	64 Kbytes	XC164CM-8F
	C0'0000 _H	C0'7FFF _H	32 Kbytes	XC164CM-4F
Reserved	20'0800 _H	BF'FFFF _H	< 10 Mbytes	Minus TwinCAN
TwinCAN registers	20'0000 _H	20'07FF _H	2 Kbytes	Accessed via EBC
Reserved	01'0000 _H	1F'FFFF _H	< 2 Mbytes	Minus segment 0
SFR area	00'FE00 _H	00'FFFF _H	0.5 Kbyte	-
Dual-Port RAM	00'F600 _H	00'FDFF _H	2 Kbytes	-
Reserved for DPRAM	00'F200 _H	00'F5FF _H	1 Kbyte	-
ESFR area	00'F000 _H	00'F1FF _H	0.5 Kbyte	-
XSFR area	00'E000 _H	00'EFFF _H	4 Kbytes	-
Reserved	00'D000 _H	00'DFFF _H	6 Kbytes	-
Data SRAM	00'C000 _H	00'CFFF _H	4 Kbytes	3)
Reserved for DSRAM	00'8000 _H	00'BFFF _H	16 Kbytes	_
Reserved	00'000 _H	00'7FFF _H	32 Kbytes	_

Table 3 XC164CM Memory Map

1) The areas marked with "<" are slightly smaller than indicated, see column "Notes".



Table 4XC164CM Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location ¹⁾	Trap Number
GPT2 CAPREL Register	GPT12E_CRIC	xx'009C _H	27 _H / 39 _D
A/D Conversion Complete	ADC_CIC	xx'00A0 _H	28 _H / 40 _D
A/D Overrun Error	ADC_EIC	xx'00A4 _H	29 _H / 41 _D
ASC0 Transmit	ASC0_TIC	xx'00A8 _H	2A _H / 42 _D
ASC0 Transmit Buffer	ASC0_TBIC	xx'011C _H	47 _H / 71 _D
ASC0 Receive	ASC0_RIC	xx'00AC _H	2B _H / 43 _D
ASC0 Error	ASC0_EIC	xx'00B0 _H	2C _H / 44 _D
ASC0 Autobaud	ASC0_ABIC	xx'017C _H	5F _H / 95 _D
SSC0 Transmit	SSC0_TIC	xx'00B4 _H	2D _H / 45 _D
SSC0 Receive	SSC0_RIC	xx'00B8 _H	2E _H / 46 _D
SSC0 Error	SSC0_EIC	xx'00BC _H	2F _H / 47 _D
PLL/OWD	PLLIC	xx'010C _H	43 _H / 67 _D
ASC1 Transmit	ASC1_TIC	xx'0120 _H	48 _H / 72 _D
ASC1 Transmit Buffer	ASC1_TBIC	xx'0178 _H	5E _H / 94 _D
ASC1 Receive	ASC1_RIC	xx'0124 _H	49 _H / 73 _D
ASC1 Error	ASC1_EIC	xx'0128 _H	4A _H / 74 _D
ASC1 Autobaud	ASC1_ABIC	xx'0108 _H	42 _H / 66 _D
End of PEC Subchannel	EOPIC	xx'0130 _H	4C _H / 76 _D
CAPCOM6 Timer T12	CCU6_T12IC	xx'0134 _H	4D _H / 77 _D
CAPCOM6 Timer T13	CCU6_T13IC	xx'0138 _H	4E _H / 78 _D
CAPCOM6 Emergency	CCU6_EIC	xx'013C _H	4F _H / 79 _D
CAPCOM6	CCU6_IC	xx'0140 _H	50 _H / 80 _D
SSC1 Transmit	SSC1_TIC	xx'0144 _H	51 _H / 81 _D
SSC1 Receive	SSC1_RIC	xx'0148 _H	52 _H / 82 _D
SSC1 Error	SSC1_EIC	xx'014C _H	53 _H / 83 _D
CAN0	CAN_0IC	xx'0150 _H	54 _H / 84 _D
CAN1	CAN_1IC	xx'0154 _H	55 _H / 85 _D
CAN2	CAN_2IC	xx'0158 _H	56 _H / 86 _D
CAN3	CAN_3IC	xx'015C _H	57 _H / 87 _D
CAN4	CAN_4IC	xx'0164 _H	59 _H / 89 _D



3.5 Capture/Compare Unit (CAPCOM2)

The CAPCOM unit supports generation and control of timing sequences on up to 16 channels with a maximum resolution of 1 system clock cycle (8 cycles in staggered mode). The CAPCOM unit is typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PWM), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Two 16-bit timers (T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustments to the application specific requirements. In addition, an external count input for CAPCOM timer T7 allows event scheduling for the capture/compare registers relative to external events.

The capture/compare register array contains 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer (T7 or T8, respectively), and programmed for capture or compare function.

10 registers of the CAPCOM2 module have each one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

Compare Modes	Function
Mode 0	Interrupt-only compare mode; Several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; Several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; Only one compare interrupt per timer period is generated
Mode 3	Pin set '1' on match; pin reset '0' on compare timer overflow; Only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; Pin toggles on each compare match; Several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; Can be used with any compare mode

Table 6	Compare	Modes	(CAPCOM2)

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched ('captured') into the capture/compare



3.7 General Purpose Timer (GPT12E) Unit

The GPT12E unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e.g. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.



count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM2 timers, and to cause a reload from the CAPREL register.

The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows the XC164CM to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) may also be generated upon transitions of GPT1 timer T3's inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.



3.9 A/D Converter

For analog signal measurement, a 10-bit A/D converter with 14 multiplexed input channels and a sample and hold circuit has been integrated on-chip. It uses the method of successive approximation. The sample time (for loading the capacitors) and the conversion time is programmable (in two modes) and can thus be adjusted to the external circuitry. The A/D converter can also operate in 8-bit conversion mode, where the conversion time is further reduced.

Overrun error detection/protection is provided for the conversion result register (ADDAT): either an interrupt request will be generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended in such a case until the previous result has been read.

For applications which require less analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converter of the XC164CM supports four different conversion modes. In the standard Single Channel conversion mode, the analog level on a specified channel is sampled once and converted to a digital result. In the Single Channel Continuous mode, the analog level on a specified channel is repeatedly sampled and converted without software intervention. In the Auto Scan mode, the analog levels on a prespecified number of channels are sequentially sampled and converted. In the Auto Scan Continuous mode, the prespecified channels are repeatedly sampled and converted. In addition, the conversion of a specific channel can be inserted (injected) into a running sequence without disturbing this sequence. This is called Channel Injection Mode.

The Peripheral Event Controller (PEC) may be used to automatically store the conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer.

After each reset and also during normal operation the ADC automatically performs calibration cycles. This automatic self-calibration constantly adjusts the converter to changing operating conditions (e.g. temperature) and compensates process variations.

These calibration cycles are part of the conversion cycle, so they do not affect the normal operation of the A/D converter.

In order to decouple analog inputs from digital noise and to avoid input trigger noise those pins used for analog input can be disconnected from the digital input stages under software control. This can be selected for each pin separately via register P5DIDIS (Port 5 Digital Input Disable).

The Auto-Power-Down feature of the A/D converter minimizes the power consumption when no conversion is in progress.



Summary of Features

- CAN functionality according to CAN specification V2.0 B active
- Data transfer rate up to 1 Mbit/s
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality and Basic CAN functionality for each message object
- 32 flexible message objects
 - Assignment to one of the two CAN nodes
 - Configuration as transmit object or receive object
 - Concatenation to a 2-, 4-, 8-, 16-, or 32-message buffer with FIFO algorithm
 - Handling of frames with 11-bit or 29-bit identifiers
 - Individual programmable acceptance mask register for filtering for each object
 - Monitoring via a frame counter
 - Configuration for Remote Monitoring Mode
- Up to eight individually programmable interrupt nodes can be used
- CAN Analyzer Mode for bus monitoring is implemented

3.13 LXBus Controller (EBC)

The EBC only controls accesses to resources connected to the on-chip LXBus. The LXBus is an internal representation of the external bus and allows accessing integrated peripherals and modules in the same way as external components.

The TwinCAN module is connected and accessed via the LXBus.



Table 8Instruction Set Summary (cont'd)					
Mnemonic	Description	Bytes			
NOP	Null operation	2			
CoMUL/CoMAC	Multiply (and accumulate)	4			
CoADD/CoSUB	Add/Subtract	4			
Co(A)SHR	(Arithmetic) Shift right	4			
CoSHL	Shift left	4			
CoLOAD/STORE	Load accumulator/Store MAC register	4			
CoCMP	Compare	4			
CoMAX/MIN	Maximum/Minimum	4			
CoABS/CoRND	Absolute value/Round accumulator	4			
CoMOV	Data move	4			
CoNEG/NOP	Negate accumulator/Null operation	4			



4.2 DC Parameters

These parameters are static or average values, which may be exceeded during switching transitions (e.g. output current).

Table 11	DC Characteristics	(Operating Conditions apply) ¹⁾
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Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Input low voltage TTL (all except XTAL1)	V _{IL}	SR	-0.5	0.2 × V _{DDP} - 0.1	V	-
Input low voltage XTAL1 ²⁾	V _{ILC}	SR	-0.5	$0.3 imes V_{ m DDI}$	V	-
Input low voltage (Special Threshold)	V _{ILS}	SR	-0.5	$0.45 \times V_{\text{DDP}}$	V	3)
Input high voltage TTL (all except XTAL1)	V _{IH}	SR	$0.2 \times V_{\text{DDP}} + 0.9$	V _{DDP} + 0.5	V	-
Input high voltage XTAL1 ²⁾	V _{IHC}	SR	$0.7 imes V_{ m DDI}$	V _{DDI} + 0.5	V	-
Input high voltage (Special Threshold)	V _{IHS}	SR	0.8 × V _{DDP} - 0.2	V _{DDP} + 0.5	V	3)
Input Hysteresis (Special Threshold)	HYS		$0.04 \times V_{\text{DDP}}$	-	V	V_{DDP} in [V], Series resis- tance = 0 $\Omega^{3)}$
Output low voltage	V _{OL}	CC	_	1.0	V	$I_{\rm OL} \leq I_{\rm OLmax}^{4)}$
			-	0.45	V	$I_{\rm OL} \leq I_{\rm OLnom}^{4)5)}$
Output high voltage ⁶⁾	V _{OH}	CC	V _{DDP} - 1.0	_	V	$I_{\rm OH} \geq {I_{\rm OHmax}}^{\rm 4)}$
			V _{DDP} - 0.45	_	V	$I_{\rm OH} \ge I_{\rm OHnom}^{4)5)}$
Input leakage current (Port 5) ⁷⁾	I _{OZ1}	CC	-	±300	nA	$0 V < V_{IN} < V_{DDP},$ $T_A \le 125 \text{ °C}$
				±200	nA	$0 V < V_{IN} < V_{DDP},$ $T_A \le 85 \ ^{\circ}C^{12)}$
Input leakage current (all other ⁸⁾) ⁷⁾	I _{OZ2}	CC	-	±500	nA	$0.45 V < V_{IN} < V_{DDP}$
Configuration pull-up	<i>I</i> _{CPUH} ¹⁰⁾		—	-10	μA	$V_{\rm IN} = V_{\rm IHmin}$
current ⁹⁾	$I_{\rm CPUL}^{11)}$		-100	-	μA	$V_{\rm IN} = V_{\rm ILmax}$



Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
XTAL1 input current	$I_{\rm IL}$	CC	_	±20	μA	$0 V < V_{IN} < V_{DDI}$
Pin capacitance ¹²⁾ (digital inputs/outputs)	C _{IO}	CC	-	10	pF	-

Table 11 DC Characteristics (Operating Conditions apply)¹⁾ (cont'd)

1) Keeping signal levels within the limits specified in this table, ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV} .

- 2) If XTAL1 is driven by a crystal, reaching an amplitude (peak to peak) of $0.4 \times V_{DDI}$ is sufficient.
- 3) This parameter is tested for P3, P9.

4) The maximum deliverable output current of a port driver depends on the selected output driver mode, see Table 12, Current Limits for Port Output Drivers. The limit for pin groups must be respected.

- 5) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are guaranteed.
- 6) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.
- 7) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV} .
- The driver of P3.15 is designed for faster switching, because this pin can deliver the system clock (CLKOUT). The maximum leakage current for P3.15 is, therefore, increased to 1 μA.
- 9) During a hardware reset this specification is valid for configuration on P1H.4, P1H.5, P9.4 and P9.5. After a hardware reset this specification is valid for NMI.
- 10) The maximum current may be drawn while the respective signal line remains inactive.
- 11) The minimum current must be drawn to drive the respective signal line active.
- 12) Not subject to production test verified by design/characterization.

Port Output Driver Mode	Maximum Output Current $(I_{OLmax}, -I_{OHmax})^{1)}$	Nominal Output Current (<i>I</i> _{OLnom} , - <i>I</i> _{OHnom})
Strong driver	10 mA	2.5 mA
Medium driver	4.0 mA	1.0 mA
Weak driver	0.5 mA	0.1 mA

Table 12 Current Limits for Port Output Drivers

 An output current above |I_{OXnom}| may be drawn from up to three pins at the same time. For any group of 16 neighboring port output pins the total output current in each direction (ΣI_{OL} and Σ-I_{OH}) must remain below 50 mA.



Table 13Power Consumption XC164CM (Operating Conditions apply)

Parameter	Sym-	Lim	nit Values	Unit	Test Condition	
	bol	Min.	Max.			
Power supply current (active) with all peripherals active	$I_{\rm DDI}$	_	15 + 2.6 × <i>f</i> _{CPU}	mA	<i>f</i> _{CPU} in [MHz] ¹⁾²⁾ , -16F derivatives	
		_	10 + 2.6 × f _{CPU}	mA	<i>f</i> _{CPU} in [MHz] ¹⁾²⁾ , -4F/8F derivatives	
Pad supply current	$I_{\rm DDP}$	_	5	mA	3)	
Idle mode supply current with all peripherals active	I _{IDX}	-	15 + 1.2 × <i>f</i> _{СРU}	mA	<i>f</i> _{CPU} in [MHz] ²⁾ , -16F derivatives	
		_	10 + 1.2 × f _{CPU}	mA	<i>f</i> _{CPU} in [MHz] ²⁾ , -4F/8F derivatives	
Sleep and Power down mode supply current caused by leakage ⁴⁾	I _{PDL} ⁵⁾	_	84,000 × e ^{-α}	mA	$V_{\text{DDI}} = V_{\text{DDImax}}^{6)}$ T_{J} in [°C] α = 4380 / (273 + T_{J} -16F derivatives	
		_	128,000 × e ^{-α}	mA	α = 4670 / (273 + T _J) -4F/8F derivatives	
Sleep and Power down mode supply current caused by leakage and the RTC running, clocked by the main oscillator ⁴⁾	I _{PDM} ⁷⁾	_	0.6 + 0.02 × f _{OSC} + I _{PDL}	mA	$V_{\text{DDI}} = V_{\text{DDImax}}$ f_{OSC} in [MHz]	

1) During Flash programming or erase operations the supply current is increased by max. 5 mA.

2) The supply current is a function of the operating frequency. This dependency is illustrated in Figure 11. These parameters are tested at V_{DDImax} and maximum CPU clock frequency with all outputs disconnected and all inputs at V_{IL} or V_{IH} .

- 3) The pad supply voltage pins (V_{DDP}) mainly provides the current consumed by the pin output drivers. A small amount of current is consumed even though no outputs are driven, because the drivers' input stages are switched and also the Flash module draws some power from the V_{DDP} supply.
- 4) The total supply current in Sleep and Power down mode is the sum of the temperature dependent leakage current and the frequency dependent current for RTC and main oscillator.
- 5) This parameter is determined mainly by the transistor leakage currents. This current heavily depends on the junction temperature (see Figure 13). The junction temperature T_J is the same as the ambient temperature T_A if no current flows through the port output drivers. Otherwise, the resulting temperature difference must be taken into account.
- 6) All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DDP} 0.1 V to V_{DDP} , all outputs (including pins configured as outputs) disconnected. This parameter is tested at 25 °C and is valid for $T_{\text{J}} \ge$ 25 °C.
- 7) This parameter is determined mainly by the current consumed by the oscillator switched to low gain mode (see Figure 12). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The given values refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.



4.3 Analog/Digital Converter Parameters

These parameters describe how the optimum ADC performance can be reached.

Parameter	Symbol		Limit	Values	Unit	Test
			Min.	Max.		Condition
Analog reference supply	V _{AREF}	SR	4.5	V _{DDP} + 0.1	V	1)
Analog reference ground	V_{AGND}	SR	V _{SS} - 0.1	V _{SS} + 0.1	V	-
Analog input voltage range	V_{AIN}	SR	V _{AGND}	V _{AREF}	V	2)
Basic clock frequency	$f_{\sf BC}$		0.5	20	MHz	3)
Conversion time for 10-bit result ⁴⁾	t _{C10P}	CC	$52 \times t_{\rm BC}$ + $t_{\rm S}$ + $6 \times t_{\rm SYS}$		_	Post-calibr. on
	<i>t</i> _{C10}	CC	$40 \times t_{\rm BC}$ + $t_{\rm BC}$	$t_{\rm S}$ + 6 × $t_{\rm SYS}$	_	Post-calibr. off
Conversion time for 8-bit result ⁴⁾	t _{C8P}	CC	$44 \times t_{\rm BC}$ + $t_{\rm BC}$	$t_{\rm S}$ + 6 × $t_{\rm SYS}$	_	Post-calibr. on
	t _{C8}	CC	$32 \times t_{\rm BC}$ + $t_{\rm BC}$	$t_{\rm S}$ + 6 × $t_{\rm SYS}$	_	Post-calibr. off
Calibration time after reset	t _{CAL}	CC	484	11,696	t _{BC}	5)
Total unadjusted error	TUE	CC	_	±2	LSB	1)
Total capacitance of an analog input	C_{AINT}	CC	_	15	pF	6)
Switched capacitance of an analog input	C_{AINS}	CC	_	10	pF	6)
Resistance of the analog input path	R _{AIN}	CC	_	2	kΩ	6)
Total capacitance of the reference input	C_{AREFT}	CC	_	20	pF	6)
Switched capacitance of the reference input	C_{AREFS}	CC	_	15	pF	6)
Resistance of the reference input path	R _{AREF}	СС	_	1	kΩ	6)

Table 14	A/D Converter Characteristics (Operating Conditions apply)
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1) TUE is tested at $V_{AREF} = V_{DDP} + 0.1 \text{ V}$, $V_{AGND} = 0 \text{ V}$. It is verified by design for all other voltages within the defined voltage range.

If the analog reference supply voltage drops below 4.5 V (i.e. $V_{AREF} \ge 4.0$ V) or exceeds the power supply voltage by up to 0.2 V (i.e. $V_{AREF} = V_{DDP} + 0.2$ V) the maximum TUE is increased to ±3 LSB. This range is not subject to production test.

The specified TUE is guaranteed only, if the absolute sum of input overload currents on Port 5 pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the respective period of time. During the reset calibration sequence the maximum TUE may be ±4 LSB.



The used mechanism to generate the master clock is selected by register PLLCON.

CPU and EBC are clocked with the CPU clock signal f_{CPU} . The CPU clock can have the same frequency as the master clock ($f_{CPU} = f_{MC}$) or can be the master clock divided by two: $f_{CPU} = f_{MC}$ / 2. This factor is selected by bit CPSYS in register SYSCON1.

The specification of the external timing (AC Characteristics) depends on the period of the CPU clock, called "TCP".

The other peripherals are supplied with the system clock signal f_{SYS} which has the same frequency as the CPU clock signal f_{CPU} .

Bypass Operation

When bypass operation is configured (PLLCTRL = $0x_B$) the master clock is derived from the internal oscillator (input clock signal XTAL1) through the input- and output-prescalers:

 $f_{MC} = f_{OSC} / ((PLLIDIV + 1) \times (PLLODIV + 1)).$

If both divider factors are selected as '1' (PLLIDIV = PLLODIV = '0') the frequency of f_{MC} directly follows the frequency of f_{OSC} so the high and low time of f_{MC} is defined by the duty cycle of the input clock f_{OSC} .

The lowest master clock frequency is achieved by selecting the maximum values for both divider factors:

 $f_{\rm MC} = f_{\rm OSC} / ((3 + 1) \times (14 + 1)) = f_{\rm OSC} / 60.$

Phase Locked Loop (PLL)

When PLL operation is configured (PLLCTRL = 11_B) the on-chip phase locked loop is enabled and provides the master clock. The PLL multiplies the input frequency by the factor **F** ($f_{MC} = f_{OSC} \times \mathbf{F}$) which results from the input divider, the multiplication factor, and the output divider (**F** = PLLMUL+1 / (PLLIDIV+1 × PLLODIV+1)). The PLL circuit synchronizes the master clock to the input clock. This synchronization is done smoothly, i.e. the master clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of $f_{\rm MC}$ is constantly adjusted so it is locked to $f_{\rm OSC}$. The slight variation causes a jitter of $f_{\rm MC}$ which also affects the duration of individual TCMs.

The timing listed in the AC Characteristics refers to TCPs. Because $f_{\rm CPU}$ is derived from $f_{\rm MC}$, the timing must be calculated using the minimum TCP possible under the respective circumstances.

The actual minimum value for TCP depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so it corresponds to the applied input frequency (crystal or oscillator) the relative deviation for periods of more than one TCP is lower than for one single TCP (see formula and **Figure 16**).



This is especially important for bus cycles using waitstates and e.g. for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler (K = PLLODIV+1) to generate the master clock signal f_{MC} . Therefore, the number of VCO cycles can be represented as K × N, where N is the number of consecutive f_{MC} cycles (TCM).

For a period of $\mathbf{N} \times \text{TCM}$ the accumulated PLL jitter is defined by the deviation D_N :

 D_N [ns] = ±(1.5 + 6.32 × N / f_{MC}); f_{MC} in [MHz], N = number of consecutive TCMs.

So, for a period of 3 TCMs @ 20 MHz and K = 12: $D_3 = \pm(1.5 + 6.32 \times 3 / 20) = 2.448$ ns. This formula is applicable for K × N < 95. For longer periods the K × N = 95 value can be

used. This steady value can be approximated by: D_{Nmax} [ns] = ±(1.5 + 600 / (K × f_{MC})).



Figure 16 Approximated Accumulated PLL Jitter

Note: The bold lines indicate the minimum accumulated jitter which can be achieved by selecting the maximum possible output prescaler factor K.



4.4.3 External Clock Drive XTAL1

These parameters define the external clock supply for the XC164CM.

Table 19	External Clock Drive	Characteristics	(Operating	Conditions apply)
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Parameter	ameter Symbol		Lir	Unit	
			Min.	Max.	
Oscillator period	t _{OSC}	SR	25	250 ¹⁾	ns
High time ²⁾	<i>t</i> ₁	SR	6	_	ns
Low time ²⁾	<i>t</i> ₂	SR	6	_	ns
Rise time ²⁾	<i>t</i> ₃	SR	_	8	ns
Fall time ²⁾	t_4	SR	_	8	ns

1) The maximum limit is only relevant for PLL operation to ensure the minimum input frequency for the PLL.

2) The clock input signal must reach the defined levels $V_{\rm ILC}$ and $V_{\rm IHC}$.



Figure 17 External Clock Drive XTAL1

Note: If the on-chip oscillator is used together with a crystal or a ceramic resonator, the oscillator frequency is limited to a range of 4 MHz to 16 MHz.

It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.

When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is verified by design only (not subject to production test).