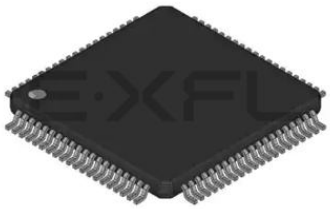
Infineon Technologies - XC2387E136F128LAAKFUMA1 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	128MHz
Connectivity	CANbus, EBI/EMI, FlexRay, I²C, LINbus, SPI, UART/USART
Peripherals	I²S, POR, PWM, WDT
Number of I/O	118
Program Memory Size	1.06MB (1.06M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	90K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2387e136f128laakfuma1

16/32-Bit

Architecture

XC2385A, XC2387A

16/32-Bit Single-Chip Microcontroller with
32-Bit Performance
XC2000 Family / Base Line

Data Sheet

V2.12 2014-06

Microcontrollers

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
39	P5.4	I	In/A	**Bit 4 of Port 5, General Purpose Input**
	ADC0_CH4	I	In/A	**Analog Input Channel 4 for ADC0**
	CCU63_T12HRB	I	In/A	**External Run Control Input for T12 of CCU63**
	T3EUDA	I	In/A	**GPT12E Timer T3 External Up/Down Control Input**
	TMS_A	I	In/A	**JTAG Test Mode Selection Input**
40	P5.5	I	In/A	**Bit 5 of Port 5, General Purpose Input**
	ADC0_CH5	I	In/A	**Analog Input Channel 5 for ADC0**
	CCU60_T12HRB	I	In/A	**External Run Control Input for T12 of CCU60**
41	P5.6	I	In/A	**Bit 6 of Port 5, General Purpose Input**
	ADC0_CH6	I	In/A	**Analog Input Channel 6 for ADC0**
42	P5.7	I	In/A	**Bit 7 of Port 5, General Purpose Input**
	ADC0_CH7	I	In/A	**Analog Input Channel 7 for ADC0**
43	P5.8	I	In/A	**Bit 8 of Port 5, General Purpose Input**
	ADC0_CH8	I	In/A	**Analog Input Channel 8 for ADC0**
	ADC1_CH8	I	In/A	**Analog Input Channel 8 for ADC1**
	CCU6x_T12HRC	I	In/A	**External Run Control Input for T12 of CCU60/1/2/3**
	CCU6x_T13HRC	I	In/A	**External Run Control Input for T13 of CCU60/1/2/3**
	U2C0_DX0F	I	In/A	**USIC2 Channel 0 Shift Data Input**
44	P5.9	I	In/A	**Bit 9 of Port 5, General Purpose Input**
	ADC0_CH9	I	In/A	**Analog Input Channel 9 for ADC0**
	ADC1_CH9	I	In/A	**Analog Input Channel 9 for ADC1**
	CC2_T7IN	I	In/A	**CAPCOM2 Timer T7 Count Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
64	P2.4	O0 / I	St/B	**Bit 4 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CC2_CC17	O3 / I	St/B	**CAPCOM2 CC17IO Capture Inp./ Compare Out.**
	A17	OH	St/B	**External Bus Interface Address Line 17**
	ESR1_0	I	St/B	**ESR1 Trigger Input 0**
	U0C0_DX0F	I	St/B	**USIC0 Channel 0 Shift Data Input**
	RxDC1A	I	St/B	**CAN Node 1 Receive Data Input**
65	P11.1	O0 / I	St/B	**Bit 1 of Port 11, General Purpose Input/Output**
	CCU61_COUT61	O1	St/B	**CCU61 Channel 1 Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CCU63_CCPOS1A	I	St/B	**CCU63 Position Input 1**
	CCU61_CTRAPD	I	St/B	**CCU61 Emergency Trap Input**
66	P11.0	O0 / I	St/B	**Bit 0 of Port 11, General Purpose Input/Output**
	CCU61_COUT60	O1	St/B	**CCU61 Channel 0 Output**
	CCU63_CCPOS0A	I	St/B	**CCU63 Position Input 0**
	RxDC0F	I	St/B	**CAN Node 0 Receive Data Input**
	ESR1_7	I	St/B	**ESR1 Trigger Input 7**
67	P2.5	O0 / I	St/B	**Bit 5 of Port 2, General Purpose Input/Output**
	U0C0_SCLKOUT	O1	St/B	**USIC0 Channel 0 Shift Clock Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CC2_CC18	O3 / I	St/B	**CAPCOM2 CC18IO Capture Inp./ Compare Out.**
	A18	OH	St/B	**External Bus Interface Address Line 18**
	U0C0_DX1D	I	St/B	**USIC0 Channel 0 Shift Clock Input**
	ESR1_10	I	St/B	**ESR1 Trigger Input 10**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
111	P1.0	O0 / I	St/B	**Bit 0 of Port 1, General Purpose Input/Output**
	U1C0_MCLKOUT	O1	St/B	**USIC1 Channel 0 Master Clock Output**
	U1C0_SELO4	O2	St/B	**USIC1 Channel 0 Select/Control 4 Output**
	A8	OH	St/B	**External Bus Interface Address Line 8**
	ESR1_3	I	St/B	**ESR1 Trigger Input 3**
	CCU62_CTRAPB	I	St/B	**CCU62 Emergency Trap Input**
	T6INB	I	St/B	**GPT12E Timer T6 Count/Gate Input**
112	P9.0	O0 / I	St/B	**Bit 0 of Port 9, General Purpose Input/Output**
	CCU63_CC60	O1	St/B	**CCU63 Channel 0 Output**
	CCU63_CC60INA	I	St/B	**CCU63 Channel 0 Input**
	T6EUDB	I	St/B	**GPT12E Timer T6 External Up/Down Control Input**
113	P10.8	O0 / I	St/B	**Bit 8 of Port 10, General Purpose Input/Output**
	U0C0_MCLKOUT	O1	St/B	**USIC0 Channel 0 Master Clock Output**
	U0C1_SELO0	O2	St/B	**USIC0 Channel 1 Select/Control 0 Output**
	U2C1_DOUT	O3	St/B	**USIC2 Channel 1 Shift Data Output**
	AD8	OH / IH	St/B	**External Bus Interface Address/Data Line 8**
	CCU60_CCPOS1A	I	St/B	**CCU60 Position Input 1**
	U0C0_DX1C	I	St/B	**USIC0 Channel 0 Shift Clock Input**
	$\overline{\text{BRKIN\_B}}$	I	St/B	**OCDS Break Signal Input**
	T3EUDB	I	St/B	**GPT12E Timer T3 External Up/Down Control Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
123	P10.13	O0 / I	St/B	**Bit 13 of Port 10, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	U1C0_SELO 3	O3	St/B	**USIC1 Channel 0 Select/Control 3 Output**
	$\overline{WR}$/$\overline{WRL}$	OH	St/B	**External Bus Interface Write Strobe Output** Active for each external write access, when $\overline{WR}$, active for ext. writes to the low byte, when $\overline{WRL}$.
	U1C0_DX0D	I	St/B	**USIC1 Channel 0 Shift Data Input**
124	P1.3	O0 / I	St/B	**Bit 3 of Port 1, General Purpose Input/Output**
	CCU62_COU T63	O1	St/B	**CCU62 Channel 3 Output**
	U1C0_SELO 7	O2	St/B	**USIC1 Channel 0 Select/Control 7 Output**
	U2C0_SELO 4	O3	St/B	**USIC2 Channel 0 Select/Control 4 Output**
	A11	OH	St/B	**External Bus Interface Address Line 11**
	ESR2_4	I	St/B	**ESR2 Trigger Input 4**
	CCU62_T12 HRB	I	St/B	**External Run Control Input for T12 of CCU62**
125	P9.4	O0 / I	St/B	**Bit 4 of Port 9, General Purpose Input/Output**
	CCU63_COU T61	O1	St/B	**CCU63 Channel 1 Output**
	U2C0_DOUT	O2	St/B	**USIC2 Channel 0 Shift Data Output**
	CCU62_COU T63	O3	St/B	**CCU62 Channel 3 Output**

2.2 Identification Registers

The identification registers describe the current version of the XC238xA and of its modules.

Table 7 XC238xA Identification Registers

Short Name	Value	Address	Notes
SCU_IDMANUF	1820_H	$00'F07E_H$	
SCU_IDCHIP	3801_H	$00'F07C_H$	
SCU_IDMEM	$30D0_H$	$00'F07A_H$	
SCU_IDPROG	1313_H	$00'F078_H$	
JTAG_ID	$0017'E083_H$	---	marking EES-AA, ES-AA or AA

3.1 Memory Subsystem and Organization

The memory space of the XC238xA is configured in the von Neumann architecture. In this architecture all internal and external resources, including code memory, data memory, registers and I/O ports, are organized in the same linear address space.

Table 8 XC238xA Memory Map [1)]

Address Area	Start Loc.	End Loc.	Area Size[2)]	Notes
IMB register space	$FF'FF00_H$	$FF'FFFF_H$	256 Bytes	–
Reserved (Access trap)	$F0'0000_H$	$FF'FEFF_H$	<1 Mbyte	Minus IMB registers
Reserved for EPSRAM	$E8'8000_H$	$EF'FFFF_H$	480 Kbytes	Mirrors EPSRAM
Emulated PSRAM	$E8'0000_H$	$E8'7FFF_H$	32 Kbytes	With Flash timing
Reserved for PSRAM	$E0'8000_H$	$E7'FFFF_H$	480 Kbytes	Mirrors PSRAM
Program SRAM	$E0'0000_H$	$E0'7FFF_H$	32 Kbytes	Maximum speed
Reserved for Flash	$CD'0000_H$	$DF'FFFF_H$	<1.25 Mbytes	–
Program Flash 3	$CC'0000_H$	$CC'FFFF_H$	64 Kbytes	–
Program Flash 2	$C8'0000_H$	$CB'FFFF_H$	256 Kbytes	–
Program Flash 1	$C4'0000_H$	$C7'FFFF_H$	256 Kbytes	–
Program Flash 0	$C0'0000_H$	$C3'FFFF_H$	256 Kbytes	[3)]
External memory area	$40'0000_H$	$BF'FFFF_H$	8 Mbytes	–
Available Ext. IO area[4)]	$21'0000_H$	$3F'FFFF_H$	< 2 Mbytes	Minus USIC/CAN
Reserved	$20'BC00_H$	$20'FFFF_H$	17 Kbytes	–
USIC alternate regs.	$20'B000_H$	$20'BFFF_H$	4 Kbytes	Accessed via EBC
MultiCAN alternate regs.	$20'8000_H$	$20'AFFF_H$	12 Kbytes	Accessed via EBC
Reserved	$20'6000_H$	$20'7FFF_H$	8 Kbytes	–
USIC registers	$20'4000_H$	$20'5FFF_H$	8 Kbytes	Accessed via EBC
MultiCAN registers	$20'0000_H$	$20'3FFF_H$	16 Kbytes	Accessed via EBC
External memory area	$01'0000_H$	$1F'FFFF_H$	< 2 Mbytes	Minus segment 0
SFR area	$00'FE00_H$	$00'FFFF_H$	0.5 Kbyte	–
Dual-Port RAM	$00'F600_H$	$00'FDFF_H$	2 Kbytes	–
Reserved for DPRAM	$00'F200_H$	$00'F5FF_H$	1 Kbyte	–
ESFR area	$00'F000_H$	$00'F1FF_H$	0.5 Kbyte	–
XSFR area	$00'E000_H$	$00'EFFF_H$	4 Kbytes	–

8 Kbytes of on-chip Stand-By SRAM (SBRAM) provide storage for system-relevant user data that must be preserved while the major part of the device is powered down. The SBRAM is accessed via a specific interface and is powered in domain M.

1024 bytes (2 × 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word-wide registers which are used to control and monitor functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XC2000 Family. In order to ensure upward compatibility they should either not be accessed or written with zeros.

The on-chip Flash memory stores code, constant data, and control data. The on-chip Flash memory consists of 1 module of 64 Kbytes (preferably for data storage) and modules with a maximum capacity of 256 Kbytes each. Each module is organized in sectors of 4 Kbytes.
The uppermost 4-Kbyte sector of segment 0 (located in Flash module 0) is used internally to store operation control parameters and protection information.

Note: The actual size of the Flash memory depends on the chosen device type.

Each sector can be separately write protected[1)], erased and programmed (in blocks of 128 Bytes). The complete Flash area can be read-protected. A user-defined password sequence temporarily unlocks protected areas. The Flash modules combine 128-bit read access with protected and efficient writing algorithms for programming and erasing. Dynamic error correction provides extremely high read data security for all read access operations. Access to different Flash modules can be executed in parallel.
For Flash parameters, please see **Section 4.5**.

Memory Content Protection

The contents of on-chip memories can be protected against soft errors (induced e.g. by radiation) by activating the parity mechanism or the Error Correction Code (ECC).
The parity mechanism can detect a single-bit error and prevent the software from using incorrect data or executing incorrect instructions.
The ECC mechanism can detect and automatically correct single-bit errors. This supports the stable operation of the system.

It is strongly recommended to activate the ECC mechanism wherever possible because this dramatically increases the robustness of an application against such soft errors.

1) To save control bits, sectors are clustered for protection purposes, they remain separate for programming/erasing.

3.6 Interrupt System

The architecture of the XC238xA supports several mechanisms for fast and flexible response to service requests; these can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

Where in a standard interrupt service the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source pointer, the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are particularly well suited to supporting the transmission or reception of blocks of data. The XC238xA has eight PEC channels, each whith fast interrupt-driven data transfer capabilities.

With a minimum interrupt response time of 7/11[1)] CPU clocks, the XC238xA can react quickly to the occurrence of non-deterministic events.

Interrupt Nodes and Source Selection

The interrupt system provides 96 physical nodes with separate control register containing an interrupt request flag, an interrupt enable flag and an interrupt priority bit field. Most interrupt sources are assigned to a dedicated node. A particular subset of interrupt sources shares a set of nodes. The source selection can be programmed using the interrupt source selection (ISSR) registers.

External Request Unit (ERU)

A dedicated External Request Unit (ERU) is provided to route and preprocess selected on-chip peripheral and external interrupt requests. The ERU features 4 programmable input channels with event trigger logic (ETL) a routing matrix and 4 output gating units (OGU). The ETL features rising edge, falling edge, or both edges event detection. The OGU combines the detected interrupt events and provides filtering capabilities depending on a programmable pattern match or miss.

Trap Processing

The XC238xA provides efficient mechanisms to identify and process exceptions or error conditions that arise during run-time, the so-called ‘Hardware Traps’. A hardware trap causes an immediate system reaction similar to a standard interrupt service (branching

1) Depending if the jump cache is used or not.

Table 9 Compare Modes (cont'd)

Compare Modes	Function
Mode 2	Interrupt-only compare mode; Only one compare interrupt per timer period is generated
Mode 3	Pin set '1' on match; pin reset '0' on compare timer overflow; Only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; Pin toggles on each compare match; Several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; Can be used with any compare mode

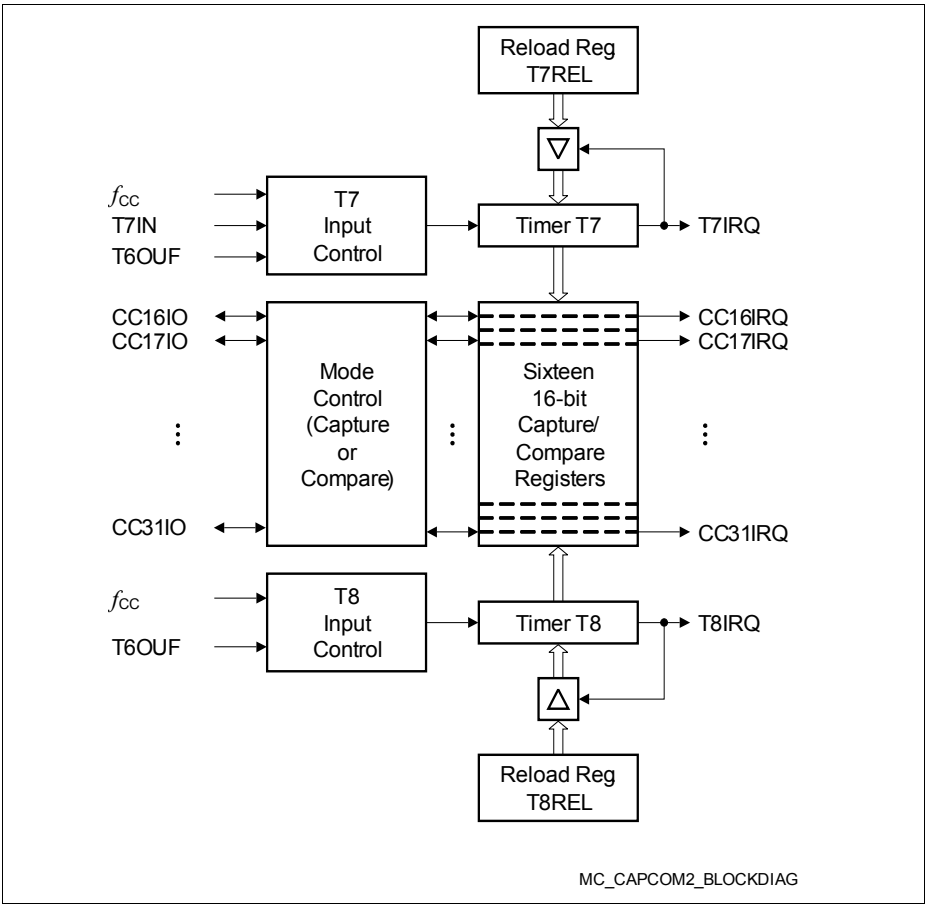


Figure 6 CAPCOM2 Unit Block Diagram

MultiCAN Features

- CAN functionality conforming to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Independent CAN nodes
- Set of independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality for message objects:
  - Can be assigned to one of the CAN nodes
  - Configurable as transmit or receive objects, or as message buffer FIFO
  - Handle 11-bit or 29-bit identifiers with programmable acceptance mask for filtering
  - Remote Monitoring Mode, and frame counter for monitoring
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

3.15 System Timer

The System Timer consists of a programmable prescaler and two concatenated timers (10 bits and 6 bits). Both timers can generate interrupt requests. The clock source can be selected and the timers can also run during power reduction modes.

Therefore, the System Timer enables the software to maintain the current time for scheduling functions or for the implementation of a clock.

3.18 Parallel Ports

The XC238xA provides up to 119 I/O lines which are organized into 11 input/output ports and 2 input ports. All port lines are bit-addressable, and all input/output lines can be individually (bit-wise) configured via port control registers. This configuration selects the direction (input/output), push/pull or open-drain operation, activation of pull devices, and edge characteristics (shape) and driver characteristics (output current) of the port drivers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. During the internal reset, all port pins are configured as inputs without pull devices active.

All port lines have alternate input or output functions associated with them. These alternate functions can be programmed to be assigned to various port pins to support the best utilization for a given application. For this reason, certain functions appear several times in **Table 10**.

All port lines that are not used for alternate functions may be used as general purpose I/O lines.

Table 10 Summary of the XC238xA's Ports

Port	Width	I/O	Connected Modules
P0	8	I/O	EBC (A7…A0), CCU6, USIC, CAN
P1	8	I/O	EBC (A15…A8), CCU6, USIC
P2	14	I/O	EBC (READY, $\overline{\text{BHE}}$, A23…A16, AD15…AD13, D15…D13), CAN, CC2, GPT12E, USIC, DAP/JTAG
P3	8	I/O	CAN, USIC
P4	8	I/O	EBC ($\overline{\text{CS3}}$…$\overline{\text{CS0}}$), CC2, CAN, GPT12E, USIC
P5	16	I	Analog Inputs, CCU6, DAP/JTAG, GPT12E, CAN
P6	4	I/O	ADC, CAN, GPT12E
P7	5	I/O	CAN, GPT12E, SCU, DAP/JTAG, CCU6, ADC, USIC
P8	7	I/O	CCU6, DAP/JTAG, USIC
P9	8	I/O	CCU6, DAP/JTAG, CAN
P10	16	I/O	EBC (ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, AD12…AD0, D12…D0), CCU6, USIC, DAP/JTAG, CAN
P11	6	I/O	CCU6, USIC, CAN
P15	8	I	Analog Inputs, GPT12E

4.1.3 Pad Timing Definition

If not otherwise noted, all timing parameters are tested and are valid for the corresponding output pins operating in strong driver, fast edge mode.
See also **“Pad Properties” on Page 113**.

4.1.4 Parameter Interpretation

The parameters listed in the following include both the characteristics of the XC238xA and its demands on the system. To aid in correctly interpreting the parameters when evaluating them for a design, they are marked accordingly in the column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the XC238xA provides signals with the specified characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the specified characteristics to the XC238xA.

Table 17 Leakage Power Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Leakage supply current (DMP_1 powered)[1]	I_{LK1} CC	–	0.03	0.05	mA	T_J= 25 °C[1]
		–	0.5	1.3	mA	T_J= 85 °C[1]
		–	2.1	6.2	mA	T_J= 125 °C[1]
		–	4.4	13.7	mA	T_J= 150 °C[1]

1) All inputs (including pins configured as inputs) are set at 0 V to 0.1 V or at V_{DDP} - 0.1 V to V_{DDP} and all outputs (including pins configured as outputs) are disconnected.

Note: A fraction of the leakage current flows through domain DMP_A (pin V_{DDPA}). This current can be calculated as 7 000 $\times e^{-\alpha}$, with α = 5 000 / (273 + 1.3$\times T_J$). For T_J = 150°C, this results in a current of 160 μA.

The leakage power consumption can be calculated according to the following formulas:

I_{LK0} = 500 000 × $e^{-\alpha}$, with α = 3 000 / (273 + B$\times T_J$)

Parameter B must be replaced by

- 1.0 for typical values
- 1.6 for maximum values

I_{LK1} = 600 000 × $e^{-\alpha}$, with α = 5 000 / (273 + B$\times T_J$)

Parameter B must be replaced by

- 1.0 for typical values
- 1.3 for maximum values

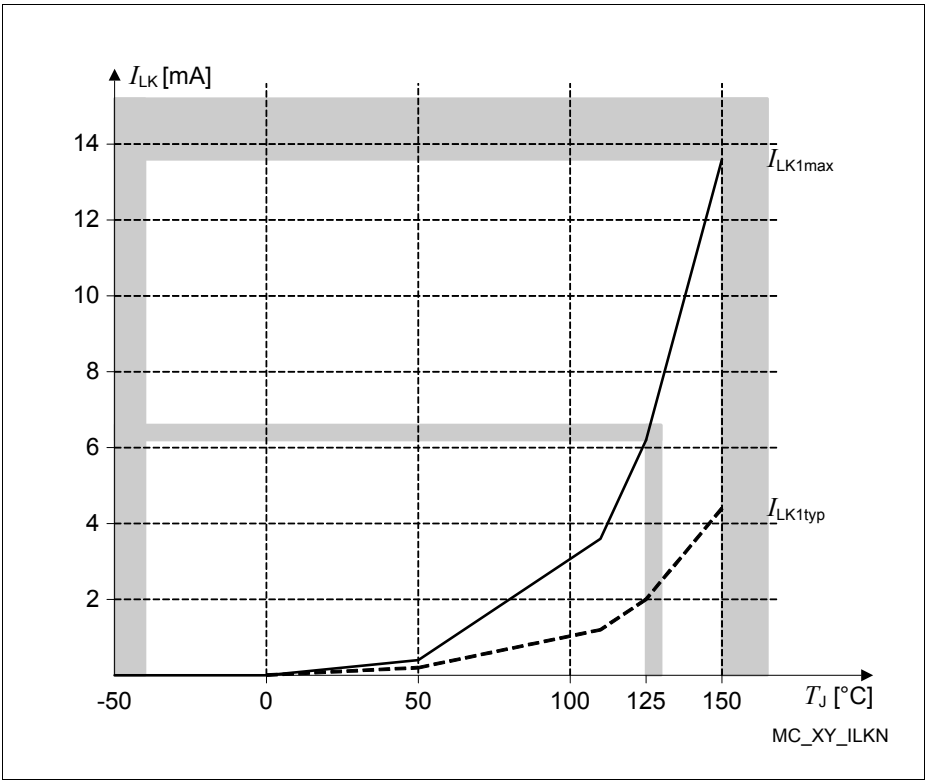


Figure 15 Leakage Supply Current as a Function of Temperature

The timing in the AC Characteristics refers to TCSs. Timing must be calculated using the minimum TCS possible under the given circumstances.
The actual minimum value for TCS depends on the jitter of the PLL. Because the PLL is constantly adjusting its output frequency to correspond to the input frequency (from crystal or oscillator), the accumulated jitter is limited. This means that the relative deviation for periods of more than one TCS is lower than for a single TCS (see formulas and **Figure 20**).

This is especially important for bus cycles using waitstates and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler K2 to generate the system clock signal f_{SYS}. The number of VCO cycles is K2 × **T**, where **T** is the number of consecutive f_{SYS} cycles (TCS).

The maximum accumulated jitter (long-term jitter) D_{Tmax} is defined by:

D_{Tmax} [ns] = ±(220 / (K2 × f_{SYS}) + 4.3)

This maximum value is applicable, if either the number of clock cycles T > (f_{SYS} / 1.2) or the prescaler value K2 > 17.

In all other cases for a timeframe of **T** × TCS the accumulated jitter D_T is determined by:

D_T [ns] = D_{Tmax} × [(1 - 0.058 × K2) × (T - 1) / (0.83 × f_{SYS} - 1) + 0.058 × K2]

f_{SYS} in [MHz] in all formulas.

Example, for a period of 3 TCSs @ 33 MHz and K2 = 4:

D_{max} = ±(220 / (4 × 33) + 4.3) = 5.97 ns (Not applicable directly in this case!)

D_3 = 5.97 × [(1 - 0.058 × 4) × (3 - 1) / (0.83 × 33 - 1) + 0.058 × 4]
= 5.97 × [0.768 × 2 / 26.39 + 0.232]
= 1.7 ns

Example, for a period of 3 TCSs @ 33 MHz and K2 = 2:

D_{max} = ±(220 / (2 × 33) + 4.3) = 7.63 ns (Not applicable directly in this case!)

D_3 = 7.63 × [(1 - 0.058 × 2) × (3 - 1) / (0.83 × 33 - 1) + 0.058 × 2]
= 7.63 × [0.884 × 2 / 26.39 + 0.116]
= 1.4 ns

4.6.4 Pad Properties

The output pad drivers of the XC238xA can operate in several user-selectable modes. Strong driver mode allows controlling external components requiring higher currents such as power bridges or LEDs. Reducing the driving power of an output pad reduces electromagnetic emissions (EME). In strong driver mode, selecting a slower edge reduces EME.

The dynamic behavior, i.e. the rise time and fall time, depends on the applied external capacitance that must be charged and discharged. Timing values are given for a capacitance of 20 pF, unless otherwise noted.

In general, the performance of a pad driver depends on the available supply voltage V_{DDP}. The following table lists the pad parameters.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Debug via JTAG

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply; C_L= 20 pF.

Table 40 JTAG Interface Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	50[1]	–	–	ns	[2]
TCK high time	t_2 SR	16	–	–	ns	
TCK low time	t_3 SR	16	–	–	ns	
TCK clock rise time	t_4 SR	–	–	8	ns	
TCK clock fall time	t_5 SR	–	–	8	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	
TDO valid from TCK falling edge (propagation delay)[3]	t_8 CC	–	25	29	ns	
TDO high impedance to valid output from TCK falling edge[4][3]	t_9 CC	–	25	29	ns	
TDO valid output to high impedance from TCK falling edge[3]	t_{10} CC	–	25	29	ns	
TDO hold after TCK falling edge[3]	t_{18} CC	5	–	–	ns	

1) The debug interface cannot operate faster than the overall system, therefore $t_1 \geq t_{SYS}$.
2) Under typical conditions, the interface can operate at transfer rates up to 20 MHz.
3) The falling edge on TCK is used to generate the TDO timing.
4) The setup time for TDO is given implicitly by the TCK cycle time.

5.3 Quality Declarations

The operation lifetime of the XC238xA depends on the applied temperature profile in the application. For a typical example, please refer to **Table 44**; for other profiles, please contact your Infineon counterpart to calculate the specific lifetime within your application.

Table 43 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation lifetime	t_{OP} CC	–	–	20	a	See **Table 44** and **Table 45**
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	–	–	2 000	V	EIA/JESD22-A114-B
Moisture sensitivity level	MSL CC	–	–	3	–	JEDEC J-STD-020C

Table 44 Typical Usage Temperature Profile

Operating Time (Sum = 20 years)	Operating Temperat.	Notes
1 200 h	T_J = 150°C	Normal operation
3 600 h	T_J = 125°C	Normal operation
7 200 h	T_J = 110°C	Normal operation
12 000 h	T_J = 100°C	Normal operation
7 × 21 600 h	T_J = 0…10°C, …, 60…70°C	Power reduction

Table 45 Long Time Storage Temperature Profile

Operating Time (Sum = 20 years)	Operating Temperat.	Notes
2 000 h	T_J = 150°C	Normal operation
16 000 h	T_J = 125°C	Normal operation
6 000 h	T_J = 110°C	Normal operation
151 200 h	$T_J \leq$ 150°C	No operation