
**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | - |
| Peripherals | POR, WDT |
| Number of I/O | 14 |
| Program Memory Size | 1KB (1K x 8) |
| Program Memory Type | ROM |
| EEPROM Size | - |
| RAM Size | 125 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 18-DIP (0.300", 7.62mm) |
| Supplier Device Package | 18-DIP |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z86l0408pscr5474 |

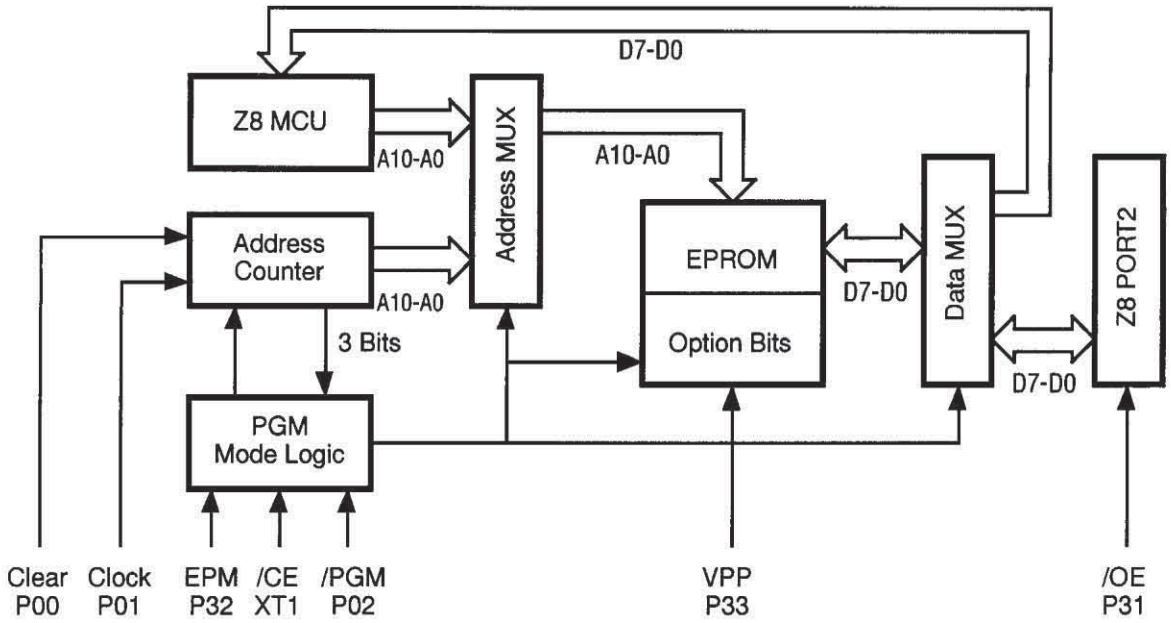



**Figure 2. EPROM Programming Mode Block Diagram**

## PIN DESCRIPTIONS

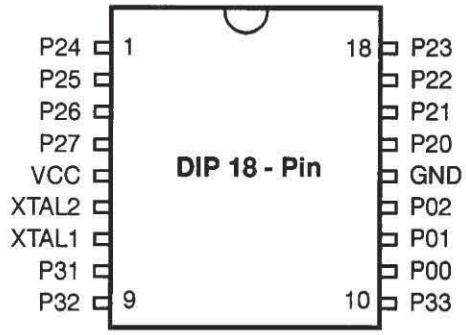



**Figure 3. 18-Pin Standard Mode Configuration**

**Table 1. 18-Pin Standard Mode Identification**

| Pin # | Symbol | Function | Direction |
|---|---|---|---|
| 1-4 | P24-P27 | Port 2, Pins 4, 5, 6, 7 | In/Output |
| 5 | $V_{CC}$ | Power Supply | |
| 6 | XTAL2 | Crystal Oscillator Clock | Output |
| 7 | XTAL1 | Crystal Oscillator Clock | Input |
| 8 | P31 | Port 3, Pin 1, AN1 | Input |
| 9 | P32 | Port 3, Pin 2, AN2 | Input |
| 10 | P33 | Port 3, Pin 3, REF | Input |
| 11-13 | P00-P02 | Port 0, Pins 0, 1, 2 | In/Output |
| 14 | GND | Ground | |
| 15-18 | P20-P23 | Port 2, Pins 0, 1, 2, 3 | In/Output |

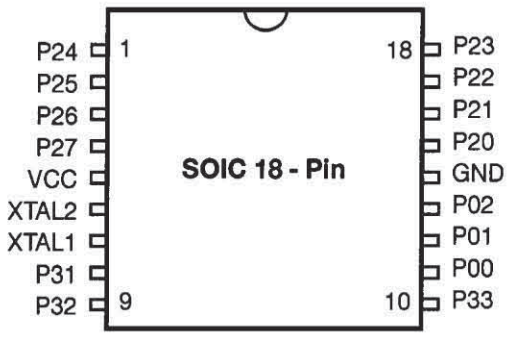



**Figure 4. 18-Pin SOIC Configuration**

**Table 2. 18-Pin SOIC Pin Identification**

| Pin # | Symbol | Function | Direction |
|---|---|---|---|
| 1-4 | P24-P27 | Port 2, Pins 4,5,6,7 | In/Output |
| 5 | $V_{CC}$ | Power Supply | |
| 6 | XTAL2 | Crystal Osc. Clock | Output |
| 7 | XTAL1 | Crystal Osc. Clock | Input |
| 8 | P31 | Port 3, Pin 1, AN1 | Input |
| 9 | P32 | Port 3, Pin 2, AN2 | Input |
| 10 | P33 | Port 3, Pin 3, REF | Input |
| 11-13 | P00-P02 | Port 0, Pins 0,1,2 | In/Output |
| 14 | GND | Ground | |
| 15-18 | P20-P23 | Port 2, Pins 0,1,2,3 | In/Output |

## DC CHARACTERISTICS

Z86L04/L08

| Sym. | Parameter | $V_{CC}$ [3] | $T_A$ = 0 °C to +70 °C Min | Max | Typical @ 25 °C | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| $V_{CH}$ | Clock Input High Voltage | 2.0V | 0.9 $V_{CC}$ | $V_{CC}$+0.3 | | V | Driven by External Clock Generator | |
| | | 3.9V | 0.9 $V_{CC}$ | $V_{CC}$+0.3 | | V | Driven by External Clock Generator | |
| $V_{CL}$ | Clock Input Low Voltage | 2.0V | $V_{SS}$–0.3 | 0.1 $V_{CC}$ | | V | Driven by External Clock Generator | |
| | | 3.9V | $V_{SS}$–0.3 | 0.1 $V_{CC}$ | | V | Driven by External Clock Generator | |
| $V_{IH}$ | Input High Voltage | 2.0V | 0.9 $V_{CC}$ | $V_{CC}$+0.3 | | V | | 1 |
| | | 3.9V | 0.9 $V_{CC}$ | $V_{CC}$+0.3 | | V | | 1 |
| $V_{IL}$ | Input Low Voltage | 2.0V | $V_{SS}$–0.3 | 0.1 $V_{CC}$ | | V | | 1 |
| | | 3.9V | $V_{SS}$–0.3 | 0.1 $V_{CC}$ | | V | | 1 |
| $V_{OH}$ | Output High Voltage | 2.0V | $V_{CC}$–0.4 | | 3.0 | V | $I_{OH}$ = – 500 µA | 4,5 |
| | | 3.9V | $V_{CC}$–0.4 | | 3.0 | V | $I_{OH}$ = – 500 µA | 4,5 |
| $V_{OL1}$ | Output Low Voltage | 2.0V | | 0.8 | 0.2 | V | $I_{OL}$ = +1.0 mA | 4,5 |
| | | 3.9V | | 0.4 | 0.1 | V | $I_{OL}$ = +1.0 mA | 4,5 |
| $V_{OL2}$ | Output Low Voltage | 2.0V | | 1.0 | 0.8 | V | $I_{OL}$ = + 3.0 mA | 4,5 |
| | | 3.9V | | 0.8 | 0.3 | V | $I_{OL}$ = + 3.0 mA | 4,5 |
| $V_{OFFSET}$ | Comparator Input Offset Voltage | 2.0V | | 25 | 10 | mV | | |
| | | 3.9V | | 25 | 10 | mV | | |
| $V_{LV}$ | $V_{CC}$ Low Voltage Auto Reset | | | 2.15 | | V | | |
| $I_{IL}$ | Input Leakage (Input Bias Current of Comparator) | 2.0V | –1.0 | 1.0 | | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| | | 3.9V | –1.0 | 1.0 | | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| $I_{OL}$ | Output Leakage | 2.0V | –1.0 | 1.0 | | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| | | 3.9V | –1.0 | 1.0 | | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| $V_{ICR}$ | Comparator Input Common Mode Voltage Range | 2.0<br>3.9 | 0<br>0 | $V_{CC}$ –1.0<br>$V_{CC}$ –1.0 | | V<br>V | | |

| Sym | Parameter | $V_{CC}$ [3] | $T_A$ = 0 °C to +70 °C Min | Max | Typical @ 25 °C | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Supply Current | 2.0V | | 3.3 | | mA | @ 2 MHz | 5,6 |
| | | 3.9V | | 6.8 | | mA | @ 2 MHz | 5,6 |
| | | 2.0V | | 6.0 | | mA | @ 8 MHz | 5,6 |
| | | 3.9V | | 9.0 | | mA | @ 8 MHz | 5,6 |
| $I_{CC1}$ | Standby Current (Halt Mode) | 2.0V | | 2.3 | | mA | @ 2 MHz | 5,6,7 |
| | | 3.9V | | 3.8 | | mA | @ 2 MHz | 5,6,7 |
| | | 2.0V | | 3.8 | | mA | @ 8 MHz | 5,6,7 |
| | | 3.9V | | 4.8 | | mA | @ 8 MHz | 5,6,7 |
| $I_{CC2}$ | Standby Current (Stop Mode) | 2.0V | | 10 | 1.0 | µA | | 6,7 |
| | | 3.9V | | 10 | 1.0 | µA | | 6,7 |
| $I_{ALL}$ | Auto Latch Low Current | 2.0V | | 12 | 3.0 | µA | $0V < V_{IN} < V_{CC}$ | |
| | | 3.9V | | 32 | 16 | µA | $0V < V_{IN} < V_{CC}$ | |
| $I_{ALH}$ | Auto Latch High Current | 2.0V | | –8 | -1.5 | µA | $0V < V_{IN} < V_{CC}$ | |
| | | 3.9V | | –16 | -8.0 | µA | | |

**Notes:**

1. Port 0, 2, and 3 only.
2. $V_{SS}$ = 0V = GND. The device operates down to $V_{LV}$. The minimum operational $V_{CC}$ is determined by the value of the voltage $V_{LV}$ at the ambient temperature.
3. $V_{CC}$ = 2.0V to 3.9V, typical values measured at $V_{CC}$ = 3.3 V.
4. Standard Mode (not Low EMI mode).
5. Inputs at $V_{CC}$ or $V_{SS}$, outputs are unloaded.
6. WDT is not running.
7. Comparator inputs at $V_{CC}$.

## AC ELECTRICAL CHARACTERISTICS

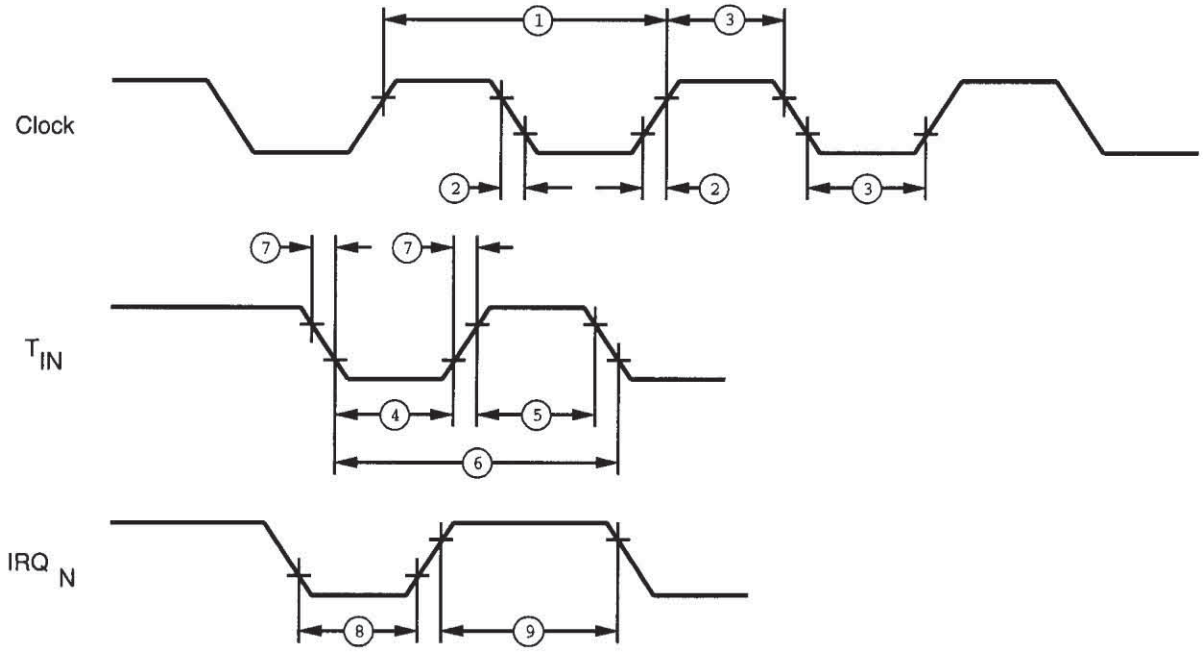



**Figure 6. AC Electrical Timing Diagram**

## AC ELECTRICAL CHARACTERISTICS

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)

| | | | | $T_A$= 0 °C to +70 °C 8 MHz | | | |
|---|---|---|---|---|---|---|---|
| No. | Symbol | Parameter | $V_{CC}$ | Min | Max | Units | Notes |
| 1 | TpC | Input Clock Period | 2.0V | 125 | DC | ns | 1 |
| | | | 3.9V | 125 | DC | ns | 1 |
| 2 | TrC,TfC | Clock Input Rise and Fall Times | 2.0V | | 25 | ns | 1 |
| | | | 3.9V | | 25 | ns | 1 |
| 3 | TwC | Input Clock Width | 2.0V | 62 | | ns | 1 |
| | | | 3.9V | 62 | | ns | 1 |
| 4 | TwTinL | Timer Input Low Width | 2.0V | 70 | | ns | 1 |
| | | | .39V | 70 | | ns | 1 |
| 5 | TwTinH | Timer Input High Width | 2.0V | 5TpC | | | 1 |
| | | | 3.9V | 5TpC | | | 1 |
| 6 | TpTin | Timer Input Period | 2.0V | 8TpC | | | 1 |
| | | | 3.9V | 8TpC | | | 1 |
| 7 | TrTin, TtTin | Timer Input Rise and Fall Time | 2.0V | | 100 | ns | 1 |
| | | | 3.9V | | 100 | ns | 1 |
| 8 | TwIL | Int. Request Input Low Time | 2.0V | 70 | | ns | 1,2,3 |
| | | | 3.9V | 70 | | ns | 1,2,3 |
| 9 | TwIH | Int. Request Input High Time | 3.0V | 5TpC | | | 1,2,3 |
| | | | 3.9V | 5TpC | | | 1,2,3 |
| 10 | Twdt | Watch-Dog Timer Delay Time Before Time-Out | 2.0V | 25 | | ms | |
| | | | 3.9V | 10 | | ms | |
| 11 | Tpor | Power-On Reset Time | 2.0V | 70 | | ms | 4 |
| | | | 3.9V | 50 | | ms | 4 |
| | | | 2.0V | 20 | | ms | 5 |
| | | | 3.9V | 6 | | ms | 5 |

**Notes:**

1. Timing Reference uses 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0.
2. Interrupt request through Port 3 (P33-P31).
3. IRQ 0,1,2 only.
4. For Z86L08 using internal RC oscillator.
5. For Z86L04 using internal RC oscillator.

**Precaution**: Maximum frequency in Low EMI mode is 1 MHz.

## PIN FUNCTIONS

**XTAL1, XTAL2** Crystal In, Crystal Out (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, RC, or an external single-phase clock (8 MHz max) to the on-chip clock oscillator and buffer.

**Port 0, P02-P00.** Port 0 is a 3-bit bidirectional, Schmitt-triggered CMOS compatible I/O port. These three I/O lines can be globally configured under software control to be inputs or outputs (Figure 7).

**Auto Latch.** The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. On Power-up and Reset, the Auto Latch will set the ports to an undetermined state of 0 or 1. Default condition is Auto Latches enabled.

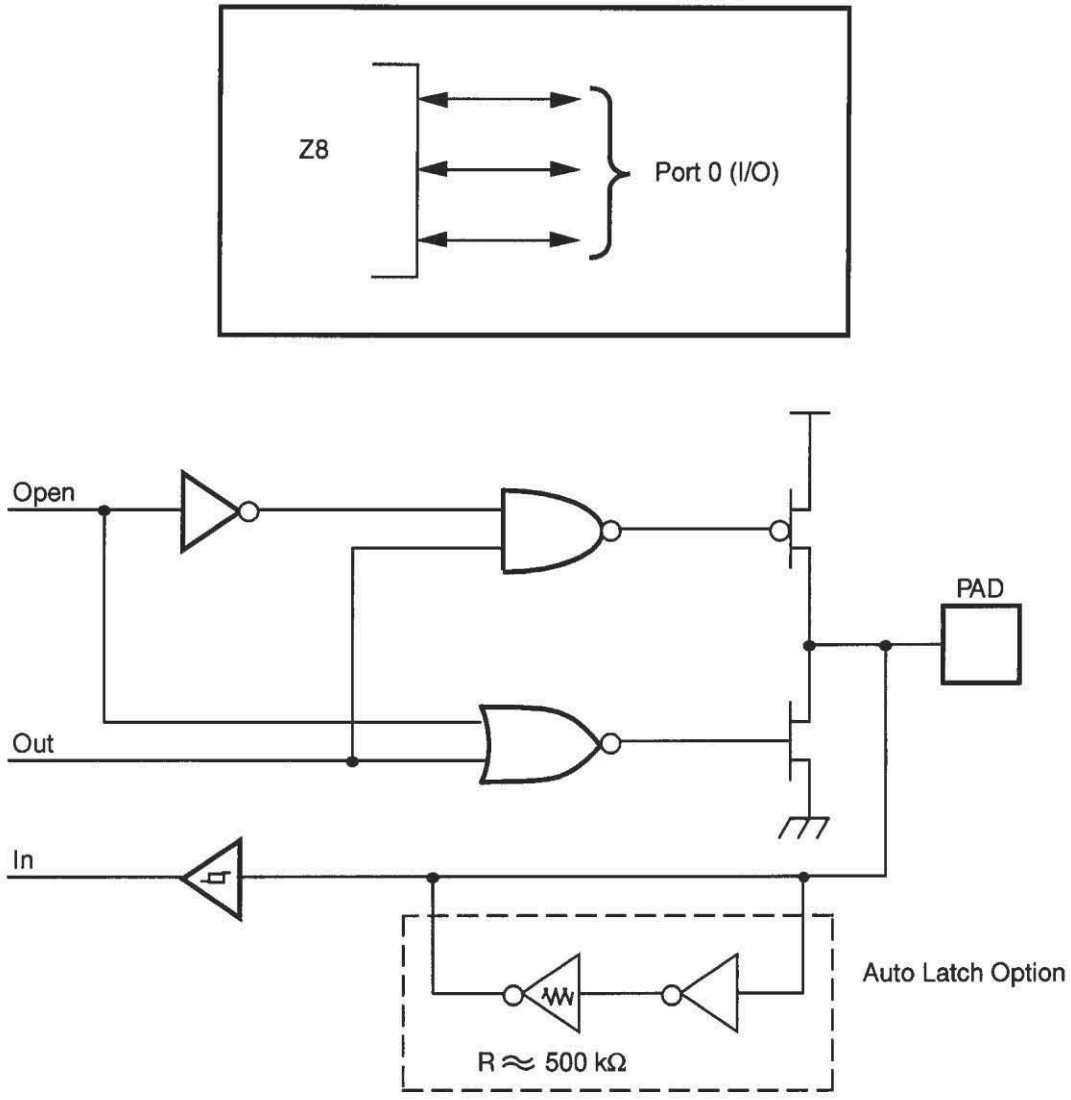



**Figure 7. Port 0 Configuration**

**Port 2, P27-P20.** Port 2 is an 8-bit, bit-programmable, bidirectional, Schmitt-triggered, CMOS, compatible I/O port. These eight I/O lines can be configured under software control to be inputs or outputs, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain (Figure 8).

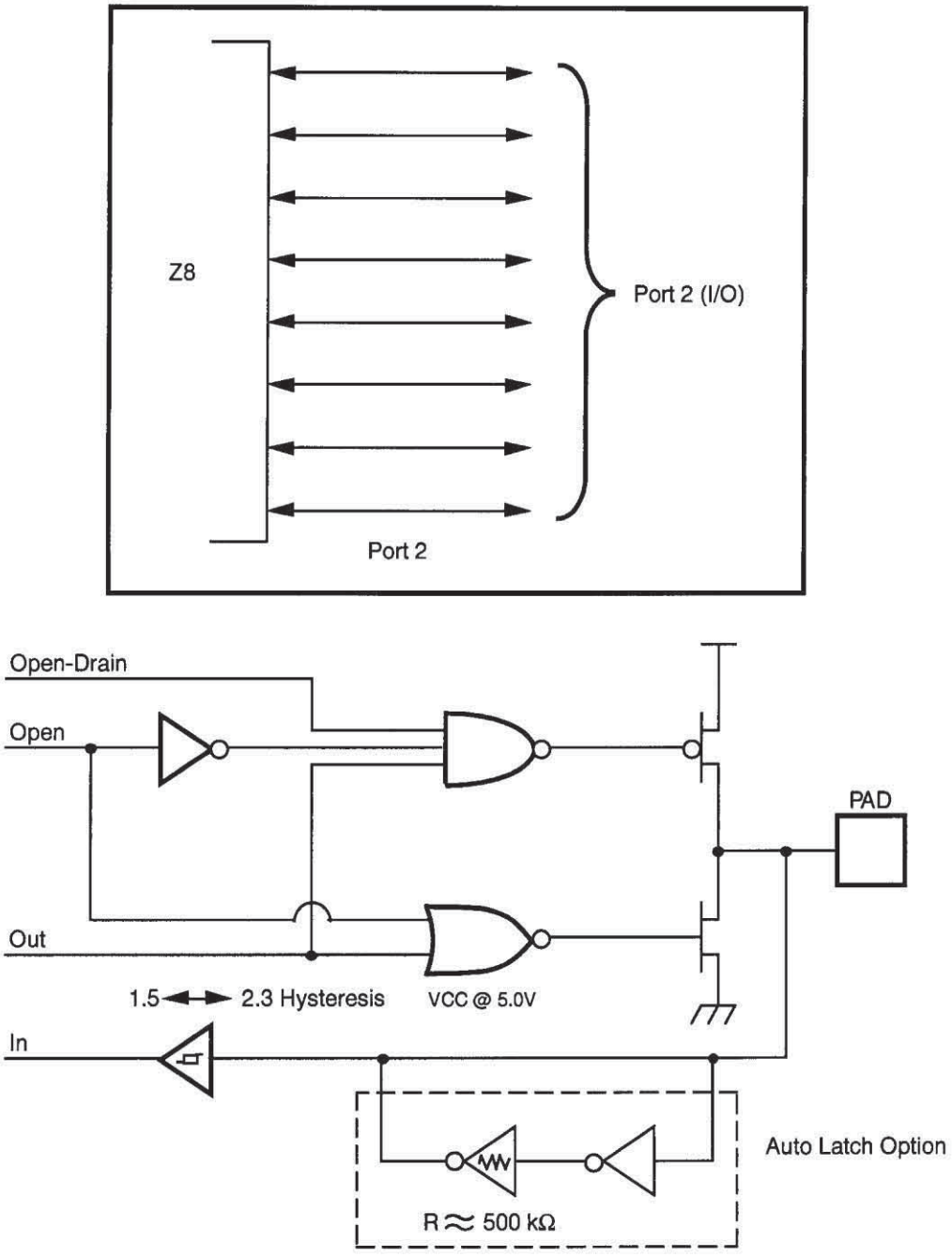



**Figure 8. Port 2 Configuration**

## PIN FUNCTIONS (Continued)

**Port 3, P33-P31.** Port 3 is a 3-bit, CMOS, compatible port with three fixed input (P33-P31) lines. These three input lines can be configured under software control as digital Schmitt-trigger inputs or analog inputs.

These three input lines are also used as the interrupt sources IRQ0-IRQ3 and as the timer input signal $T_{IN}$ (Figure 9).

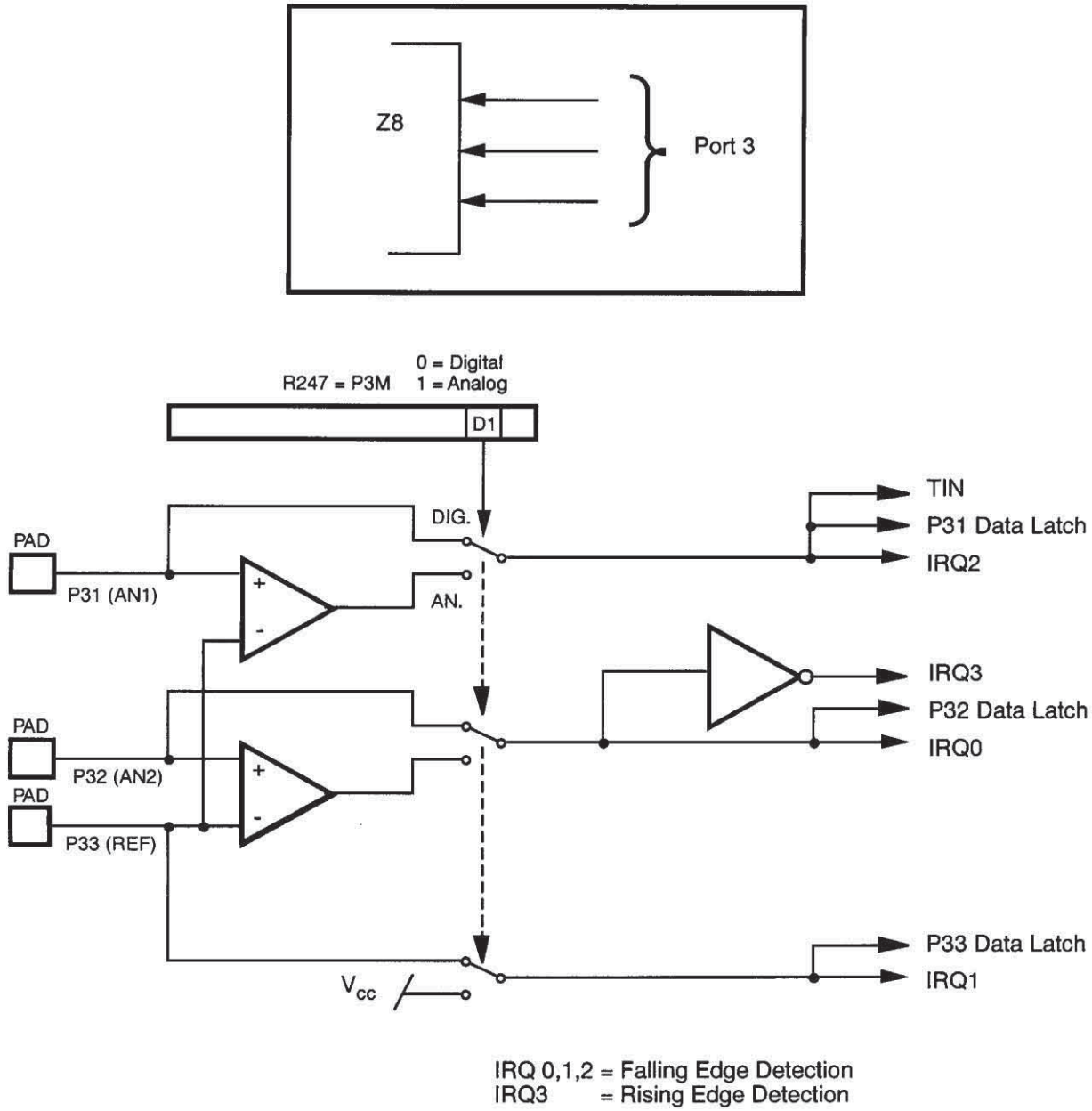



**Figure 9. Port 3 Configuration**

**Comparator Inputs.** Two analog comparators are added to input of Port 3, P31 and P32, for interface flexibility. The comparators reference voltage P33 (REF) is common to both comparators.

Typical applications for the on-board comparators; Zero crossing detection, A/D conversion, voltage scaling, and threshold detection. In analog mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP mode. The common voltage range is 0-4V when the $V_{CC}$ is 5.0V; the power supply and common mode rejection ratios are 90 dB and 60 dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output is used for interrupt generation, Port 3 data inputs, or $T_{IN}$ through P31. Alternatively, the comparators can be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

## FUNCTIONAL DESCRIPTION

The following special functions have been incorporated into the Z86L04/L08 devices to enhance the standard Z8 core architecture to provide the user with increased design flexibility.

**RESET.** This function is accomplished by means of a Power-On Reset or a Watch-Dog Timer Reset. Upon power-up, the Power-On Reset circuit waits for $T_{POR}$ ms, plus 18 clock cycles, then starts program execution at address 000C (Hex) (Figure 10). The control registers' reset values are shown in Table 3.

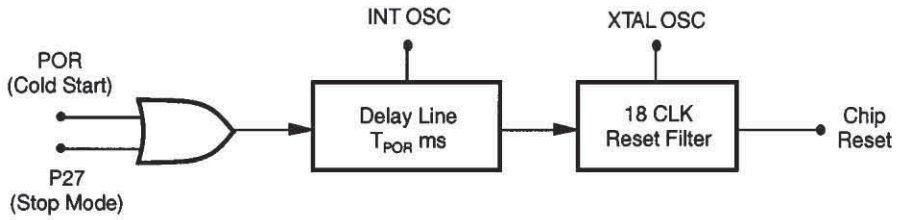



**Figure 10. Internal Reset Configuration**

**Power-On Reset (POR).** A timer circuit clocked by a dedicated on-board RC oscillator is used for a POR timer function. The POR time allows $V_{CC}$ and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the five following conditions:

- Power bad to power good status
- Stop-Mode Recovery
- WDT time-out
- WDT time-out (in HALT Mode)
- WDT time-out (in STOP Mode)

**Watch-Dog Timer Reset.** The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and is retriggered on subsequent execution of the WDT instruction. The timer circuit is driven by an on-board RC oscillator. If the permanent WDT option is selected then the WDT is enabled after reset and operates in RUN Mode, HALT mode, STOP mode and cannot be disabled. If the permanent WDT option is not selected then the WDT, when enabled by the user's software, does not operate in STOP Mode, but it can operate in HALT Mode by using a WDH instruction.

**Table 3. Control Register Reset Values**

| | | Reset Condition | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Addr** | **Reg.** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **Comments** |
| FF | SPL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| FE | GPR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| FD | RP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| FC | FLAGS | U | U | U | U | U | U | U | U | |
| FB | IMR | 0 | U | U | U | U | U | U | U | |
| FA | IRQ | U | U | 0 | 0 | 0 | 0 | 0 | 0 | IRQ3 is used for positive edge detection |
| F9 | IPR | U | U | U | U | U | U | U | U | |
| F8* | P01M | U | U | U | 0 | U | U | 0 | 1 | |
| F7* | P3M | U | U | U | U | U | U | 0 | 0 | P2 open-drain |
| F6* | P2M | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Inputs after reset |
| F5 | PRE0 | U | U | U | U | U | U | U | 0 | |
| F4 | T0 | U | U | U | U | U | U | U | U | |
| F3 | PRE1 | U | U | U | U | U | U | 0 | 0 | |
| F2 | T1 | U | U | U | U | U | U | U | U | |
| F1 | TMR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

**Notes:**
*Registers are not reset after a STOP-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be reconfigured as shown in Table 4 and the user must avoid bus contention on the port pins or it may affect device reliability.

**Program Memory.** The Z8 addresses up to 1024,2048 bytes of internal program memory (Figure 11). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0-1023/0-2047 are on-chip mask programmable ROM.

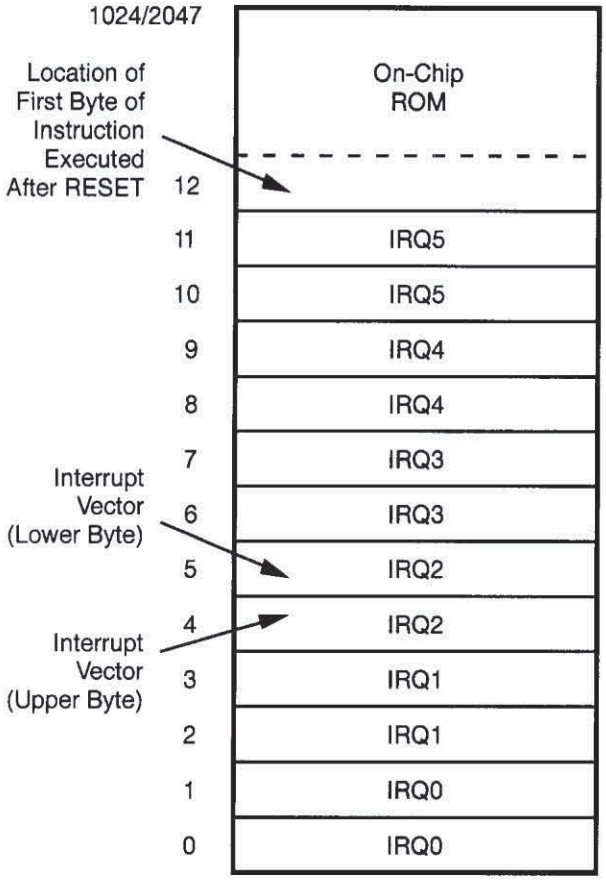



**Figure 11. Program Memory Map**

**Register File.** The Register File consists of three I/O port registers, 61 general-purpose registers, and 12 control and status registers R0-R3, R4-R127 and R241-R255, respectively (Figure 12). General-purpose registers occupy the 04H to 7FH address space. I/O ports are mapped as per the existing CMOS Z8. The instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 13) addresses the starting location of the active working-register group.

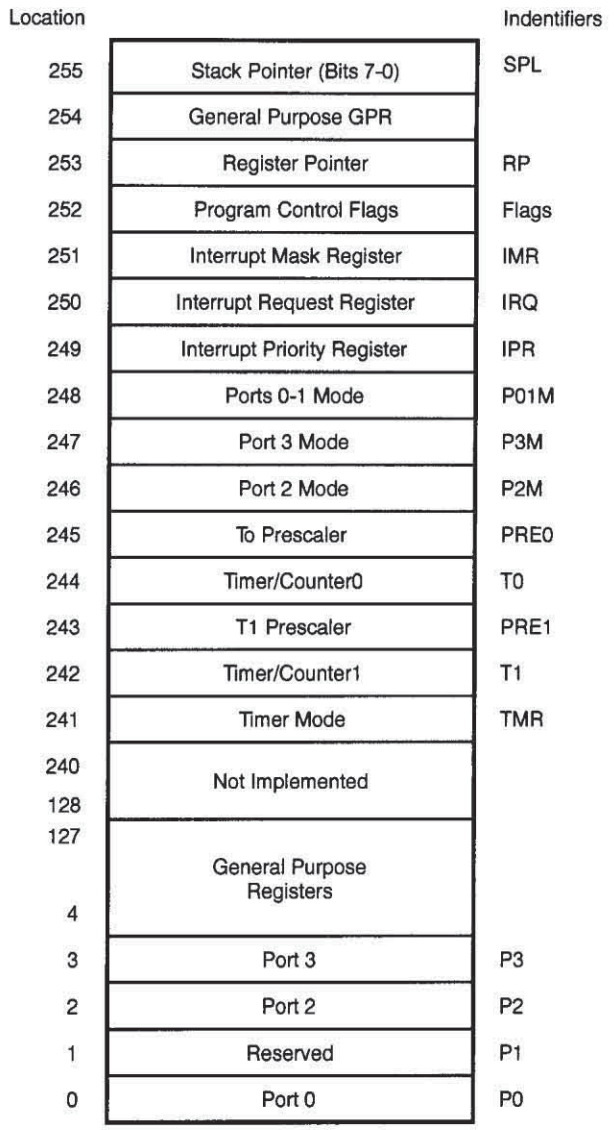



**Figure 12. Register File**

## FUNCTIONAL DESCRIPTION (Continued)

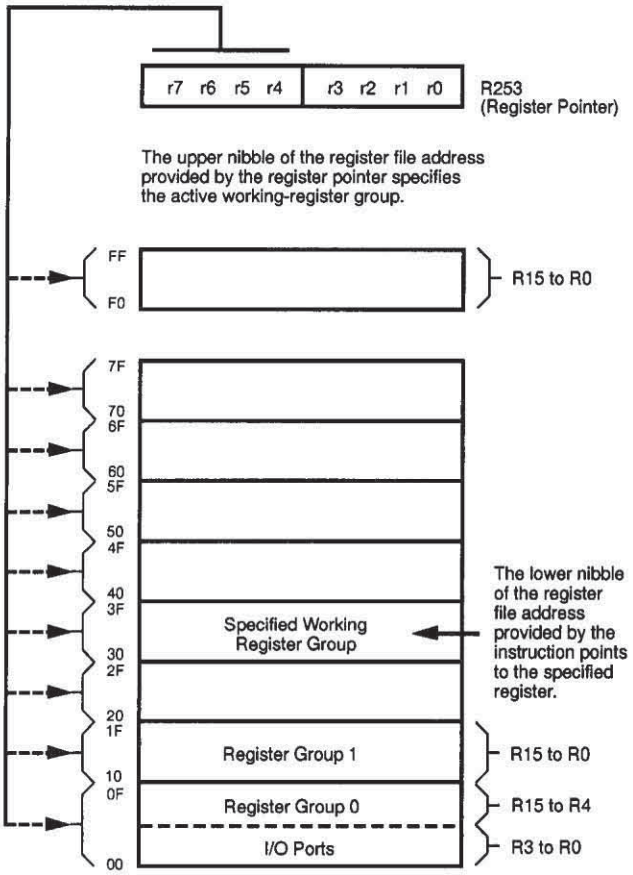



**Figure 13. Register Pointer**

**Stack Pointer.** The Z8 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 60 general-purpose registers. It is set to 00Hex after any reset.

**General-Purpose Registers (GPR).** These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the $V_{CC}$ voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register. But is set to 00Hex after any reset.

**Counter/Timer.** There are two 8-bit programmable counter/timers (T0 and T1), each driven by its 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources. (Figure 14).

The 6-bit prescaler divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ5 (T1 or IRQ4 (T0) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (Single-Pass mode) or to automatically reload the initial value and continue counting (Modulo-N Continuous Mode).

The counters, but not the prescaler, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or used as a gate input for the internal clock.

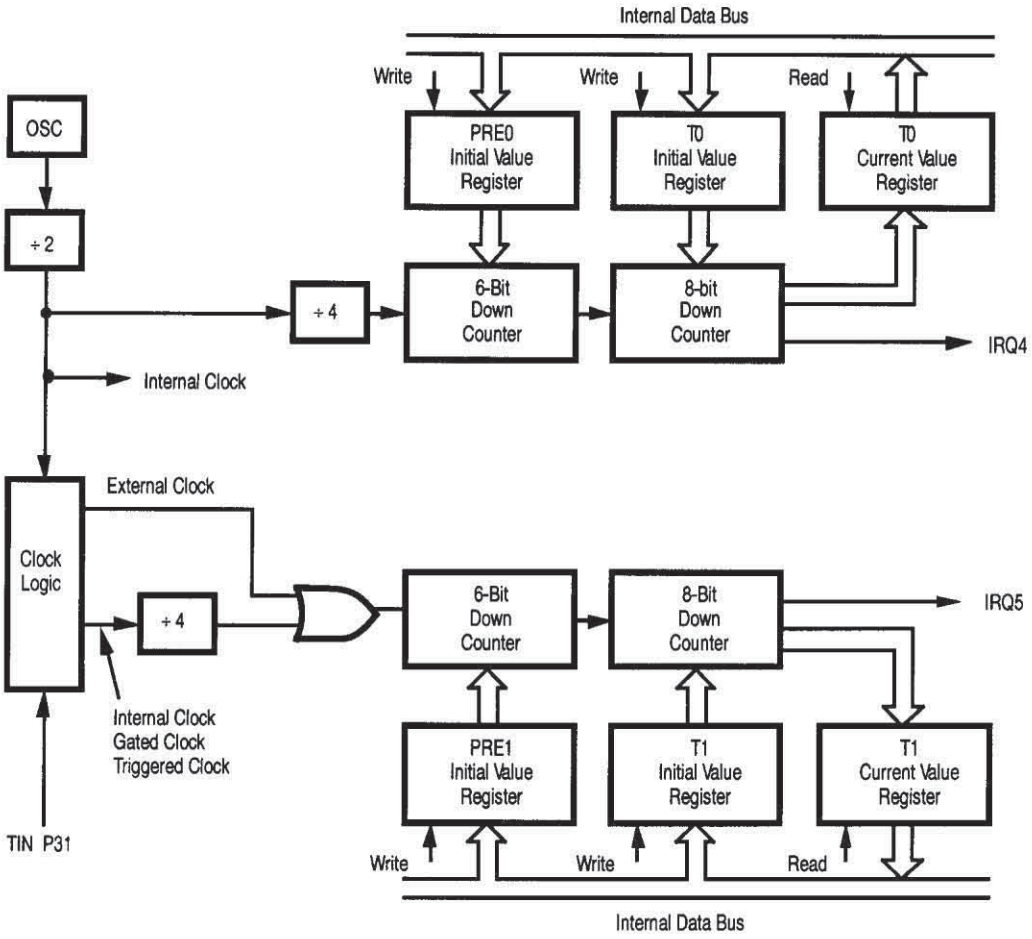



**Figure 14. Counter/Timers Block Diagram**

## FUNCTIONAL DESCRIPTION (Continued)

**Interrupts.** The Z8 has five interrupts from four different sources. These interrupts are maskable and prioritized (Figure 15). The sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and one counter/timer. The Interrupt Mask Register globally or individually enables or disables the five interrupt requests (Table 4).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an Interrupt Request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

User must select any Z86E08 mode in Zilog's C12 ICE-BOX™ emulator. The rising edge interrupt is not directly supported on the Z86CCP00ZEM emulator.

**Table 4. Interrupt Types, Sources, and Vectors**

| Name | Source | Vector Location | Comments |
|---|---|---|---|
| IRQ0 | AN2(P32) | 0,1 | External (F)Edge |
| IRQ1 | REF(P33) | 2,3 | External (F)Edge |
| IRQ2 | AN1(P31) | 4,5 | External (F)Edge |
| IRQ3 | AN2(P32) | 6,7 | External (R)Edge |
| IRQ4 | T0 | 8,9 | Internal |
| IRQ5 | T1 | 10,11 | Internal |

**Note:**
F = Falling edge triggered
R = Rising edge triggered

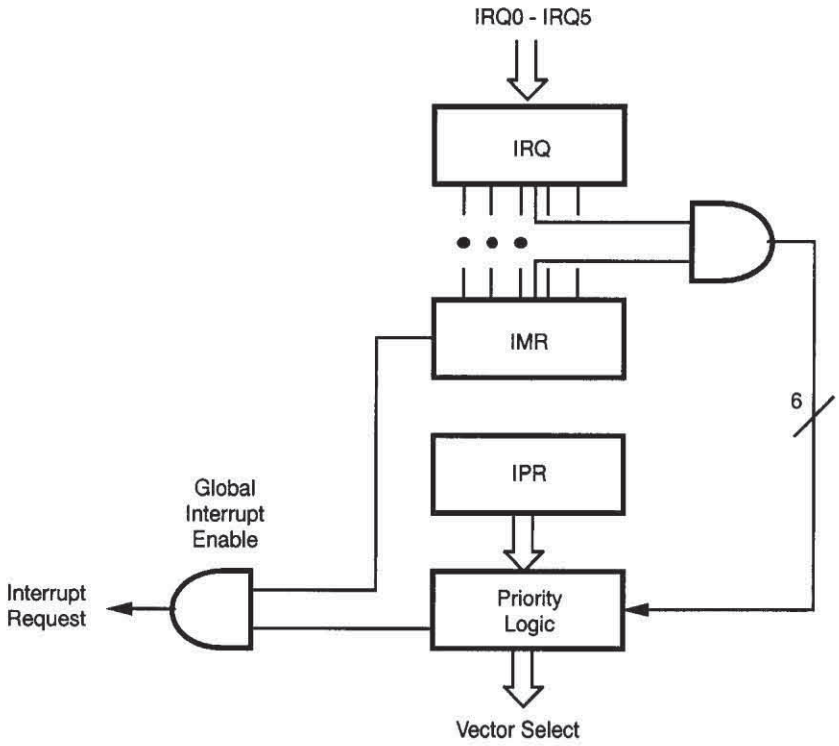
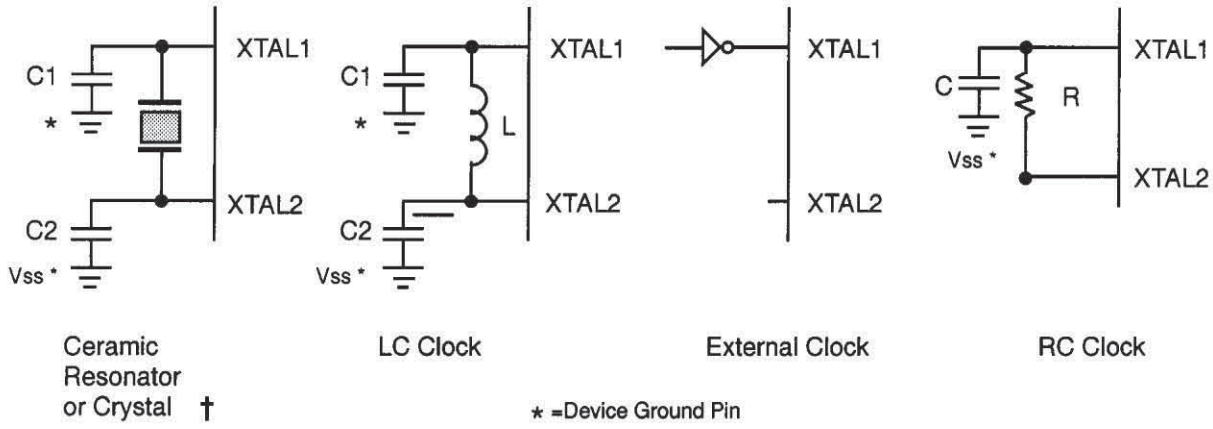



**Figure 15. Interrupt Block Diagram**

**Clock.** The Z8 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = INPUT, XTAL2 = OUTPUT). The crystal should be AT cut, 8 MHz max, with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal or ceramic resonator should be connected across XTAL1 and XTAL2 using the vendors crystal or ceramic resonator recommended capacitors from each pin directly to device ground pin 14 (Figure 16). Note that the crystal capacitor loads should be connected to $V_{SS}$, Pin 14 to reduce Ground noise injection.




† **Note:** If 32 KHz oscillator is selected then an external 10 Megohm resistor must be connected between XTAL1 and XTAL2 pins.

**Figure 16. Oscillator Configuration**

## Z8 CONTROL REGISTERS

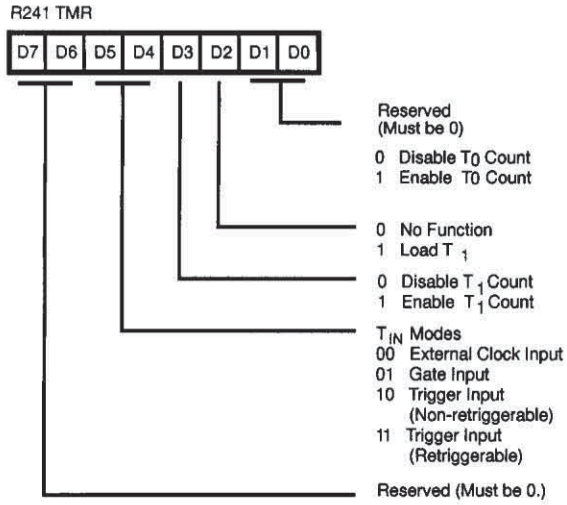



**Figure 18. Timer Mode Register ($F1_H$: Read/Write)**

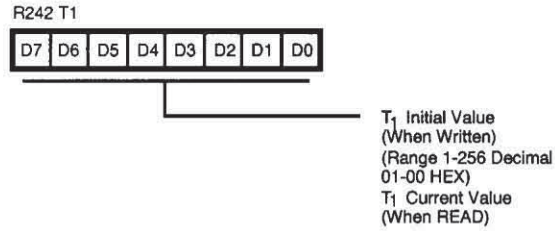



**Figure 19. Counter Timer 1 Register ($f2_H$:Read/Write)**

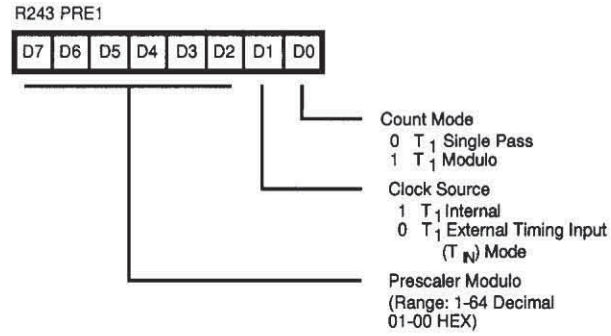



**Figure 20. Prescaler1 Register ($F3_H$: Write Only)**

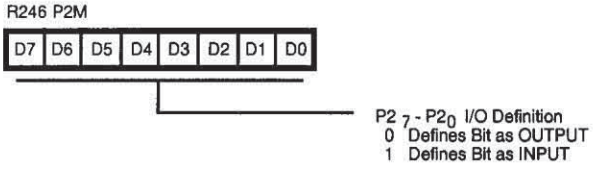



**Figure 21. Port 2 Mode Register ($F6_H$: Write Only)**

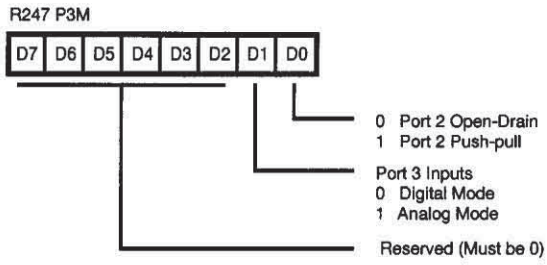



**Figure 22. Port 3 Mode Register ($F7_H$: Write Only)**

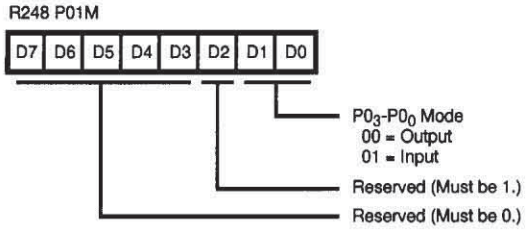



**Figure 23. Port 0 and 1 Mode Register ($F8_H$: Write Only)**

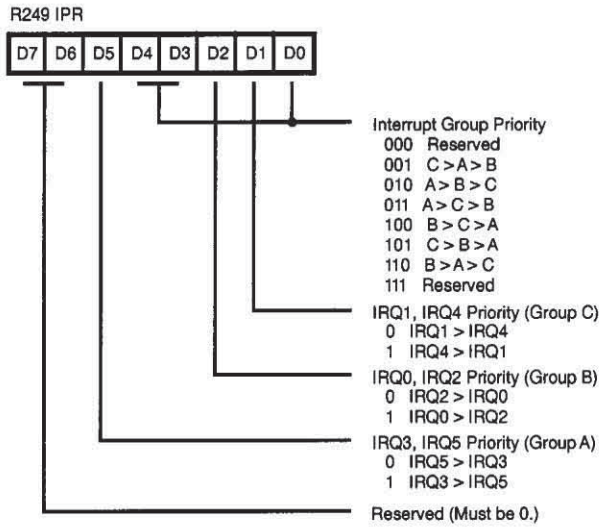
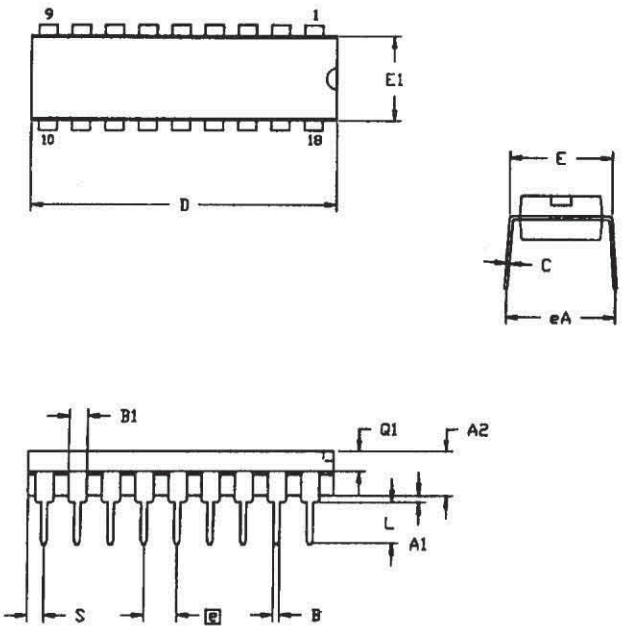



**Figure 24. Interrupt Priority Register ($F9_H$: Write Only)**

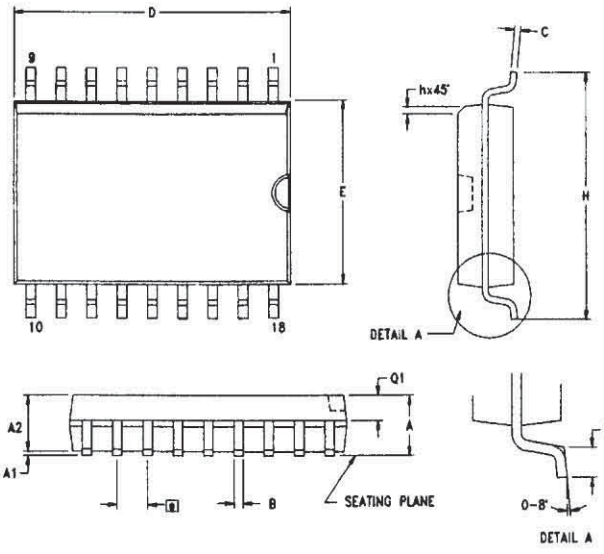
## PACKAGE INFORMATION




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A1 | 0.51 | 0.81 | .020 | .032 |
| A2 | 3.25 | 3.43 | .128 | .135 |
| B | 0.38 | 0.53 | .015 | .021 |
| B1 | 1.14 | 1.65 | .045 | .065 |
| C | 0.23 | 0.38 | .009 | .015 |
| D | 22.35 | 23.37 | .880 | .920 |
| E | 7.62 | 8.13 | .300 | .320 |
| E1 | 6.22 | 6.48 | .245 | .255 |
| e | 2.54 TYP | | .100 TYP | |
| eA | 7.87 | 8.89 | .310 | .350 |
| L | 3.18 | 3.81 | .125 | .150 |
| Q1 | 1.52 | 1.65 | .060 | .065 |
| S | 0.89 | 1.65 | .035 | .065 |

CONTROLLING DIMENSIONS : INCH

**Figure 30. 18-Pin DIP Package Diagram**




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 2.40 | 2.65 | 0.094 | 0.104 |
| A1 | 0.10 | 0.30 | 0.004 | 0.012 |
| A2 | 2.24 | 2.44 | 0.088 | 0.096 |
| B | 0.36 | 0.46 | 0.014 | 0.018 |
| C | 0.23 | 0.30 | 0.009 | 0.012 |
| D | 11.40 | 11.75 | 0.449 | 0.463 |
| E | 7.40 | 7.60 | 0.291 | 0.299 |
| e | 1.27 TYP | | 0.050 TYP | |
| H | 10.00 | 10.65 | 0.394 | 0.419 |
| h | 0.30 | 0.50 | 0.012 | 0.020 |
| L | 0.60 | 1.00 | 0.024 | 0.039 |
| Q1 | 0.97 | 1.07 | 0.038 | 0.042 |

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

**Figure 31. 18-Pin SOIC Package Diagram**

## ORDERING INFORMATION

**Standard Temperature**

| 18-Pin DIP | 18-Pin SOIC |
|---|---|
| Z86L0408PSC | Z86L0408SSC |
| Z86L0808PSC | Z86L0808SSC |

For fast results, contact your local Zilog sales office for assistance in ordering the part(s) desired.

## CODES

### Preferred Package

P = Plastic DIP

### Longer Lead Time

S = SOIC

### Preferred Temperature

S = 0 °C to +70 °C

### Speed

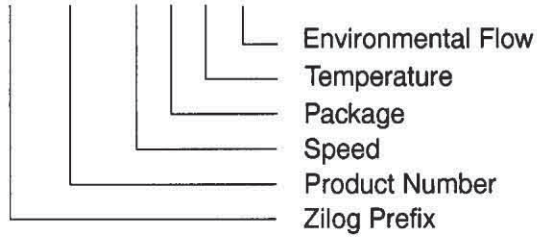
08 = 8 MHz

### Environmental

C = Plastic Standard

Example:

Z 86L08 08 P S C is a Z86L08, 08 MHz, Plastic DIP, 0 °C to +70 °C, Plastic Standard Flow



**Pre-Characterization Product:**

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

**Low Margin:**

Customer is advised that this product does not meet Zilog's internal guardbanded test policies for the specification requested and is supplied on an exception basis. Customer is cautioned that delivery may be uncertain and that, in addition to all other limitations on Zilog liability stated on the front and back of the acknowledgement, Zilog makes no claim as to quality and reliability under the CPS. The product remains subject to standard warranty for replacement due to defects in materials and workmanship.



Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
FAX 408 370-8056
Internet: http://www.zilog.com