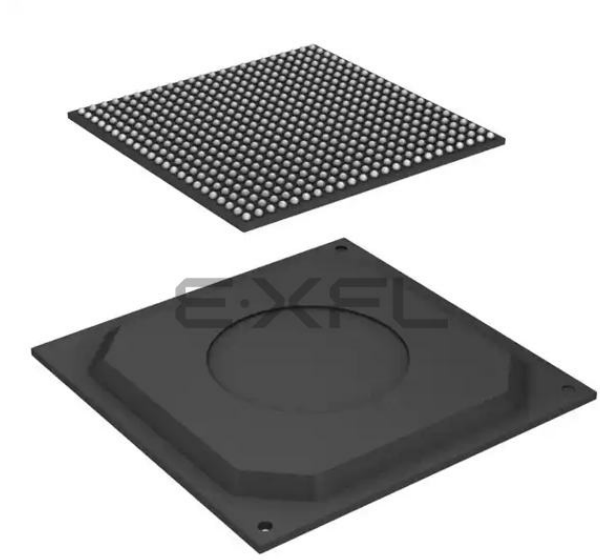

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR2, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	SATA 1.5Gbps (1)
USB	USB 2.0 (2), USB 2.0 + PHY (2)
Voltage - I/O	1.3V, 1.8V, 2.775V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	529-FBGA
Supplier Device Package	529-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx537cvv8b

- Multilevel memory system—The multilevel memory system of the i.MX53 is based on the L1 instruction and data caches, L2 cache, internal and external memory. The i.MX53 supports many types of external memory devices, including DDR2, low voltage DDR2, LPDDR2, DDR3, NOR Flash, PSRAM, cellular RAM, NAND Flash (MLC and SLC), OneNAND™, and managed NAND including eMMC up to rev 4.4.
- Smart speed technology—The i.MX53 device has power management throughout the IC that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product requiring levels of power far lower than industry expectations.
- Multimedia powerhouse—The multimedia performance of the i.MX53 processor ARM core is boosted by a multilevel cache system, Neon (including advanced SIMD, 32-bit single-precision floating point support) and vector floating point coprocessors. The system is further enhanced by a multi-standard hardware video codec, autonomous image processing unit (IPU), and a programmable smart DMA (SDMA) controller.
- Powerful graphics acceleration— The i.MX53 processors provide two independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator (33 Mtri/s, 200 Mpix/s, and 800 Mpix/s z-plane performance) and an OpenVG™ 1.1 2D graphics accelerator (200 Mpix/s).
- Interface flexibility—The i.MX53 processor supports connection to a variety of interfaces, including LCD controller for two displays and CMOS sensor interface, high-speed USB on-the-go with PHY, plus three high-speed USB hosts, multiple expansion card ports (high-speed MMC/SDIO host and others), 10/100 Ethernet controller, and a variety of other popular interfaces (PATA, UART, I^2C, and I^2S serial audio, among others).
- Advanced security—The i.MX53 processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. For detailed information about the i.MX53 security features contact a Freescale representative.

The i.MX53 application processor is a follow-on to the i.MX51, with improved performance, power efficiency, and multimedia capabilities.

1.1 Functional Part Differences and Ordering Information

shows the functional differences between the different parts in the i.MX53 family.

Table 1 provides ordering information.

Table 1. Ordering Information

Part Number	Mask Set	CPU Frequency	Notes	Package[1]
MCIMX537CVV8C	N78C	800 MHz	—	19 x 19 mm, 0.8 mm pitch BGA Case TEPBGA-2

[1] Case TEPBGA-2 is RoHS compliant, lead-free MSL (moisture sensitivity level) 3.

1.2 Features

The i.MX53 multimedia applications processor (AP) is based on the ARM Platform, which has the following features:

- MMU, L1 instruction and L1 data cache
- Unified L2 cache
- Maximum frequency of the core (including Neon, VFPv3 and L1 cache): 800 MHz
- Neon coprocessor (SIMD media processing architecture) and vector floating point (VFP-Lite) coprocessor supporting VFPv3
- TrustZone

The memory system consists of the following components:

- Level 1 cache:
  - — Instruction (32 Kbyte)
  - — Data (32 Kbyte)
- Level 2 cache:
  - — Unified instruction and data (256 Kbyte)
- Level 2 (internal) memory:
  - — Boot ROM, including HAB (64 Kbyte)
  - — Internal multimedia/shared, fast access RAM (128 Kbyte)
  - — Secure/non-secure RAM (16 Kbyte)
- External memory interfaces:
  - — 16/32-bit DDR2-800, LV-DDR2-800 or DDR3-800 up to 2 Gbyte
  - — 32-bit LPDDR2
  - — 8/16-bit NAND SLC/MLC Flash, up to 66 MHz, 4/8/14/16-bit ECC
  - — 8/16-bit NOR Flash, PSRAM, and cellular RAM.
  - — 32-bit multiplexed mode NOR Flash, PSRAM & cellular RAM.
  - — 8-bit Asynchronous (DTACK mode) EIM interface.
  - — All EIM pins are muxed on other interfaces (data with NFC pins). I/O muxing logic selects EIM port, as primary muxing at system boot.
  - — Samsung OneNAND™ and managed NAND including eMMC up to rev 4.4 (in muxed I/O mode)

The i.MX53 system is built around the following system on chip interfaces:

- 64-bit AMBA AXI v1.0 bus—used by ARM platform, multimedia accelerators (such as VPU, IPU, GPU3D, GPU2D) and the external memory controller (EXTMC) operating at 200 MHz.
- 32-bit AMBA AHB 2.0 bus—used by the rest of the bus master peripherals operating at 133 MHz.
- 32-bit IP bus—peripheral bus used for control (and slow data traffic) of the most system peripheral devices operating at 66 MHz.

3 Modules List

The i.MX53 processor contains a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX53 Digital and Analog Blocks

Block Mnemonic	Block Name	Subsystem	Brief Description
ARM	ARM Platform	ARM	The ARM Cortex™ A8 platform consists of the ARM processor version r2p5 (with TrustZone) and its essential sub-blocks. It contains the 32 Kbyte L1 instruction cache, 32 Kbyte L1 data cache, Level 2 cache controller and a 256 Kbyte L2 cache. The platform also contains an event monitor and debug modules. It also has a NEON coprocessor with SIMD media processing architecture, a register file with 32/64-bit general-purpose registers, an integer execute pipeline (ALU, Shift, MAC), dual single-precision floating point execute pipelines (FADD, FMUL), a load/store and permute pipeline and a non-pipelined vector floating point (VFP Lite) coprocessor supporting VFPv3.
ASRC	Asynchronous Sample Rate Converter	Multimedia Peripherals	The asynchronous sample rate converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120 dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs.
AUDMUX	Digital Audio Multiplexer	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports (three internal and four external) with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
CAMP-1 CAMP-2	Clock Amplifier	Clocks, Resets, and Power Control	Clock amplifier
CCM GPC SRC	Clock Control Module Global Power Controller System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, as well as for system power management. The system includes four PLLs.
CSPI ECSPI-1 ECSPI-2	Configurable SPI, Enhanced CSPI	Connectivity Peripherals	Full-duplex enhanced synchronous serial interface, with data rates 16-60 Mbit/s. It is configurable to support master/slave modes. In Master mode it supports four slave selects for multiple peripherals.
CSU	Central Security Unit	Security	The central security unit (CSU) is responsible for setting comprehensive security policy within the i.MX53 platform, and for sharing security information between the various security modules. The security control registers (SCR) of the CSU are set during boot time by the high assurance boot (HAB) code and are locked to prevent further writing.

Table 2. i.MX53 Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6 GPIO-7	General Purpose I/O Modules	System Control Peripherals	These modules are used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with a programmable prescaler and compare and capture register. A timer counter value can be captured using an external event, and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU3D	Graphics Processing Unit	Multimedia Peripherals	The GPU, version 3, provides hardware acceleration for 2D and 3D graphics algorithms with sufficient processor power to run desk-top quality interactive graphics applications on displays up to HD1080 resolution. It supports color representation up to 32 bits per pixel. GPU enables high-performance mobile 3D and 2D vector graphics at rates up to 33 Mtriangles/s, 200 Mpix/s, 800 Mpix/s (z).
GPU2D	Graphics Processing Unit-2D	Multimedia Peripherals	The GPU2D version 1, provides hardware acceleration for 2D graphic algorithms with sufficient processor power to run desk-top quality interactive graphics applications on displays up to HD1080 resolution.
I2C-1 I2C-2 I2C-3	I^2C Controller	Connectivity Peripherals	I^2C provides serial interface for controlling peripheral devices. Data rates of up to 400 kbps are supported.
IIM	IC Identification Module	Security	The IC identification module (IIM) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically programmable poly fuses (e-Fuses). The IIM also provides a set of volatile software-accessible signals that can be used for software control of hardware elements not requiring non-volatility. The IIM provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals requiring permanent non-volatility. The IIM also provides up to 28 volatile control signals. The IIM consists of a master controller, a software fuse value shadow cache, and a set of registers to hold the values of signals visible outside the module. IIM interfaces to the electrical fuse array (split to banks). Enabled to set up boot modes, security levels, security keys and many other system parameters. i.MX53A consists of 4 x 256-bit + 1 x 128-bit fuse-banks (total 1152 bits) through IIM interface.

Table 2. i.MX53 Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SECRAM	Secure / Non-secure RAM	Internal Memory	Secure / non-secure Internal RAM, controlled by SCC.
SJC	Secure JTAG Interface	System Control Peripherals	JTAG manipulation is a known hacker's method of executing unauthorized program code, getting control over secure applications, and running code in privileged modes. The JTAG port provides a debug access to several hardware blocks including the ARM processor and the system bus. The JTAG port must be accessible during platform initial laboratory bring-up, manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. However, in order to properly secure the system, unauthorized JTAG usage should be strictly forbidden. In order to prevent JTAG manipulation while allowing access for manufacturing tests and software debugging, the i.MX53 processor incorporates a mechanism for regulating JTAG access. SJC provides four different JTAG security modes that can be selected through an e-fuse configuration.
SPBA	Shared Peripheral Bus Arbiter	System Control Peripherals	SPBA (shared peripheral bus arbiter) is a two-to-one IP bus interface (IP bus) arbiter.
SPDIF	Sony Philips Digital Interface	Multimedia Peripherals	A standard digital audio transmission protocol developed jointly by the Sony and Philips corporations. Both transmitter and receiver functionalists are supported.
SRTC	Secure Real Time Clock	Security	The SRTC incorporates a special system state retention register (SSRR) that stores system parameters during system shutdown modes. This register and all SRTC counters are powered by dedicated supply rail NVCC_SRTC_POW. The NVCC_SRTC_POW can be energized separately even if all other supply rails are shut down. This register is helpful for storing warm boot parameters. The SSRR also stores the system security state. In case of a security violation, the SSRR mark the event (security violation indication).
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface used on the i.MX53A processor to provide connectivity with off-chip audio peripherals. The SSI interfaces connect internally to the AUDMUX for mapping to external ports. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock/frame sync options. Each SSI has two pairs of 8 x 24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream, which reduces CPU overhead in use cases where two time slots are being used simultaneously.

Table 2. i.MX53 Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
IPTP	IEEE1588 Precision Time Protocol	Connectivity Peripherals	The IEEE 1588-2002 (version 1) standard defines a precision time protocol (PTP) - which is a time-transfer protocol that enables synchronization of networks (for example, Ethernet), to a high degree of accuracy and precision. The IEEE1588 hardware assist is composed of the two blocks: time stamp unit and real time clock, which provide the timestamping protocol's functionality, generating and reading the needed timestamps. The hardware-assisted implementation delivers more precise clock synchronization at significantly lower CPU load compared to purely software implementations.
Temperature Monitor	(Part of SATA Block)	System Control Peripherals	The temperature sensor is an internal module to the i.MX53 that monitors the die temperature. The monitor is capable in generating SW interrupt, or trigger the CCM, to reduce the core operating frequency.
TVE	TV Encoder	Multimedia	The TV encoder, version 2.1 is implemented in conjunction with the image processing unit (IPU) allowing handheld devices to display captured still images and video directly on a TV or LCD projector. It supports composite PAL/NTSC, VGA, S-video, and component up to HD1080p analog video outputs.
TZIC	TrustZone Aware Interrupt Controller	ARM/Control	The TrustZone interrupt controller (TZIC) collects interrupt requests from all i.MX53 sources and routes them to the ARM core. Each interrupt can be configured as a normal or a secure interrupt. Software Force Registers and software Priority Masking are also supported.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	Each of the UART blocks supports the following serial data transmit/receive protocols and configurations: • 7 or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none) • Programmable bit-rates up to 4 Mbps. This is a higher max baud rate relative to the 1.875 Mbps, which is specified by the TIA/EIA-232-F standard. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USB	USB Controller	Connectivity Peripherals	USB supports USB2.0 480 MHz, and contains: • One high-speed OTG sub-block with integrated HS USB PHY • One high-speed host sub-block with integrated HS USB PHY • Two identical high-speed Host modules The high-speed OTG module, which is internally connected to the HS USB PHY, is equipped with transceiver-less logic to enable on-board USB connectivity without USB transceivers All the USB ports are equipped with standard digital interfaces (ULPI, HS IC-USB) and transceiver-less logic to enable onboard USB connectivity without USB transceivers.

3.1 Special Signal Considerations

The package contact assignments can be found in Section 6, "Package Information and Contact Assignments." Signal descriptions are defined in the i.MX53 Reference Manual. Special signal considerations information is contained in Chapter 1 of *i.MX53 System Development User's Guide* (MX53UG).

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX53 processor.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 3 for a quick reference to the individual tables and sections.

Table 3. i.MX53 Chip-Level Conditions

For these characteristics, …	Topic appears …
Absolute Maximum Ratings	Table 4 on page 16
TEPBGA-2 Package Thermal Resistance Data	Table 5 on page 17
i.MX53 Operating Ranges	Table 6 on page 18
External Clock Sources	Table 7 on page 20
Maximal Supply Currents	Table 8 on page 20
USB Interface Current Consumption	Table 9 on page 23

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under Table 4 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the Operating Ranges table is not implied.

Table 4. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Peripheral Core Supply Voltage	VCC	-0.3	1.35	V
ARM Core Supply Voltage	VDDGP	-0.3	1.4	V
Supply Voltage UHVIO	Supplies denoted as I/O Supply	-0.5	3.6	V
Supply Voltage for non UHVIO	Supplies denoted as I/O Supply	-0.5	3.3	V
USB VBUS	VBUS	—	5.25	V

4.1.6 USB-OH-3 (OTG + 3 Host ports) Module and the Two USB PHY (OTG and H1) Current Consumption

Table 9 shows the USB interface current consumption.

Table 9. USB Interface Current Consumption

Parameter	Conditions		Typical at 25 °C	Max	Unit
Analog Supply 3.3 V USB_H1_VDDA33 USB_OTG_VDDA33	Full Speed	RX	5.5	6	mA
		TX	7	8	
	High Speed	RX	5	6	
		TX	5	6	
Analog Supply 2.5 V USB_H1_VDDA25 USB_OTG_VDDA25	Full Speed	RX	6.5	7	mA
		TX	6.5	7	
	High Speed	RX	12	13	
		TX	21	22	
Digital Supply VCC (1.2 V)	Full Speed	RX	8	—	mA
		TX	8	—	
	High Speed	RX	8	—	
		TX	8	—	

4.2 Power Supply Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the i.MX53 processor (worst-case scenario)

4.2.1 Power-Up Sequence

The following observations should be considered:

- The consequent steps in power up sequence should not start before the previous step supplies have been stabilized within 90-110% of their nominal voltage, unless stated otherwise.
- NVCC_SRTC_POW should remain powered ON continuously, to maintain internal real-time clock status. Otherwise, it has to be powered ON together with VCC, or preceding VCC.
- The VCC should be powered ON together, or any time after NVCC_SRTC_POW.
- NVCC_CKIH should be powered ON after VCC is stable and before other I/O supplies (NVCC_xxx) are powered ON.

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output. The association is shown in Table 111.

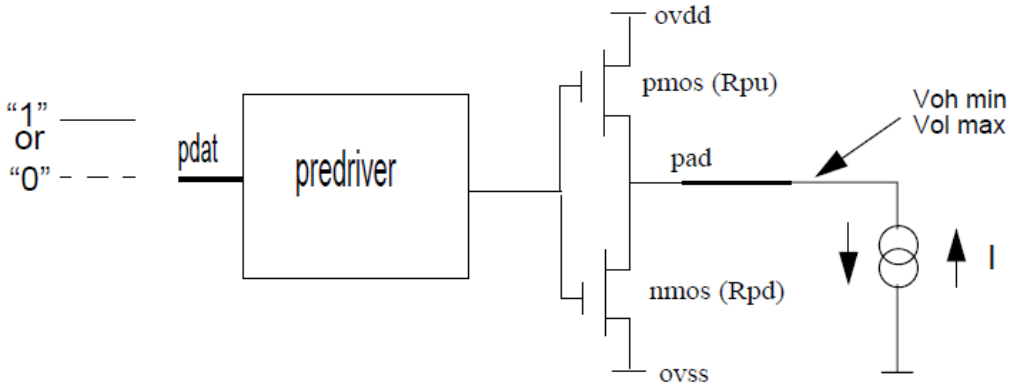


Figure 3. Circuit for Parameters Voh and Vol for I/O Cells

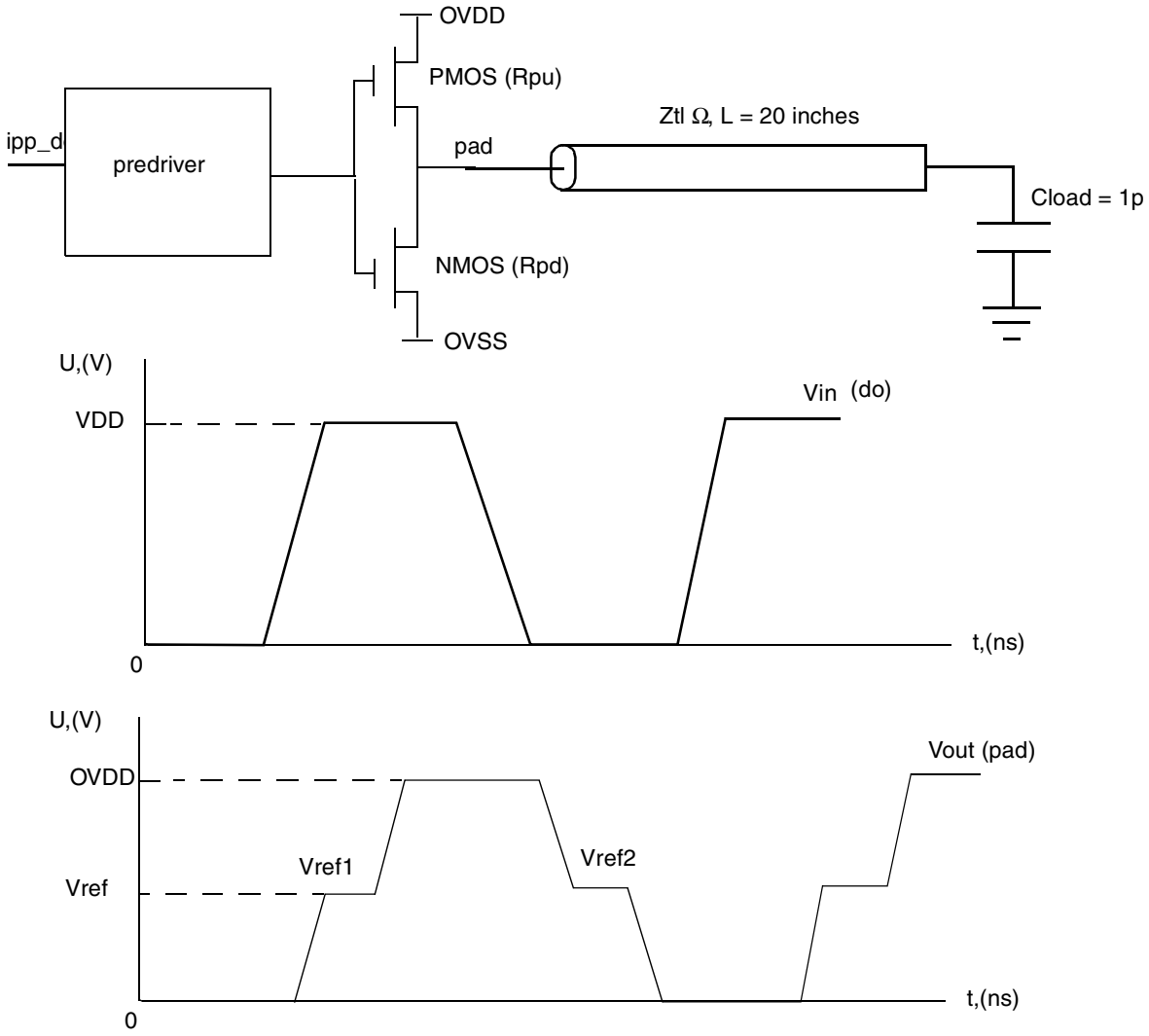
4.3.1 General Purpose I/O (GPIO) DC Parameters

The parameters in Table 10 are guaranteed per the operating ranges in Table 6, unless otherwise noted. Table 10 shows DC parameters for GPIO pads, operating at two supply ranges:

- 1.1 V to 1.3 V
- 1.65 V to 3.1 V

Table 10. GPIO I/O DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High-level output voltage[1]	Voh	Iout = -0.8 mA	OVDD - 0.15	—	—	V
Low-level output voltage[1]	Vol	Iout = 0.8 mA	—	—	0.15	V
High-Level DC input voltage[1, 2]	VIH	—	0.7 × OVDD	—	OVDD	V
Low-Level DC input voltage[1, 2]	VIL	—	0	—	0.3 × OVDD	V
Input Hysteresis	VHYS	OVDD = 1.875 V OVDD = 2.775 V	0.25	0.34 0.45	—	V
Schmitt trigger VT+[2, 3]	VT+	—	0.5 × OVDD	—	—	V
Schmitt trigger VT-[2, 3]	VT-	—	—	—	0.5 × OVDD	V
Input current (no pull-up/down)	Iin	Vin = OVDD or 0	—	—	10	µA
Input current (22 kΩ Pull-up)	Iin	Vin = 0 V Vin = OVDD	—	—	161 10	µA
Input current (47 kΩ Pull-up)	Iin	Vin = 0 V Vin = OVDD	—	—	76 10	µA
Input current (100 kΩ Pull-up)	Iin	Vin = 0 V Vin= OVDD	—	—	40 10	µA



$$Rpu = \frac{Vovdd - Vref1}{Vref1} \times Ztl$$

$$Rpd = \frac{Vref2}{Vovdd - Vref2} \times Ztl$$

Figure 4. Impedance Matching Load for Measurement

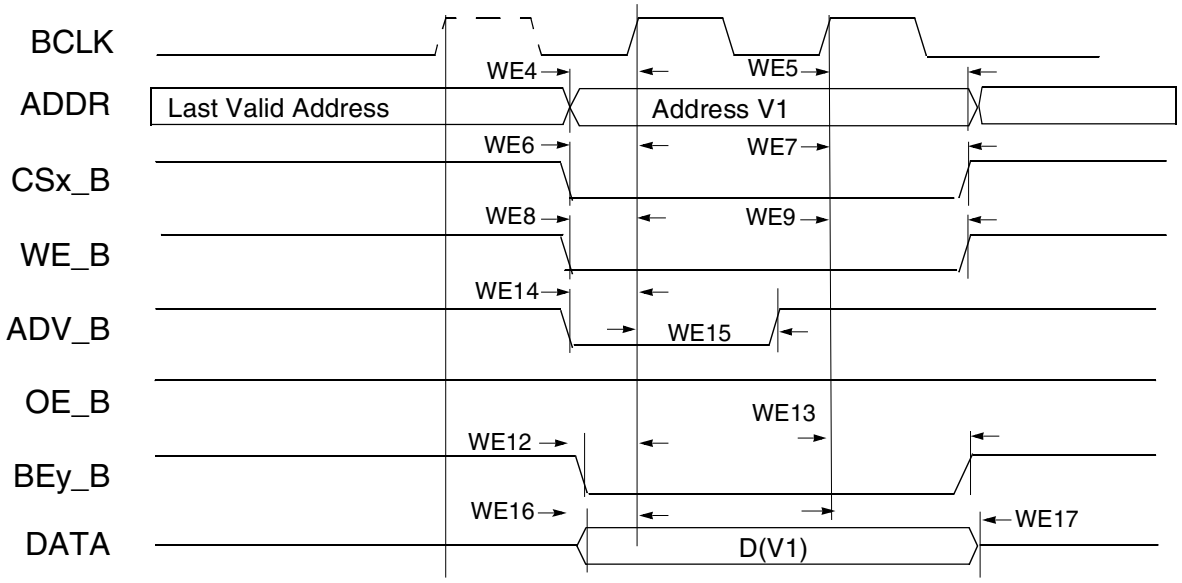


Figure 19. Synchronous Memory, Write Access, WSC=1, WBEA=0, and WADVN=0

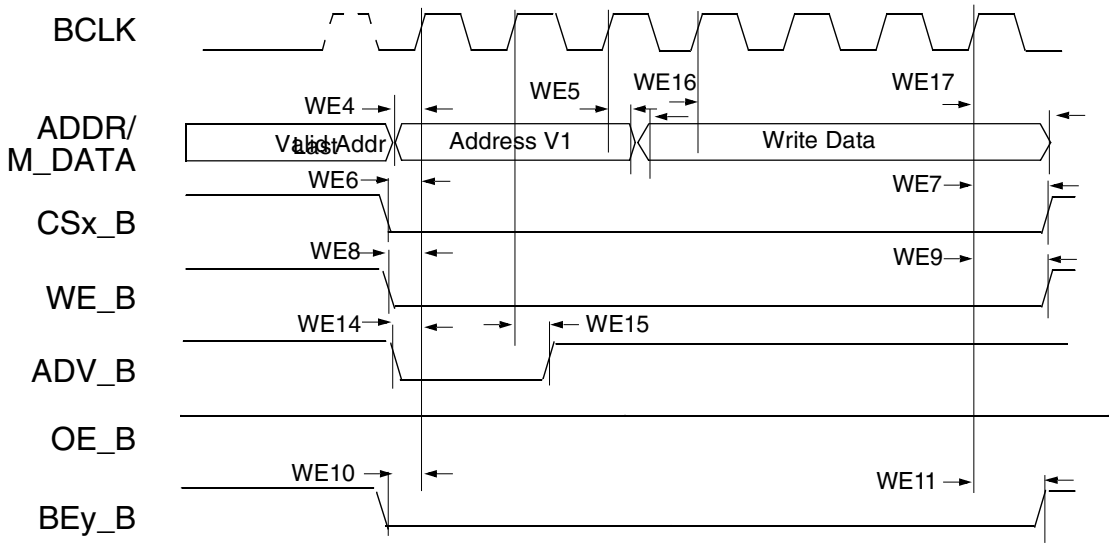


Figure 20. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6, ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

Table 45. CSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time	t_{clk}	60	—	ns
CS2	SCLK High or Low Time	t_{SW}	26	—	ns
CS3	SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	SSx pulse width	t_{CSLH}	26	—	ns
CS5	SSx Lead Time (Slave Select setup time)	t_{SCS}	26	—	ns
CS6	SSx Lag Time (SS hold time)	t_{HCS}	26	—	ns
CS7	MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-1	21	ns
CS8	MISO Setup Time	t_{Smiso}	5	—	ns
CS9	MISO Hold Time	t_{Hmiso}	5	—	ns
CS10	RDY to SSx Time[2]	t_{SDRY}	5	—	ns

1 See specific I/O AC parameters Section 4.5, "I/O AC Parameters"

2 SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.7.2.2 CSPI Slave Mode Timing

Figure 33 depicts the timing of CSPI in slave mode. Timing characteristics were not available at the time of publication.

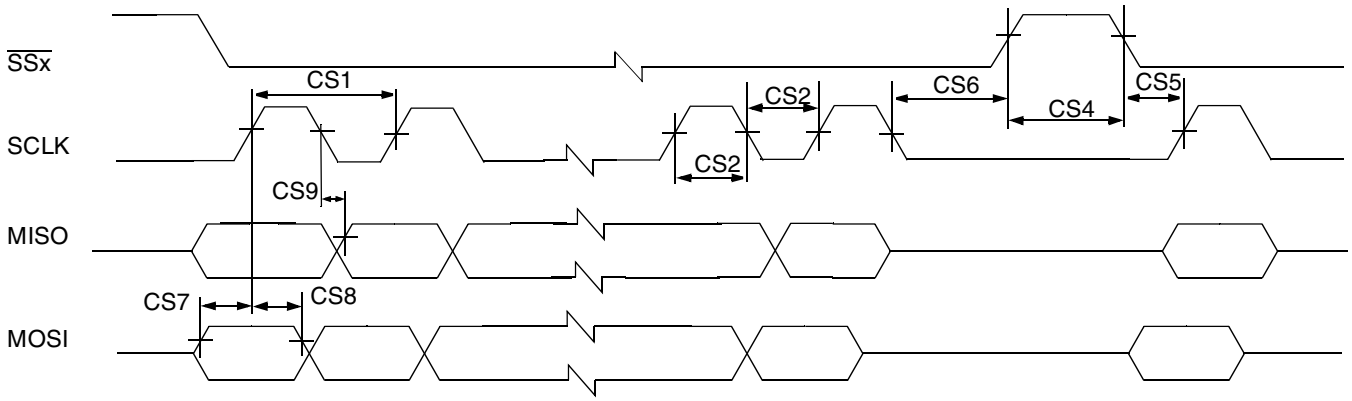


Figure 33. CSPI/ECSPI Slave Mode Timing Diagram

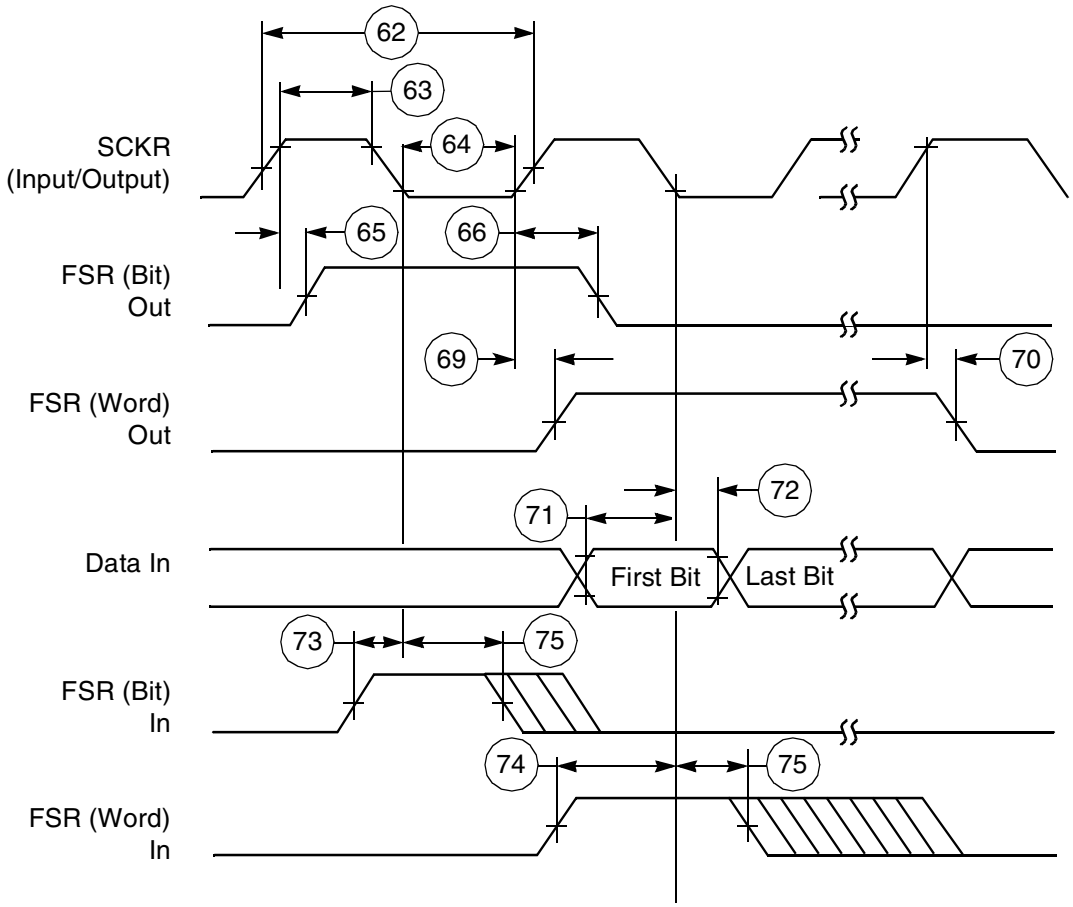


Figure 35. ESAI Receiver Timing

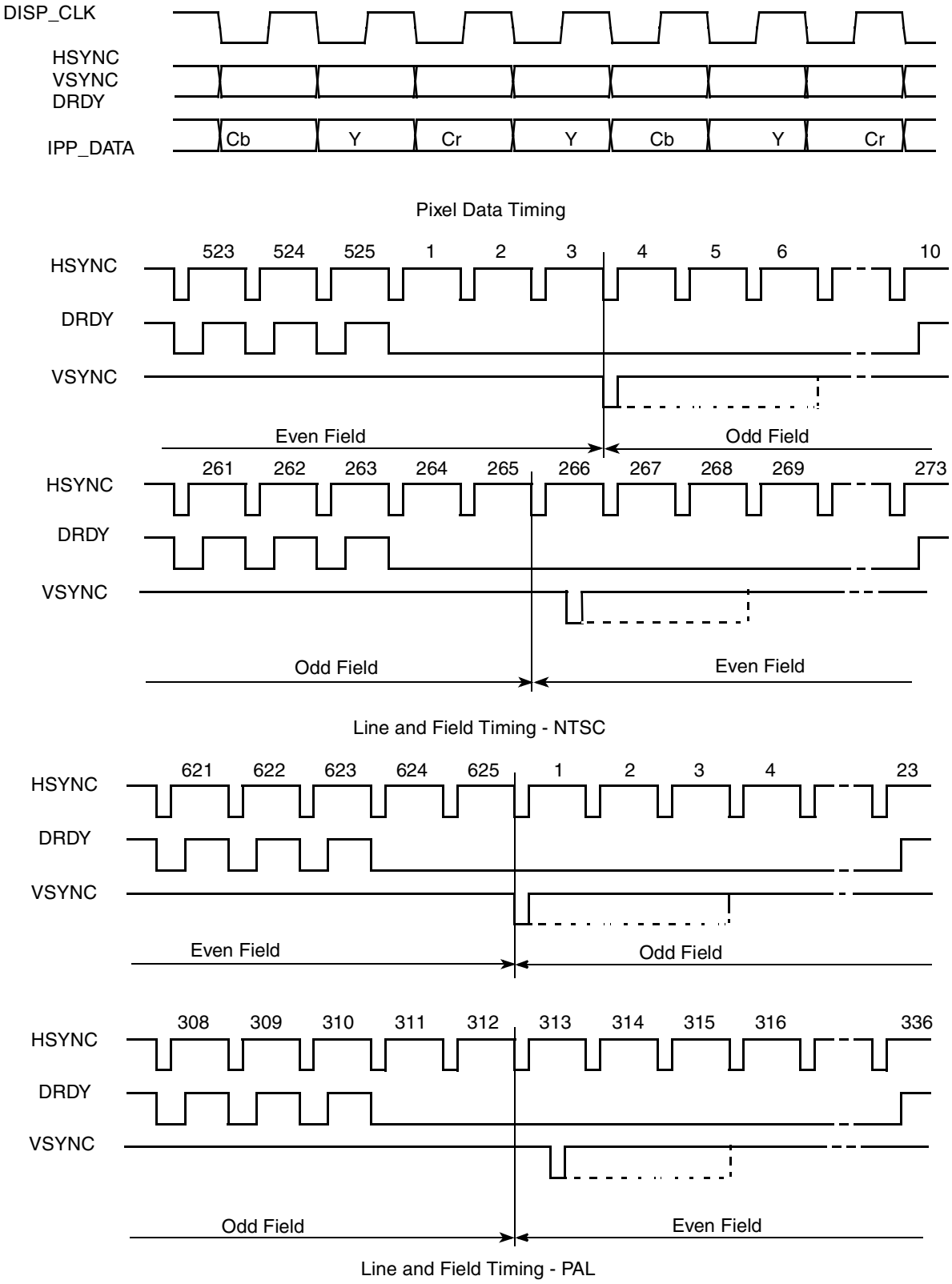


Figure 51. TV Encoder Interface Timing Diagram

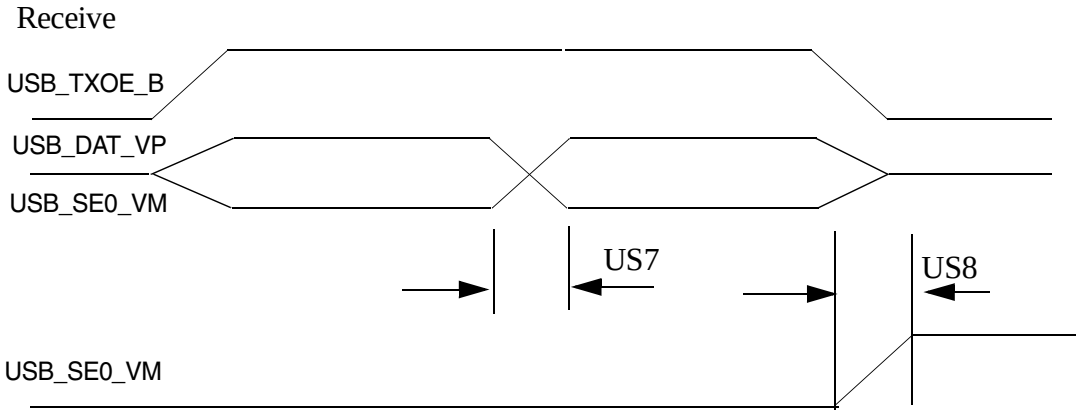


Figure 90. USB Receive Waveform in DAT_SE0 Bidirectional Mode

Table 92. Definitions of USB Waveform in DAT_SE0 Bi — Directional Mode

No.	Parameter	Signal Name	Direction	Min	Max	Unit	Conditions / Reference Signal
US1	TX Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US2	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US3	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US4	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US7	RX Rise/Fall Time	USB_DAT_VP	In	—	3.0	ns	35 pF
US8	RX Rise/Fall Time	USB_SE0_VM	In	—	3.0	ns	35 pF

Table 111. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config. Value
DRAM_A3	N20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[3]	Output	Low
DRAM_A4	K20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[4]	Output	Low
DRAM_A5	N21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[5]	Output	Low
DRAM_A6	M22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[6]	Output	Low
DRAM_A7	N22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[7]	Output	Low
DRAM_A8	N23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[8]	Output	Low
DRAM_A9	M21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[9]	Output	Low
DRAM_CALIBRATION	M23	NVCC_EMI_DRAM	special	—	—	(used in DRAM driver calibration. See Section 3.1, “Special Signal Considerations”)	Input	—
DRAM_CAS	L18	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_CAS	Output	High
DRAM_CS0	K18	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_CS[0]	Output	High
DRAM_CS1	P19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_CS[1]	Output	High
DRAM_D0	H20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[0]	Output	High
DRAM_D1	G21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[1]	Output	High
DRAM_D10	E22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[10]	Output	High
DRAM_D11	D20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[11]	Output	High
DRAM_D12	E23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[12]	Output	High
DRAM_D13	C23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[13]	Output	High
DRAM_D14	F23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[14]	Output	High
DRAM_D15	C22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[15]	Output	High
DRAM_D16	U20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[16]	Output	High

Table 111. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config. Value
DRAM_D6	J22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[6]	Output	High
DRAM_D7	G22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[7]	Output	High
DRAM_D8	E21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[8]	Output	High
DRAM_D9	D21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_D[9]	Output	High
DRAM_DQM0	H21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_DQM[0]	Output	Low
DRAM_DQM1	E20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_DQM[1]	Output	Low
DRAM_DQM2	T20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_DQM[2]	Output	Low
DRAM_DQM3	W20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_DQM[3]	Output	Low
DRAM_RAS	J19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_RAS	Output	High
DRAM_RESET	P18	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_RESET	Output	Low
DRAM_SDBA0	R19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_SDBA[0]	Output	Low
DRAM_SDBA1	P20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_SDBA[1]	Output	Low
DRAM_SDBA2	N19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_SDBA[2]	Output	Low
DRAM_SDCKE0	H19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_SDCKE[0]	Output	Low
DRAM_SDCKE1	T19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_SDCKE[1]	Output	Low
DRAM_SDCLK_0	K23	NVCC_EMI_DRAM	DDR3CLK	ALT0	EXTMC	emi_DRAM_SDCLK0	Output	Floating
DRAM_SDCLK_0_B	K22	NVCC_EMI_DRAM	DDR3CLK	ALT0	EXTMC	emi_DRAM_SDCLK0_B	Output	Floating
DRAM_SDCLK_1	P22	NVCC_EMI_DRAM	DDR3CLK	ALT0	EXTMC	emi_DRAM_SDCLK1	Output	Floating
DRAM_SDCLK_1_B	P23	NVCC_EMI_DRAM	DDR3CLK	ALT0	EXTMC	emi_DRAM_SDCLK1_B	Output	Floating

Table 111. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config. Value
EIM_DA10	AB7	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[10]	Input[2]	100 KΩ PU
EIM_DA11	AC6	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[11]	Input	100 KΩ PU
EIM_DA12	V10	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[12]	Input	100 KΩ PU
EIM_DA13	AC7	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[13]	Input	100 KΩ PU
EIM_DA14	Y10	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[14]	Input	100 KΩ PU
EIM_DA15	AA9	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[15]	Input	100 KΩ PU
EIM_DA2	AA7	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[2]	Input[2]	100 KΩ PU
EIM_DA3	W9	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[3]	Input[2]	100 KΩ PU
EIM_DA4	AB6	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[4]	Input[2]	100 KΩ PU
EIM_DA5	V9	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[5]	Input[2]	100 KΩ PU
EIM_DA6	Y9	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[6]	Input[2]	100 KΩ PU
EIM_DA7	AC5	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[7]	Input[2]	100 KΩ PU
EIM_DA8	AA8	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[8]	Input[2]	100 KΩ PU
EIM_DA9	W10	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[9]	Input[2]	100 KΩ PU
EIM_EB0	AC3	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_EB[0]	Output[2]	—
EIM_EB1	AB5	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_EB[1]	Output[2]	—
EIM_EB2	Y3	NVCC_EIM_MAIN	UHVIO	ALT1	GPIO-2	gpio2_GPIO[30]	Input	100 KΩ PU
EIM_EB3	Y4	NVCC_EIM_MAIN	UHVIO	ALT1	GPIO-2	gpio2_GPIO[31]	Input	100 KΩ PU
EIM_LBA	AA6	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_LBA	Output[2]	—
EIM_OE	V8	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_OE	Output	—
EIM_RW	AB4	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_RW	Output	—

Table 112. 19 x 19 mm, 0.8 mm Pitch Ball Map (continued)

Y	W	V	U	T	R	P
EIM_D23	EIM_D20	EIM_D18	CSI0_DAT14	CSI0_DAT8	CSI0_DAT4	CSI0_PIXCLK
EIM_D24	EIM_D22	EIM_D19	CSI0_DAT15	CSI0_DAT11	CSI0_DAT5	CSI0_MCLK
EIM_EB2	EIM_D25	EIM_D21	CSI0_DAT18	CSI0_DAT12	CSI0_DAT7	CSI0_DATA_EN
EIM_EB3	EIM_D30	EIM_D27	CSI0_DAT19	CSI0_DAT16	CSI0_DAT9	CSI0_VSYNC
EIM_A24	EIM_D31	EIM_D26	EIM_D17	CSI0_DAT17	CSI0_DAT10	PATA_DATA15
EIM_A20	EIM_A25	EIM_A23	EIM_D16	CSI0_DAT13	CSI0_DAT6	PATA_DATA14
EIM_CS1	EIM_A19	EIM_A17	NVCC_EIM_SEC	VCC	NVCC_CSI	GND
EIM_DA0	EIM_CS0	EIM_OE	VCC	GND	VCC	GND
EIM_DA6	EIM_DA3	EIM_DA5	NVCC_EIM_MAIN	VCC	GND	VCC
EIM_DA14	EIM_DA9	EIM_DA12	NVCC_EIM_MAIN	GND	VCC	GND
NANDF_ALE	EIM_BCLK	NVCC_SRTC_POW	NANDF_RB0	VCC	GND	VCC
LVDS1_TX3_P	NANDF_CS0	NVCC_XTAL	VDDA	NVCC_NANDF	VCC	GND
LVDS1_CLK_P	NANDF_CS3	NANDF_CS1	NVCC_LVDS	VCC	GND	VCC
GND	PMIC_ON_REQ	NANDF_CS2	NVCC_LVDS_BG	GND	VCC	GND
GND	PMIC_STBY_REQ	GND	GND	VCC	GND	VCC
LVDS0_TX2_N	GPIO_10	TVDAC_AHVDDRGB	TVDAC_DHVDD	GND	VCC	GND
LVDS0_TX0_N	GPIO_12	GPIO_11	TVDAC_AHVDDRGB	VCC	GND	NVCC_EMI_DRAM
TVDAC_VREF	GPIO_14	GND	VCC	NVCC_EMI_DRAM	DRAM_SDODT1	DRAM_RESET
GND	GND	GND	GND	DRAM_SDCKE1	DRAM_SDBA0	DRAM_CS1
DRAM_D24	DRAM_DQM3	GND	DRAM_D16	DRAM_DQM2	GND	DRAM_SDBA1
DRAM_D26	DRAM_D25	GND	DRAM_D18	DRAM_D17	DRAM_D19	GND
DRAM_SDQS3	DRAM_D27	GND	DRAM_D22	DRAM_SDQS2	DRAM_D21	DRAM_SDCLK_1
DRAM_SDQS3_B	DRAM_D31	DRAM_D29	DRAM_D20	DRAM_SDQS2_B	DRAM_D23	DRAM_SDCLK_1_B
Y	W	V	U	T	R	P

7 Revision History

Table 113 provides a revision history for this data sheet.

Table 113. i.MX53 Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev. 6	03/2013	In Table 1, “Ordering Information” removed MCIMX535DVV2C, as it no longer exists. In Table 6, “i.MX53 Operating Ranges,” updated minimum values of LVDS interface supply (NVCC_LVDS) and LVDS band gap supply (NVCC_LVDS_BG) to 2.375 volts.
Rev. 5	09/2012	• In Table 1, "Ordering Information," on page 2,” renamed “Features” column as “CPU Frequency.” • In Section 1.2, “Features:” —Changed “SATA I” to “SATA II” under Hard disk drives bullet —Added a new bullet item to mention support for tamper detection mechanism • In Section 1.2, “Features,” added a new bullet item to mention support for FlexCAN feature. • Removed the note shown at the end of Section 1.2, “Features.” • In Table 2, "i.MX53 Digital and Analog Blocks," on page 7, removed details of MPEG2 encoder, as this is not supported on i.MX53. • In Table 6, "i.MX53 Operating Ranges," on page 18: —Changed VDDGP max voltage, for all frequency ranges and for STOP mode, to 1.15 V —Updated footnote on TVDAC_DHVDD and TVDAC_AHVDDRGB • In Table 8, "Maximal Supply Currents," on page 20: —Corrected power line name, MVCC_XTAL, to NVCC_XTAL —Added a footnote on NVCC_EMI_DRAM —Updated max current value and added a footnote for power line, NVCC_SRTC_POW —Removed duplicate entries for NVCC_EMI_DRAM and NVCC_XTAL • In Section 4.2.3, “Power Supplies Usage,” updated the fourth bullet item. • In Figure 25, "Asynchronous A/D Muxed Write Access," on page 58, renamed “WE41” as “WE41A” and shifted its position to left. • In Table 57, "Camera Input Signal Cross Reference, Format and Bits Per Cycle," on page 80, added a footnote on “YCbCr 8 bits 2 cycles” column header.
Rev. 4	11/2011	• In Section 1, “Introduction,” changed 1 GHz to 1.2 GHz in the second paragraph and updated the bulleted list after the second paragraph. • In Table 1, "Ordering Information," on page 2: —Removed part numbers “PCIMX535DVV1C” and “MCIMX538DZK1C” —Added a new part number “MCIMX535DVV2C” —Updated package information for part number “PCIMX538DZK1C” —Updated the second footnote • In Section 1.2, “Features,” changed “Target frequency” to “Maximum frequency” and 1 GHz to 1–1.2 GHz in the third bullet item of the first bulleted list. • In Table 2, "i.MX53 Digital and Analog Blocks," on page 7, removed “Sorenson H.263 decode, 4CIF resolution, 8 Mbps bit rate” from VPU brief description. • In Table 4, "Absolute Maximum Ratings," on page 16, changed the maximum voltage for VDDGP from 1.35V to 1.4V. • In Table 6, "i.MX53 Operating Ranges," on page 18: —Added a row and a footnote for “ARM core supply voltage $f_{ARM} \leq$ 1200 MHz” parameter of VDDGP —Added a new footnote for “Peripheral supply voltage” parameter of VCC —Updated the footnote for “Junction temperature” parameter • In Section 1.2, “Features,” changed “Target frequency” to “Maximum frequency” in the third bullet item of the first bulleted list. • In Table 2, "i.MX53 Digital and Analog Blocks," on page 7, removed “Sorenson H.263 decode, 4CIF resolution, 8 Mbps bit rate” from VPU brief description. (continued on next page)