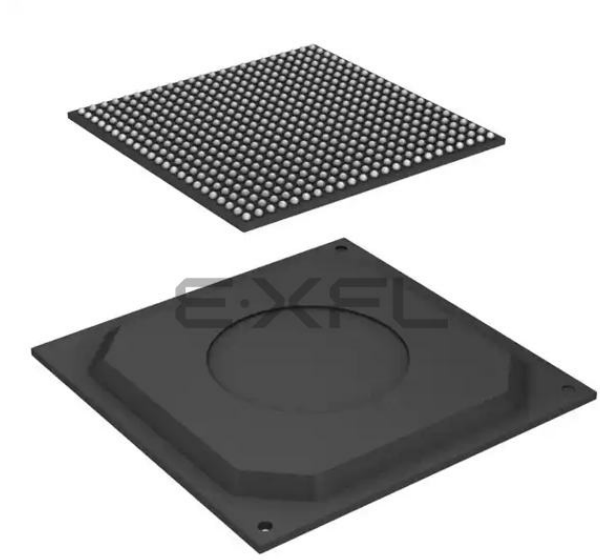

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR2, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	SATA 1.5Gbps (1)
USB	USB 2.0 (2), USB 2.0 + PHY (2)
Voltage - I/O	1.3V, 1.8V, 2.775V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	529-FBGA
Supplier Device Package	529-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx537cvv8c

Table 2. i.MX53 Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
DEBUG	Debug System	System Control	The debug system provides real-time trace debug capability of both instructions and data. It supports a trace protocol that is an integral part of the ARM Real Time Debug solution (RealView). Real-time tracing is controlled by specifying a set of triggering and filtering resources, which include address and data comparators, three cross-system triggers (CTI), counters, and sequencers. debug access port (DAP)— The DAP provides real-time access for the debugger without halting the core to system memory, peripheral register, debug configuration registers and JTAG scan chains.
EXTMC	External Memory Controller	Connectivity Peripherals	The EXTMC is an external and internal memory interface. It performs arbitration between multi-AXI masters to multi-memory controllers, divided into four major channels, fast memories (DDR2/DDR3/LPDDR2) channel, slow memories (NOR-FLASH / PSRAM / NAND-FLASH etc.) channel, internal memory (RAM, ROM) channel and graphical memory (GMEM) channel. In order to increase the bandwidth performance, the EXTMC separates the buffering and the arbitration between different channels so parallel accesses can occur. By separating the channels, slow accesses do not interfere with fast accesses. EXTMC Features: • 64-bit and 32-bit AXI ports • Enhanced arbitration scheme for fast channel, including dynamic master priority, and taking into account which pages are open or closed and what type (read or write) was the last access • Flexible bank interleaving • Support 16/32-bit DDR2-800 or DDR3-800 or LPDDR2. • Support up to 2 GByte DDR memories. • Support NFC, EIM signal muxing scheme. • Support 8/16/32-bit Nor-Flash/PSRAM memories (sync and async operating modes), at slow frequency. (8-bit is not supported on D[23]-D[16]). • Support 4/8/14/16-bit ECC, page sizes of 512-B, 2-KB and 4-KB Nand-Flash (including MLC) • Multiple chip selects (up to 4). • Enhanced DDR memory controller, supporting access latency hiding • Support watermark for security (internal and external memories)
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter values can be programmed on the fly.
ESAI	Enhanced Serial Audio Interface	Connectivity Peripherals	The enhanced serial audio interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. The ESAI has 12 pins for data and clocking connection to external devices.

Table 2. i.MX53 Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
RTIC	Run-Time Integrity Checker	Security	Protecting read only data from modification is one of the basic elements in trusted platforms. The run-time integrity checker, version 3 (RTIC) block is a data-monitoring device responsible for ensuring that the memory content is not corrupted during program execution. The RTIC mechanism periodically checks the integrity of code or data sections during normal OS run-time execution without interfering with normal operation. The purpose of the RTIC is to ensure the integrity of the peripheral memory contents, protect against unauthorized external memory elements replacement and assist with boot authentication.
SAHARA	SAHARA Security Accelerator	Security	SAHARA (symmetric/asymmetric hashing and random accelerator), version 4, is a security coprocessor. It implements symmetric encryption algorithms, (AES, DES, 3DES, RC4 and C2), public key algorithms (RSA and ECC), hashing algorithms (MD5, SHA-1, SHA-224 and SHA-256), and a hardware true random number generator. It has a slave IP Bus interface for the host to write configuration and command information, and to read status information. It also has a DMA controller, with an AHB bus interface, to reduce the burden on the host to move the required data to and from memory.
SATA	Serial ATA	Connectivity Peripherals	SATA HDD interface, includes the SATA controller and the PHY. It is a complete mixed-signal IP solution for SATA HDD connectivity.
SCCv2	Security Controller, ver. 2	Security	The security controller is a security assurance hardware module designed to safely hold sensitive data, such as encryption keys, digital right management (DRM) keys, passwords and biometrics reference data. The SCCv2 monitors the system's alert signal to determine if the data paths to and from it are secure, that is, it cannot be accessed from outside of the defined security perimeter. If not, it erases all sensitive data on its internal RAM. The SCCv2 also features a key encryption module (KEM) that allows non-volatile (external memory) storage of any sensitive data that is temporarily not in use. The KEM utilizes a device-specific hidden secret key and a symmetric cryptographic algorithm to transform the sensitive data into encrypted data.
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off loading various cores in dynamic data routing. The SDMA features list is as follows: • Powered by a 16-bit instruction-set micro-RISC engine • Multi-channel DMA supports up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast context-switching with two-level priority-based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unidirectional and bidirectional flows (copy mode) • Up to 8-word buffer for configurable burst transfers to / from the EXTMC • Support of byte swapping and CRC calculations • A library of scripts and API is available

Table 4. Absolute Maximum Ratings (continued)

Parameter Description	Symbol	Min	Max	Unit
Input voltage on USB_OTG_DP, USB_OTG_DN, USB_H1_DP, USB_H1_DN pins	USB_DP/USB_DN	-0.3	3.63[1]	V
Input/Output Voltage Range	V_{in}/V_{out}	-0.5	OVDD +0.3[2]	V
ESD Damage Immunity: • Human Body Model (HBM) • Charge Device Model (CDM)	V_{esd}	 — —	 2000 500	V
Storage Temperature Range	$T_{STORAGE}$	-40	150	°C

1 USB_DN and USB_DP can tolerate 5 V for up to 24 hours.

2 The term OVDD in this section refers to the associated supply rail of an input or output. The association is described in Table 111 on page 148. The maximum range can be superseded by the DC tables.

4.1.2 Thermal Resistance

4.1.2.1 TEPBGA-2 Package Thermal Resistance

Table 5 provides the TEPBGA-2 package thermal resistance data.

Table 5. TEPBGA-2 Package Thermal Resistance Data

Rating	Board	Symbol	Value	Unit
Junction to Ambient (natural convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	28	°C/W
Junction to Ambient (natural convection)[1, 2, 3]	Four layer board (2s2p)	$R_{\theta JA}$	16	°C/W
Junction to Ambient (at 200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	21	°C/W
Junction to Ambient (at 200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	13	°C/W
Junction to Board[4]	—	$R_{\theta JB}$	6	°C/W
Junction to Case[5]	—	$R_{\theta JC}$	4	°C/W
Junction to Package Top (natural convection)[6]	—	Ψ_{JT}	4	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.2.2 Power-Down Sequence

Power-down sequence should follow one of the following two options:

- Option 1: Switch all supplies down simultaneously with further free discharge. A deviation of few microseconds of actual power-down of the different power rails is acceptable.
- Option 2: Switch down supplies, in any order, keeping the following rules:
  - NVCC_CKIH must be powered down at the same time or after the UHVIO I/O cell supplies (for full supply list, see Table 6, Ultra High voltage I/O (UHVIO) supplies). A deviation of few microseconds of actual power-down of the different power rails is acceptable.
  - VDD_REG must be powered down at the same time or after NVCC_EMI_DRAM supply. A deviation of few microseconds of actual power-down of the different power rails is acceptable.
  - If all of the following conditions are met:
    – VDD_REG is powered down to 0V (Not Hi-Z)
    – VDD_DIG_PLL and VDD_ANA_PLL are provided externally,
    – VDD_REG is powered down before VDD_DIG_PLL and VDD_ANA_PLL
    Then the following rule should be kept: VDD_REG output impedance must be higher than 1 kW, when inactive.

4.2.3 Power Supplies Usage

- All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is off. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Rail” columns in pin list tables of Section 6, “Package Information and Contact Assignments.”
- If not using SATA interface and the embedded thermal sensor, the VP and VPH should be grounded. In particular, keeping VPH turned OFF while the VP is powered ON is not recommended and might lead to excessive power consumption.
- When internal clock source is used for SATA temperature monitor the USB_PHY supplies and PLL need to be active because they are providing the clock.
- If not using the TVE module, the TVDAC_DHVDD and TVDAC_AHVDDRGB can be kept floating or tied to GND—the recommendation is to float. If only the GPIO pads in TVDAC_AHVDDRGB domain are in use, the supplies can be set to GPIO pad voltage range (1.65 V to 3.1 V).

4.3 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate 3 I/O (DDR3) for DDR2/LVDDR2, LPDDR2 and DDR3 modes
- Low Voltage I/O (LVIO)
- Ultra High Voltage I/O (UHVIO)
- LVDS I/O

4.3.5 LVDS I/O DC Parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

Table 16 shows the Low Voltage Differential Signaling (LVDS) DC electrical characteristics. The parameters in Table 16 are guaranteed per the operating ranges in Table 6, unless otherwise noted.

Table 16. LVDS DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Differential Voltage	V_{OD}	Rload = 100Ω between padP and padN	250	350	450	mV
Output High Voltage	V_{OH}		1.25	1.375	1.6	V
Output Low Voltage	V_{OL}		0.9	1.025	1.25	
Offset Voltage	V_{OS}		1.125	1.2	1.375	

4.4 Output Buffer Impedance Characteristics

This section defines the I/O Impedance parameters of the i.MX53 processor for the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate 3 I/O (DDR3) for DDR2/LVDDR2, LPDDR2, and DDR3 modes
- Ultra High Voltage I/O (UHVIO)
- LVDS I/O

NOTE

Output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission lime. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 4).

4.5.1 GPIO I/O AC Electrical Characteristics

AC electrical characteristics for GPIO I/O in slow and fast modes are presented in the Table 20 and Table 21, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bit in the IOMUXC control registers.

Table 20. GPIO I/O AC Parameters Slow Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF	—	—	1.91/1.52 3.07/2.65	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF	—	—	2.22/1.81 3.81/3.42	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF	—	—	2.88/2.42 5.43/5.02	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF	—	—	4.94/4.50 10.55/9.70	ns
Output Pad Slew Rate (Max Drive)[1]	tps	15 pF 35 pF	0.5/0.65 0.32/0.37	—	—	V/ns
Output Pad Slew Rate (High Drive)[1]	tps	15 pF 35 pF	0.43/0.54 0.26/0.41	—	—	
Output Pad Slew Rate (Medium Drive)[1]	tps	15 pF 35 pF	0.34/0.41 0.18/0.2	—	—	
Output Pad Slew Rate (Low Drive)[1]	tps	15 pF 35 pF	0.20/0.22 0.09/0.1	—	—	
Output Pad di/dt (Max Drive)	tdit	—	—	—	30	mA/ns
Output Pad di/dt (High Drive)	tdit	—	—	—	23	
Output Pad di/dt (Medium drive)	tdit	—	—	—	15	
Output Pad di/dt (Low drive)	tdit	—	—	—	7	
Input Transition Times[2]	trm	—	—	—	25	ns

1 tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

2 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 21. GPIO I/O AC Parameters Fast Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF	—	—	1.45/1.24 2.76/2.54	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF	—	—	1.81/1.59 3.57/3.33	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF	—	—	2.54/2.29 5.25/5.01	ns

Table 24. LPDDR2 I/O DDR3 mode AC Characteristics[1] (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single output slew rate	tsr	At 25 Ω to Vref	2.5	—	5	V/ns
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 266 MHz clk = 400 MHz	—	—	0.2 0.1	ns

1 Note that the JEDEC JESD79_3C specification supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4 The typical value of Vox(ac) is expected to be about 0.5 x OVDD and Vox(ac) is expected to track variation in OVDD. Vox(ac) indicates the voltage at which differential output signal must cross.

4.5.3 LVIO I/O AC Electrical Characteristics

AC electrical characteristics for LVIO I/O in slow and fast modes are presented in the Table 25 and Table 26, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bit in the IOMUXC control registers.

Table 25. LVIO I/O AC Parameters in Slow Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 38. EIM Bus Timing Parameters (continued)[1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE3	BCLK High Level Width	0.4 x t		0.8 x t		1.2 x t		1.6 x t	
WE4	Clock rise to address valid[3]	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE5	Clock rise to address invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE6	Clock rise to CSx_B valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE7	Clock rise to CSx_B invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE8	Clock rise to WE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE9	Clock rise to WE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE10	Clock rise to OE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE11	Clock rise to OE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE12	Clock rise to BEy_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE13	Clock rise to BEy_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE14	Clock rise to ADV_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE15	Clock rise to ADV_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE16	Clock rise to Output Data Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE17	Clock rise to Output Data Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE18	Input Data setup time to Clock rise	2 ns	—	4 ns	—	—	—	—	—
WE19	Input Data hold time from Clock rise	2 ns	—	2 ns	—	—	—	—	—
WE20	WAIT_B setup time to Clock rise	2 ns	—	4 ns	—	—	—	—	—
WE21	WAIT_B hold time from Clock rise	2 ns	—	2 ns	—	—	—	—	—

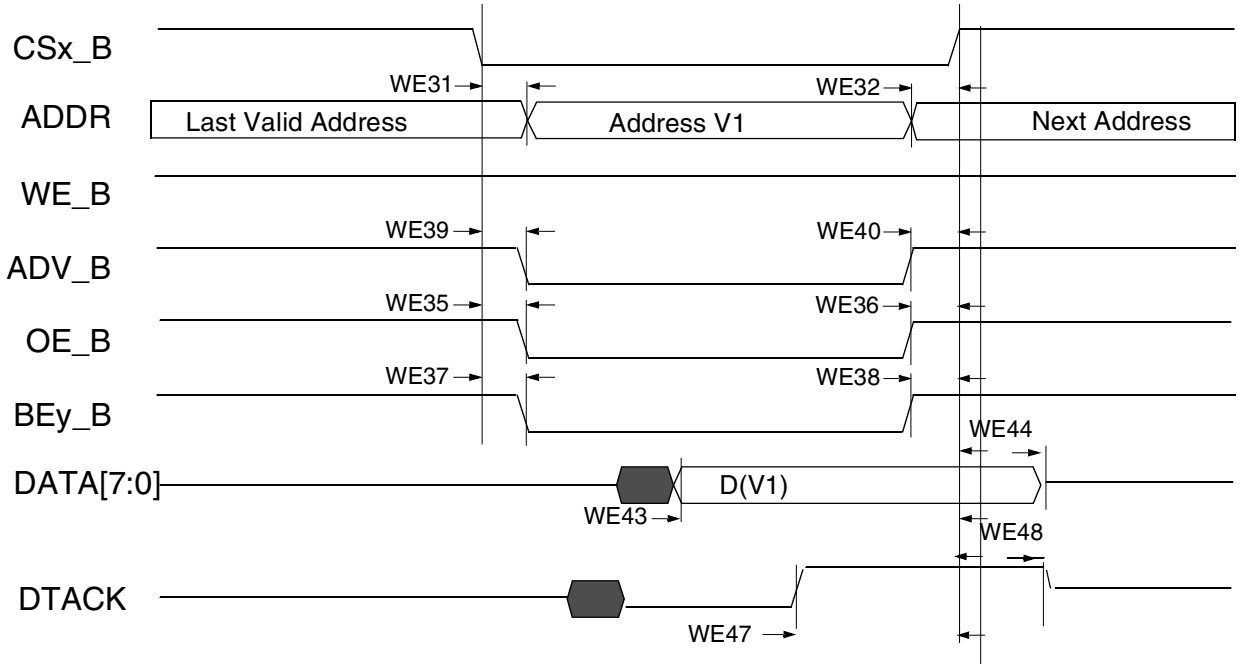

Figure 26. DTACK Read Access (DAP=0)

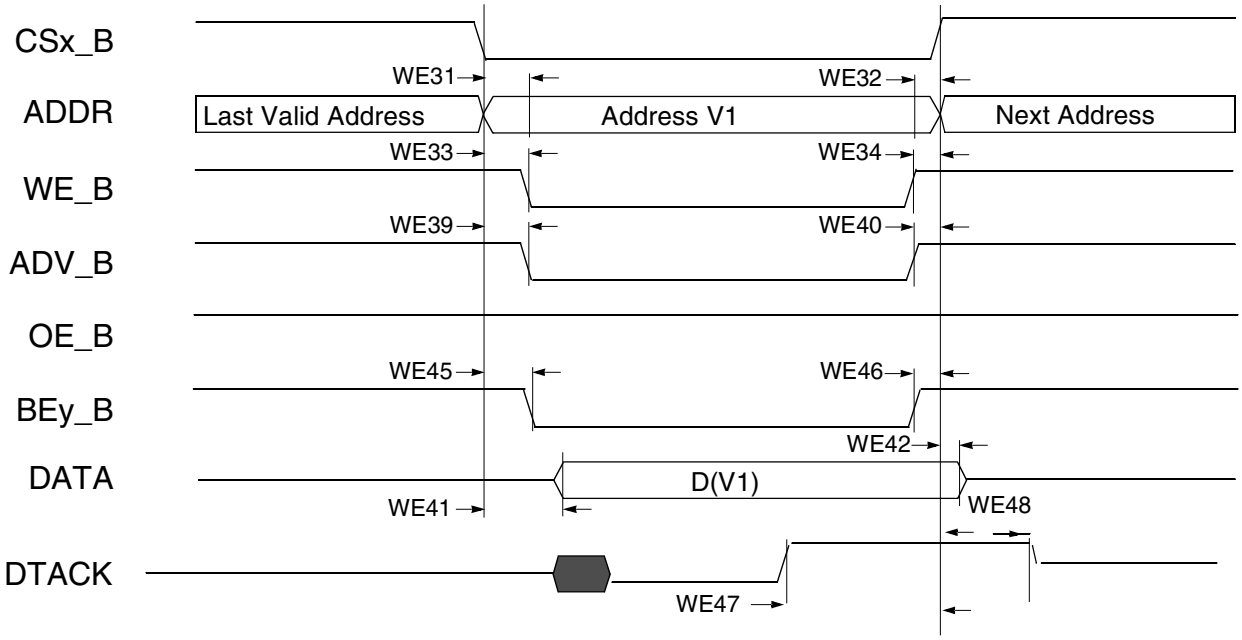

Figure 27. DTACK Write Access (DAP=0)

Table 48. Enhanced Serial Audio Interface (ESAI) Timing (continued)

No.	Characteristics[1,2,3]	Symbol	Expression[3]	Min	Max	Condition[4]	Unit
80	SCKT rising edge to FST out (wr) high[6]	— —	— —	— —	20.0 10.0	x ck i ck	ns
81	SCKT rising edge to FST out (wr) low[6]	— —	— —	— —	22.0 12.0	x ck i ck	ns
82	SCKT rising edge to FST out (wl) high	— —	— —	— —	19.0 9.0	x ck i ck	ns
83	SCKT rising edge to FST out (wl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
84	SCKT rising edge to data out enable from high impedance	— —	— —	— —	22.0 17.0	x ck i ck	ns
86	SCKT rising edge to data out valid	— —	— —	— —	18.0 13.0	x ck i ck	ns
87	SCKT rising edge to data out high impedance [77]	— —	— —	— —	21.0 16.0	x ck i ck	ns
89	FST input (bl, wr) setup time before SCKT falling edge[6]	— —	— —	2.0 18.0	— —	x ck i ck	ns
90	FST input (wl) setup time before SCKT falling edge	— —	— —	2.0 18.0	— —	x ck i ck	ns
91	FST input hold time after SCKT falling edge	— —	— —	4.0 5.0	— —	x ck i ck	ns
95	HCKR/HCKT clock cycle	—	2 x T_C	15	—	—	ns
96	HCKT input rising edge to SCKT output	—	—	—	18.0	—	ns
97	HCKR input rising edge to SCKR output	—	—	—	18.0	—	ns

1 VCORE_VDD= 1.00 ± 0.10V
Tj = -40 °C to 125 °C
CL= 50 pF

2 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that SCKT and SCKR are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that SCKT and SCKR are the same clock)

3 bl = bit length
wl = word length
wr = word length relative

4 SCKT(SCKT pin) = transmit clock
SCKR(SCKR pin) = receive clock
FST(FST pin) = transmit frame sync
FSR(FSR pin) = receive frame sync
HCKT(HCKT pin) = transmit high frequency clock
HCKR(HCKR pin) = receive high frequency clock

5 For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

Table 49. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
eSDHC Input/Card Outputs CMD, DAT (Reference to CLK)					
SD7	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	eSDHC Input Hold Time[4]	t_{IH}	2.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.7.4.2 eMMC4.4 (Dual Data Rate) eSDHCv3 AC Timing

Figure 37 depicts the timing of eMMC4.4. Table 50 lists the eMMC4.4 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

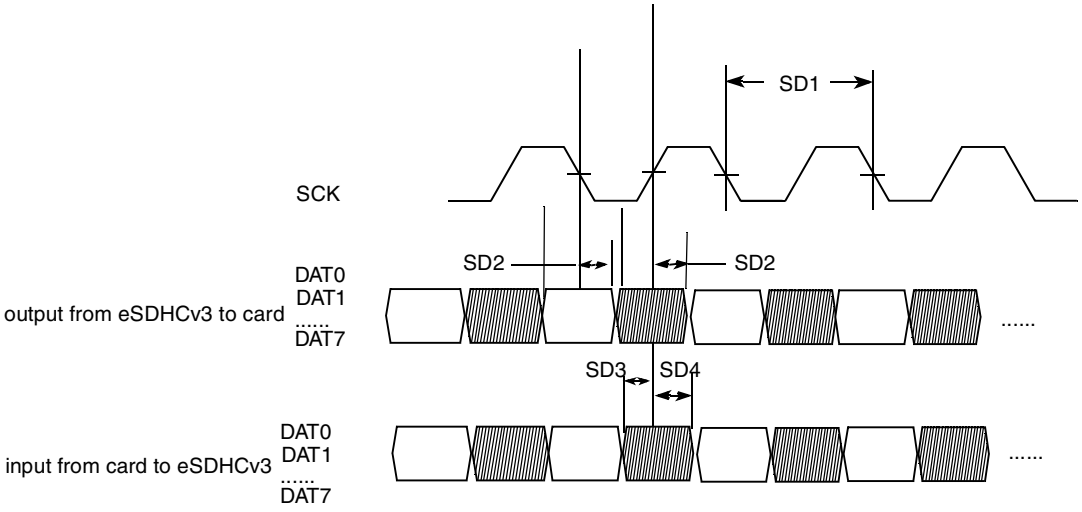

Figure 37. eMMC4.4 Timing

Table 50. eMMC4.4 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}	0	52	MHz
eSDHC Output / Card Inputs CMD, DAT (Reference to CLK)					
SD2	eSDHC Output Delay	t_{OD}	-4.5	4.5	ns

Table 60. Synchronous Display Interface Timing Characteristics (Pixel Level) (continued)

ID	Parameter	Symbol	Value	Description	Unit
IP5o	Offset of IPP_DISP_CLK	Todicp	DISP_CLK_OFFSET × Tdiclk	DISP_CLK_OFFSET—offset of IPP_DISP_CLK edges from local start point, in DI_CLK×2 (0.5 DI_CLK Resolution) Defined by DISP_CLK counter	ns
IP13o	Offset of VSYNC	Tovs	VSYNC_OFFSET × Tdiclk	VSYNC_OFFSET—offset of Vsync edges from a local start point, when a Vsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution).The VSYNC_OFFSET should be built by suitable DI's counter.	ns
IP8o	Offset of HSYNC	Tohs	HSYNC_OFFSET × Tdiclk	HSYNC_OFFSET—offset of Hsync edges from a local start point, when a Hsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution).The HSYNC_OFFSET should be built by suitable DI's counter.	ns
IP9o	Offset of DRDY	Todrdy	DRDY_OFFSET × Tdiclk	DRDY_OFFSET—offset of DRDY edges from a suitable local start point, when a corresponding data has been set on the bus, in DI_CLK×2 (0.5 DI_CLK Resolution) The DRDY_OFFSET should be built by suitable DI's counter.	ns

[1] Display interface clock period immediate value.

$$Tdicp = \begin{cases} T_{diclk} \times \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}, & \text{for integer } \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD} \\ T_{diclk}\left(floor\left[\frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}\right] + 0.5 \pm 0.5\right), & \text{for fractional } \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD} \end{cases}$$

DISP_CLK_PERIOD—number of DI_CLK per one Tdicp. Resolution 1/16 of DI_CLK.

DI_CLK_PERIOD—relation of between programing clock frequency and current system clock frequency

Display interface clock period average value.

$$\bar{T}dicp = T_{diclk} \times \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}$$

[2] DI's counter can define offset, period and UP/DOWN characteristic of output signal according to programed parameters of the counter. Same of parameters in the table are not defined by DI's registers directly (by name), but can be generated by corresponding DI's counter. The SCREEN_WIDTH is an input value for DI's HSYNC generation counter. The distance between HSYNCs is a SCREEN_WIDTH.

The maximal accuracy of UP/DOWN edge of controls is:

$$Accuracy = (0.5 \times T_{diclk}) \pm 0.62ns$$

4.7.8.7.1 TVEv2 TV Encoder Performance Specifications

The TV encoder output specifications are shown in Table 62. All the parameters in the table are defined under the following conditions:

- R_{set} = 1.05 kΩ ±1%, resistor on TVDAC_VREF pin to GND
- R_{load} = 37.5 Ω ±1%, output load to the GND

Table 62. TV Encoder Video Performance Specifications

Parameter	Conditions	Min	Typ	Max	Unit
DAC STATIC PERFORMANCE					
Resolution[1]	—	—	10	—	Bits
Integral Nonlinearity (INL)[2]	—	—	1	2	LSBs
Differential Nonlinearity (DNL) [2]	—	—	0.6	1	LSBs
Channel-to-channel gain matching[2]	—	—	2	—	%
Full scale output voltage[2]	R_{set} = 1.05 kΩ ±1% R_{load} = 37.5 Ω ±1%	1.24	1.306	1.37	V
DAC DYNAMIC PERFORMANCE					
Spurious Free Dynamic Range (SFDR)	F_{out} = 3.38 MHz F_{samp} = 216 MHz	—	59	—	dBc
Spurious Free Dynamic Range (SFDR)	F_{out} = 8.3 MHz F_{samp} = 297 MHz	—	54	—	dBc
VIDEO PERFORMANCE IN SD MODE[2]					
Short Term Jitter (Line to Line)	—	—	2.5	—	±ns
Long Term Jitter (Field to Field)	—	—	3.5	—	±ns
Frequency Response	0–4.0 MHz	-0.1	—	0.1	dB
	5.75 MHz	-0.7	—	0	dB
Luminance Nonlinearity	—	—	0.5	—	±%
Differential Gain	—	—	0.35	—	%
Differential Phase	—	—	0.6	—	Degrees
Signal-to-Noise Ratio (SNR)	Flat field full bandwidth	—	75	—	dB
Hue Accuracy	—	—	0.8	—	±Degrees
Color Saturation Accuracy	—	—	1.5	—	±%
Chroma AM Noise	—	—	-70	—	dB
Chroma PM Noise	—	—	-47	—	dB
Chroma Nonlinear Phase	—	—	0.5	—	±Degrees
Chroma Nonlinear Gain	—	—	2.5	—	±%
Chroma/Luma Intermodulation	—	—	0.1	—	±%
Chroma/Luma Gain Inequality	—	—	1.0	—	±%

Table 62. TV Encoder Video Performance Specifications (continued)

Parameter	Conditions	Min	Typ	Max	Unit
Chroma/Luma Delay Inequality	—	—	1.0	—	±ns
VIDEO PERFORMANCE IN HD MODE[2]					
Luma Frequency Response	0–30 MHz	-0.2	—	0.2	dB
Chroma Frequency Response	0–15 MHz, YCbCr 422 mode	-0.2	—	0.2	dB
Luma Nonlinearity	—	—	3.2	—	%
Chroma Nonlinearity	—	—	3.4	—	%
Luma Signal-to-Noise Ratio	0–30 MHz	—	62	—	dB
Chroma Signal-to-Noise Ratio	0–15 MHz	—	72	—	dB

1 Guaranteed by design.

2 Guaranteed by characterization.

4.7.8.8 Asynchronous Interfaces

The following sections describes the types of asynchronous interfaces.

4.7.8.8.1 Standard Parallel Interfaces

The IPU has four signal generator machines for asynchronous signal. Each machine generates IPU's internal control levels (0 or 1) by UP and DOWN that are defined in registers. Each asynchronous pin has a dynamic connection with one of the signal generators. This connection is redefined again with a new display access (pixel/component). The IPU can generate control signals according to system 80/68 requirements. The burst length is received as a result from predefined behavior of the internal signal generator machines.

The access to a display is realized by the following:

- CS (IPP_CS) chip select
- WR (IPP_PIN_11) write strobe
- RD (IPP_PIN_12) read strobe
- RS (IPP_PIN_13) Register select (A0)

Both system 80 and system 68k interfaces are supported for all described modes as depicted in Figure 52, Figure 53, Figure 54, and Figure 55. The timing images correspond to active-low IPP_CS, WR and RD signals.

Each asynchronous access is defined by an access size parameter. This parameter can be different between different kinds of accesses. This parameter defines a length of windows, when suitable controls of the current access are valid. A pause between two different display accesses can be guaranteed by programing suitable access sizes. There are no minimal/maximal hold/setup times hard defined by DI. Each control signal can be switched at any time during access size.

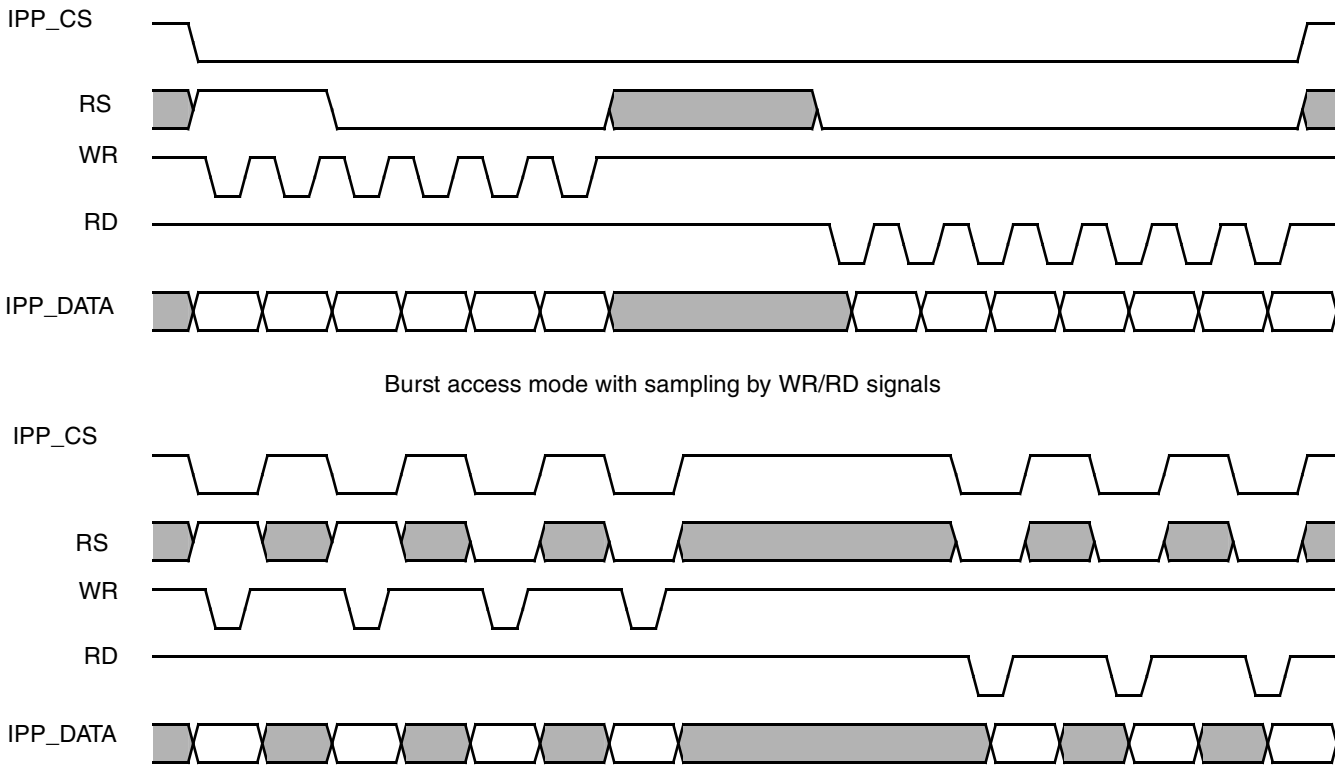

Figure 53. Asynchronous Parallel System 80 Interface (Type 2) Timing Diagram

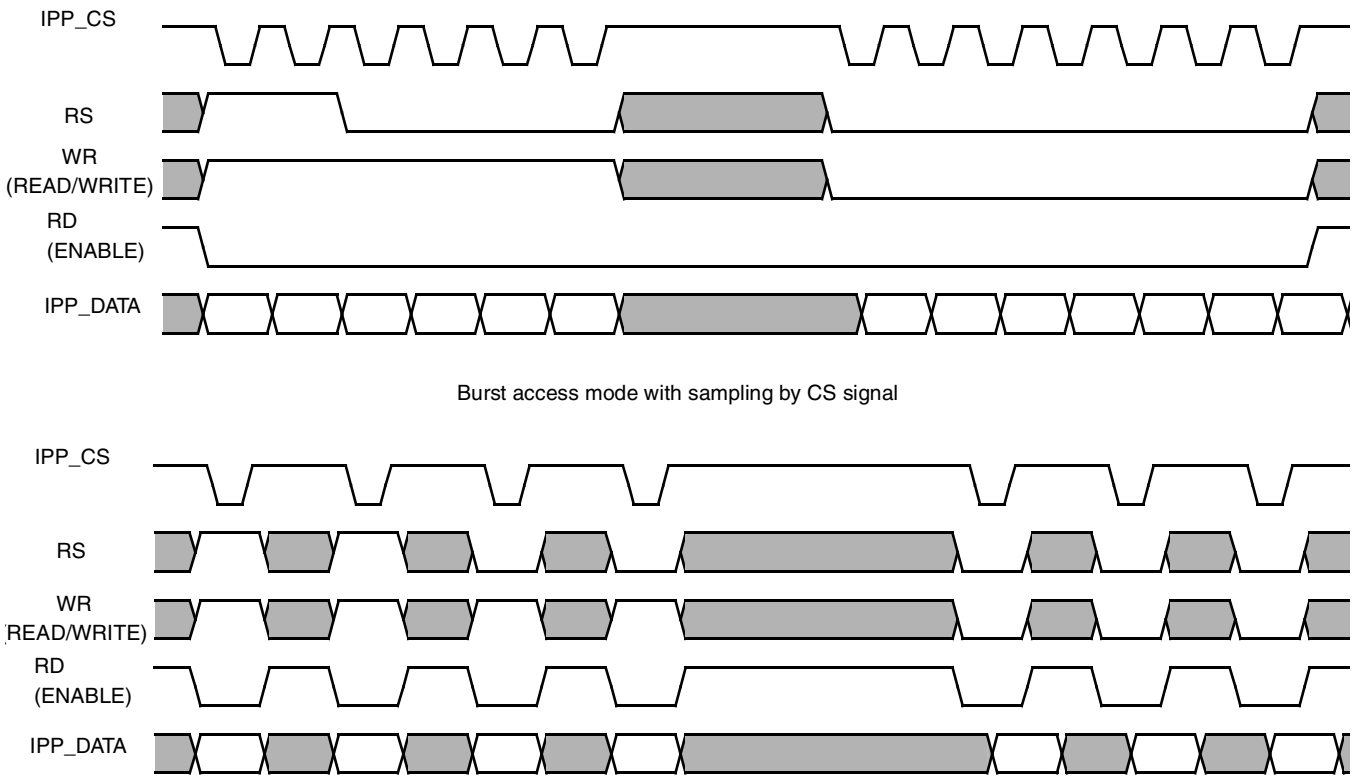

Figure 54. Asynchronous Parallel System 68k Interface (Type 1) Timing Diagram

In the timing equations, some timing parameters are used. These parameters depend on the implementation of the i.MX53 PATA interface on silicon, the bus buffer used, the cable delay and cable skew. Table 70 shows ATA timing parameters.

Table 70. PATA Timing Parameters

Name	Description	Value/ Contributing Factor[1]
T	Bus clock period (AHB_CLK_ROOT)	Peripheral clock frequency (7.5 ns for 133 MHz clock)
ti_ds	Set-up time ata_data to ata_iordy edge (UDMA-in only) UDMA0 UDMA1 UDMA2, UDMA3 UDMA4 UDMA5	 15 ns 10 ns 7 ns 5 ns 4 ns
ti_dh	Hold time ata_iordy edge to ata_data (UDMA-in only) UDMA0, UDMA1, UDMA2, UDMA3, UDMA4 UDMA5	 5.0 ns 4.6 ns
tco	Propagation delay bus clock L-to-H to ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data, ata_buffer_en	12.0 ns
tsu	Set-up time ata_data to bus clock L-to-H	8.5 ns
tsui	Set-up time ata_iordy to bus clock H-to-L	8.5 ns
thi	Hold time ata_iordy to bus clock H to L	2.5 ns
tskew1	Max difference in propagation delay bus clock L-to-H to any of following signals ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en	7 ns
tskew2	Max difference in buffer propagation delay for any of following signals: ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en	Transceiver
tskew3	Max difference in buffer propagation delay for any of following signals ata_iordy, ata_data (read)	Transceiver
tbuf	Max buffer propagation delay	Transceiver
tcable1	Cable propagation delay for ata_data	Cable
tcable2	Cable propagation delay for control signals ata_dior, ata_diow, ata_iordy, ata_dmack	Cable
tskew4	Max difference in cable propagation delay between ata_iordy and ata_data (read)	Cable
tskew5	Max difference in cable propagation delay between (ata_dior, ata_diow, ata_dmack) and ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_data(write)	Cable
tskew6	Max difference in cable propagation delay without accounting for ground bounce	Cable

[1] Values provided where applicable.

4.7.13.2.2 SATA PHY Receiver Characteristics

Table 78 provides specifications for SATA PHY receiver characteristics.

Table 78. SATA PHY Receiver Characteristics

Parameters	Symbol	Min	Typ	Max	Unit
Minimum Rx eye height (differential peak-to-peak)	$V_{MIN\_RX\_EYE\_HEIGHT}$	—	—	175	mV
Tolerance	PPM	-400	—	400	ppm

4.7.13.3 SATA_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 191 Ω 1% precision resistor on SATA_REXT pad to ground.

Resistor calibration consists of learning which state of the internal Resistor Calibration register causes an internal, digitally trimmed calibration resistor to best match the impedance applied to the SATA_REXT pin. The calibration register value is then supplied to all Tx and Rx termination resistors.

During the calibration process (for a few tens of microseconds), up to 0.3 mW can be dissipated in the external SATA_REXT resistor. At other times, no power is dissipated by the SATA_REXT resistor.

4.7.13.4 SATA Connectivity When Not in Use

NOTE

The Temperature Sensor is part of the SATA module. If SATA IP is disabled, the Temperature Sensor will not work as well. Temperature Sensor functionality is important in supporting high performance applications without overheating the device (at high ambient temp).

When both SATA and thermal sensor are not required, connect VP and VPH supplies to ground. The rest of the ports, both inputs and outputs (SATA_REFCLKM, SATA_REFCLKP, SATA_REXT, SATA_RXM, SATA_RXP, SATA_TXM) can be left floating. It is not recommended to turn off the VPH while the VP is active.

When SATA is not in use but thermal sensor is still required, both VP and VPH supplies must be powered on according to their nominal voltage levels. The reference clock input frequency must fall within the specified range of 25 MHz to 156.25 MHz. SATA_REXT does not need to be connected, as the termination impedance is not of consequence.

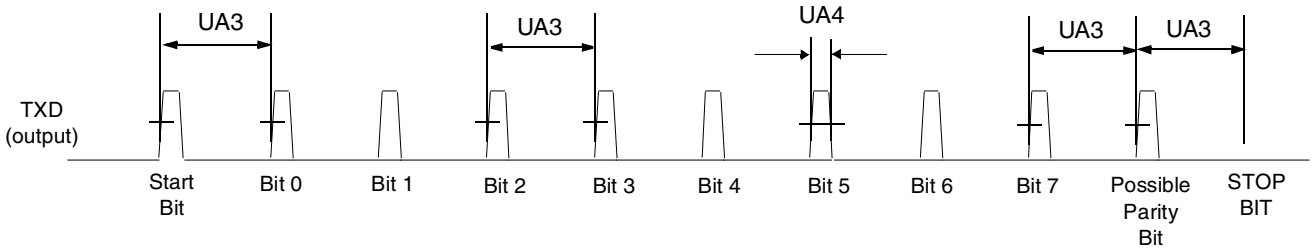

Figure 87. UART IrDA Mode Transmit Timing Diagram

Table 89. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$[1] - T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	(3/16) x ($1/F_{baud\_rate}$) - T_{ref_clk}	(3/16) x ($1/F_{baud\_rate}$) + T_{ref_clk}	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.7.17.3.4 UART IrDA Mode Receiver

Figure 88 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 90 lists the receive timing characteristics.

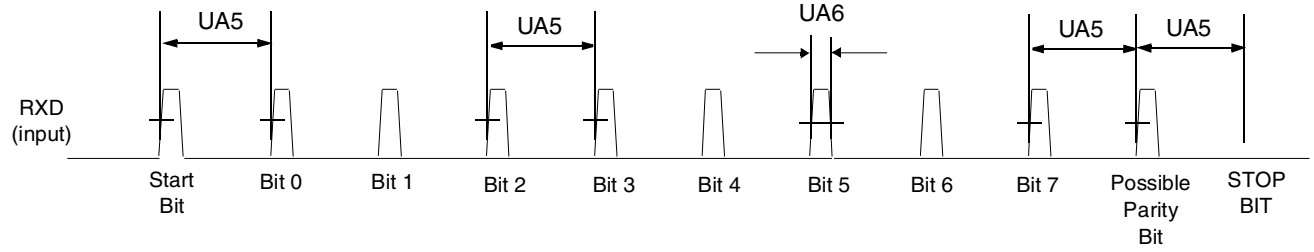

Figure 88. UART IrDA Mode Receive Timing Diagram

Table 90. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] - 1/(16 x F_{baud_rate})	$1/F_{baud\_rate}$ + 1/(16 x F_{baud_rate})	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 us	(5/16) x ($1/F_{baud\_rate}$)	—

1 The UART receiver can tolerate 1/(16 x F_{baud_rate}) tolerance in each bit. But accumulation tolerance in one frame must not exceed 3/(16 x F_{baud_rate}).

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.7.19.4 USB PHY Voltage Thresholds

Table 104 lists the USB PHY voltage thresholds.

Table 104. VBUS Comparators Thresholds

Parameter	Conditions	Min	Typ	Max	Unit
A-Device Session Valid	—	0.8	1.4	2.0	V
B-Device Session Valid	—	0.8	1.4	4.0	V
B-Device Session End	—	0.2	0.45	0.8	V
VBUS Valid Comparator Threshold[1]	—	4.4	4.6	4.75	V

1 For VBUS maximum rating, see Table 4 on page 16

4.7.19.5 USB PHY Termination

USB driver impedance in FS and HS modes is 45 Ω ±10% (steady state). No external resistors required.

4.8 XTAL Electrical Specifications

Table 105 shows the XTALOSC electrical specifications.

Table 106 shows the XTALOSC_32K electrical specifications.

Table 105. XTALOSC Electrical Specifications

Parameter	Min	Typ	Max	Units
Frequency	22	24	27	MHz

Table 106. XTALOSC_32K Electrical Specifications

Parameter	Min	Typ	Max	Units
Frequency	—	32.768/32.0[1]	—	kHz

1 Recommended nominal frequency 32.768 kHz.

4.9 Integrated LDO Voltage Regulators Parameters

The PLL supplies VDD_DIG_PLL and VDD_ANA_PLL can be powered ON from internal LDO voltage regulator (default case). In this case VDD_REG is used as internal regulator's power source. The regulator's output can be used as a supply for other domains such as VDDA and VDDAL1.

Table 107 shows the VDD_DIG_PLL and VDD_ANA_PLL Integrated Voltage Regulators Parameters.