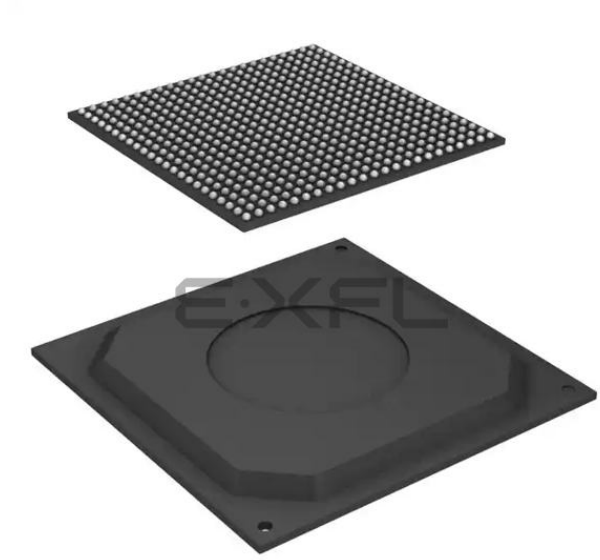

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR2, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	SATA 1.5Gbps (1)
USB	USB 2.0 (2), USB 2.0 + PHY (2)
Voltage - I/O	1.3V, 1.8V, 2.775V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	529-FBGA
Supplier Device Package	529-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx537cvv8cr2

Table 2. i.MX53 Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
ESDHCV3-3	Ultra-High-Speed eMMC / SD Host Controller	Connectivity Peripherals	Ultra high-speed eMMC / SD host controller, enhanced to support eMMC 4.4 standard specification, for 832 MBps. • Port 3 is specifically enhanced to support eMMC 4.4 specification, for double data rate (832 Mbps, 8-bit port). ESDHCV3 is backward compatible to ESDHCV2 and supports all the features of ESDHCV2 as described below.
ESDHCV2-1 ESDHCV2-2 ESDHCv2-4	Enhanced Multi-Media Card / Secure Digital Host Controller		Enhanced multimedia card / secure digital host controller • Ports 1, 2, and 4 are compatible with the “MMC System Specification” version 4.3, full support and supporting 1, 4 or 8-bit data. The generic features of the eSDHCv2 module, when serving as SD / MMC host, include the following: • Can be configured either as SD / MMC controller • Supports eSD and eMMC standard, for SD/MMC embedded type cards • Conforms to SD Host Controller Standard Specification, version 2.0, full support. • Compatible with the SD Memory Card Specification, version 1.1 • Compatible with the SDIO Card Specification, version 1.2 • Designed to work with SD memory, miniSD memory, SDIO, miniSDIO, SD Combo, MMC and MMC RS cards • Configurable to work in one of the following modes: —SD/SDIO 1-bit, 4-bit —MMC 1-bit, 4-bit, 8-bit • Full/high speed mode. • Host clock frequency variable between 32 kHz to 52 MHz • Up to 200 Mbps data transfer for SD/SDIO cards using 4 parallel data lines • Up to 416 Mbps data transfer for MMC cards using 8 parallel data lines
FEC	Fast Ethernet Controller	Connectivity Peripherals	The Ethernet media access controller (MAC) is designed to support both 10 Mbps and 100 Mbps Ethernet/IEEE Std 802.3™ networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The i.MX53 also consists of HW assist for IEEE1588™ standard. See, TSU and CE_RTC (IEEE1588) section for more details.
FIRI	Fast Infrared Interface	Connectivity Peripherals	Fast infrared interface
FLEXCAN-1 FLEXCAN-2	Flexible Controller Area Network	Connectivity Peripherals	The controller area network (CAN) protocol was primarily, but not exclusively, designed to be used as a vehicle serial data bus. Meets the following specific requirements of this application: real-time processing, reliable operation in the EXTMC environment of a vehicle, cost-effectiveness and required bandwidth. The FLEXCAN is a full implementation of the CAN protocol specification, Version 2.0 B (ISO 11898), which supports both standard and extended message frames at 1 Mbps.

Table 13. DDR3 I/O DC Electrical Parameters (continued)

Over/undershoot peak	Vpeak	—	—	—	0.4	V
Over/undershoot area (above OVDD or below OVSS)	Varea	—	—	—	0.67	V-ns
Termination Voltage	Vtt	Vtt tracking OVDD/2	0.49 x OVDD	Vref	0.51 x OVDD	V
Input current (no pull-up/down)	Iin	VI = 0 V VI=OVDD	— —	— —	1 1	µA
Pull-up/Pull-down impedance mismatch	—	Minimum impedance configuration	—	—	3	Ω
240 Ω unit calibration resolution	—	—	—	—	10	Ω
Keeper Circuit Resistance	—	—	—	130[4]	—	kΩ

1 OVDD— I/O power supply (1.425 V–1.575 V for DDR3)

2 Vref— DDR3 external reference voltage

3 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

4 Use an off-chip pull resistor of less than 60 kΩ to override this keeper.

4.3.3 Low Voltage I/O (LVIO) DC Parameters

The parameters in Table 14 are guaranteed per the operating ranges in Table 6, unless otherwise noted. The LVIO pads operate only as inputs.

Table 14. LVIO DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
High-Level DC input voltage[1, 2]	Vih	Ioh = -0.8 mA	0.7 × OVDD	—	OVDD	V
Low-Level DC input voltage[1, 2]	Vil	Iol = 0.8 mA	0	—	0.3 × OVDD	V
Input Hysteresis	Vhys	OVDD = 1.875 V OVDD = 2.775 V	0.35	0.62 1.27	—	V
Schmitt trigger VT+[2, 3]	VT+	—	0.5 × OVDD	—	—	V
Schmitt trigger VT-[2, 3]	VT-	—	—	—	0.5 × OVDD	V
Input current (no pull-up/down)	Iin	Vin = OVDD or 0 V	—	—	1	µA
Input current (22 kΩ Pull-up)	Iin	Vin = 0 V Vin = OVDD	—	—	161 1	µA
Input current (47 kΩ Pull-up)	Iin	Vin = 0 V Vin = OVDD	—	—	76 1	µA
Input current (100 kΩ Pull-up)	Iin	Vin = 0 V Vin = OVDD	—	—	36 1	µA
Input current (100 kΩ Pull-down)	Iin	Vin = 0 V Vin = OVDD	—	—	1 36	µA
Keeper Circuit Resistance	—		—	130[4]	—	kΩ

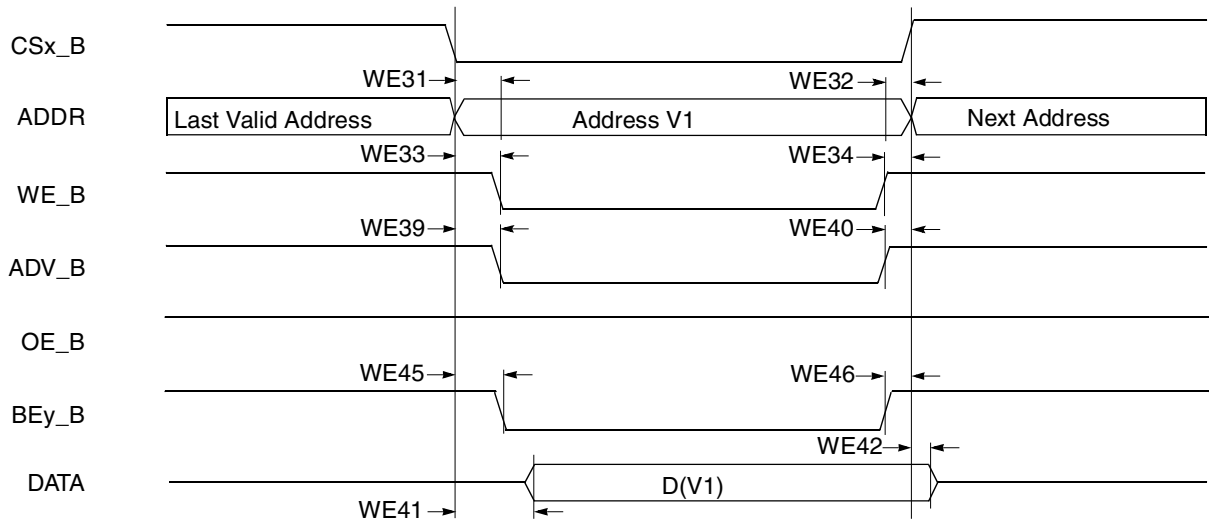

Figure 24. Asynchronous Memory Write Access

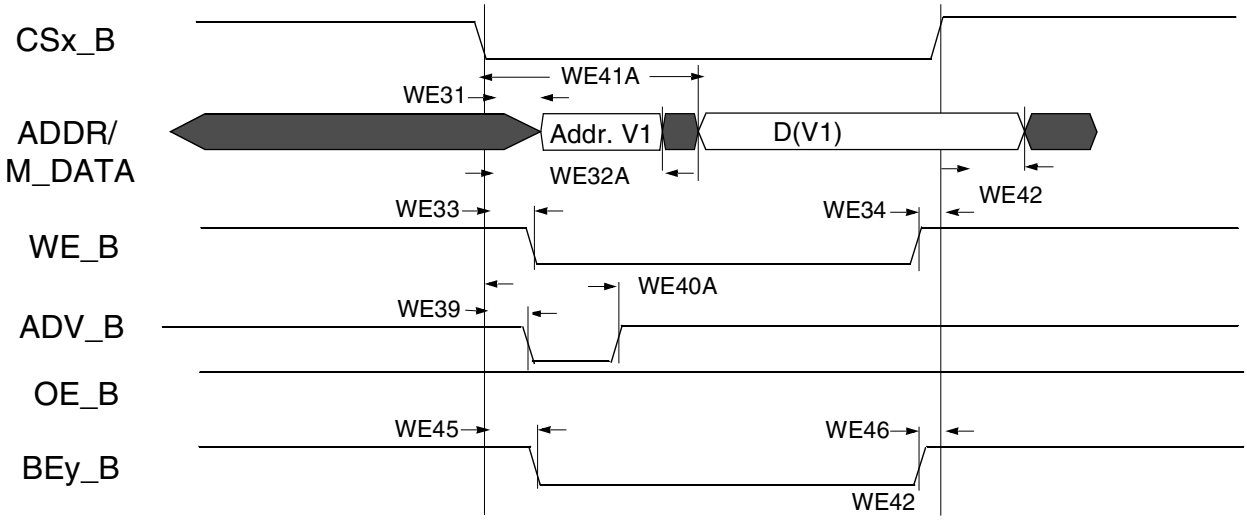

Figure 25. Asynchronous A/D Muxed Write Access

Table 45. CSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time	t_{clk}	60	—	ns
CS2	SCLK High or Low Time	t_{SW}	26	—	ns
CS3	SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	SSx pulse width	t_{CSLH}	26	—	ns
CS5	SSx Lead Time (Slave Select setup time)	t_{SCS}	26	—	ns
CS6	SSx Lag Time (SS hold time)	t_{HCS}	26	—	ns
CS7	MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-1	21	ns
CS8	MISO Setup Time	t_{Smiso}	5	—	ns
CS9	MISO Hold Time	t_{Hmiso}	5	—	ns
CS10	RDY to SSx Time[2]	t_{SDRY}	5	—	ns

1 See specific I/O AC parameters Section 4.5, "I/O AC Parameters"

2 SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.7.2.2 CSPI Slave Mode Timing

Figure 33 depicts the timing of CSPI in slave mode. Timing characteristics were not available at the time of publication.

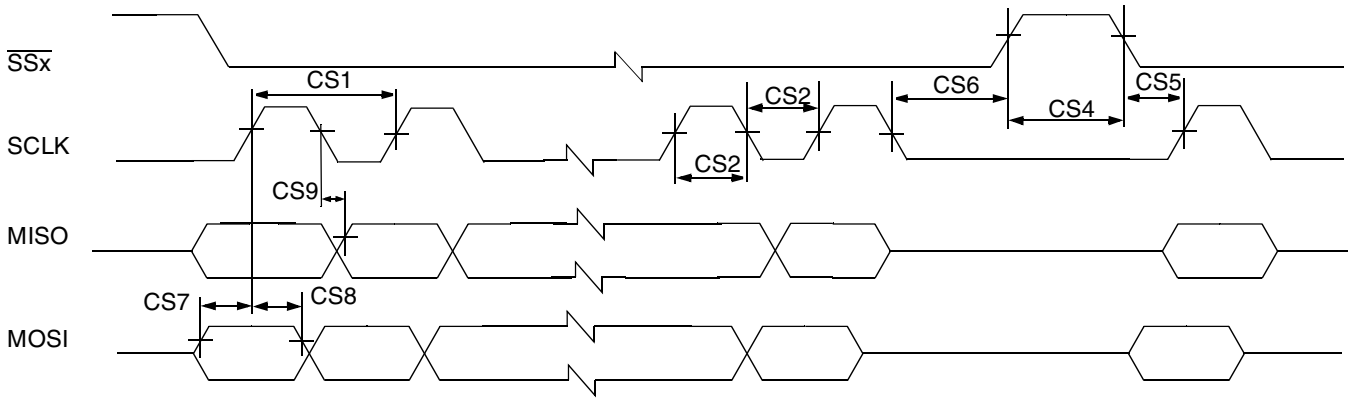

Figure 33. CSPI/ECSPI Slave Mode Timing Diagram

6 The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but it spreads from one serial clock before the first bit clock (like the bit length frame sync signal), until the second-to-last bit clock of the first word in the frame.

7 Periodically sampled and not 100% tested.

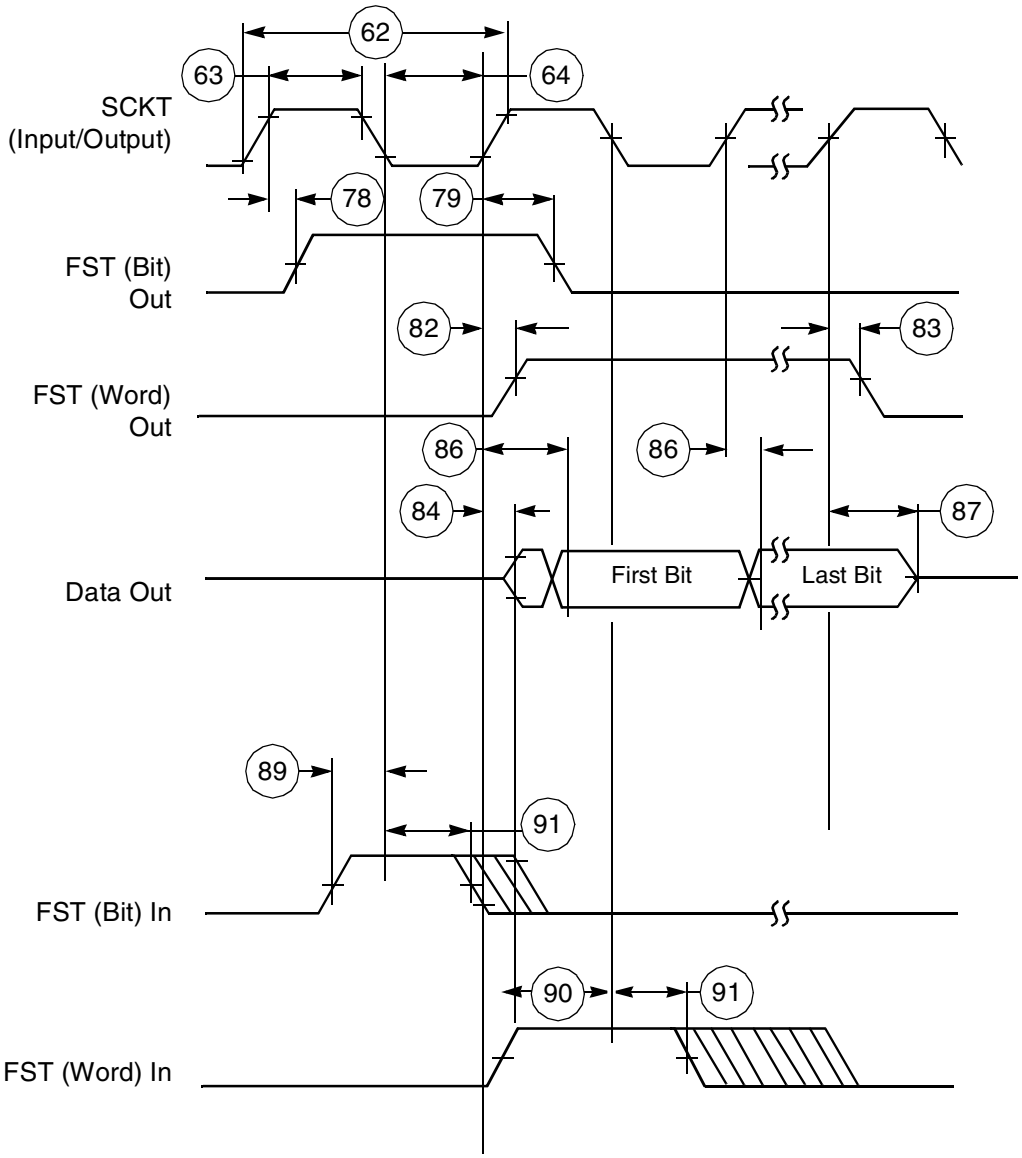

Figure 34. ESAI Transmitter Timing

4.7.8 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: sensor image signal processing, display processing, image conversions, and other related functions.
- Synchronization and control capabilities, such as avoidance of tearing artifacts.

4.7.8.1 IPU Sensor Interface Signal Mapping

The IPU supports a number of sensor input formats. Table 57 defines the mapping of the Sensor Interface Pins used for various supported interface formats.

Table 57. Camera Input Signal Cross Reference, Format and Bits Per Cycle

Signal Name[1]	RGB565 8 bits 2 cycles	RGB565[2] 8 bits 3 cycles	RGB666[3] 8 bits 3 cycles	RGB888 8 bits 3 cycles	YCbCr[4] 8 bits 2 cycles	RGB565[5] 16 bits 2 cycles	YCbCr[6] 16 bits 1 cycle	YCbCr[7] 16 bits 1 cycle	YCbCr[8] 20 bits 1 cycle
CSIx_DAT0	—	—	—	—	—	—	—	0	C[0]
CSIx_DAT1	—	—	—	—	—	—	—	0	C[1]
CSIx_DAT2	—	—	—	—	—	—	—	C[0]	C[2]
CSIx_DAT3	—	—	—	—	—	—	—	C[1]	C[3]
CSIx_DAT4	—	—	—	—	—	B[0]	C[0]	C[2]	C[4]
CSIx_DAT5	—	—	—	—	—	B[1]	C[1]	C[3]	C[5]
CSIx_DAT6	—	—	—	—	—	B[2]	C[2]	C[4]	C[6]
CSIx_DAT7	—	—	—	—	—	B[3]	C[3]	C[5]	C[7]
CSIx_DAT8	—	—	—	—	—	B[4]	C[4]	C[6]	C[8]
CSIx_DAT9	—	—	—	—	—	G[0]	C[5]	C[7]	C[9]
CSIx_DAT10	—	—	—	—	—	G[1]	C[6]	0	Y[0]
CSIx_DAT11	—	—	—	—	—	G[2]	C[7]	0	Y[1]
CSIx_DAT12	B[0], G[3]	R[2],G[4],B[2]	R/G/B[4]	R/G/B[0]	Y/C[0]	G[3]	Y[0]	Y[0]	Y[2]
CSIx_DAT13	B[1], G[4]	R[3],G[5],B[3]	R/G/B[5]	R/G/B[1]	Y/C[1]	G[4]	Y[1]	Y[1]	Y[3]
CSIx_DAT14	B[2], G[5]	R[4],G[0],B[4]	R/G/B[0]	R/G/B[2]	Y/C[2]	G[5]	Y[2]	Y[2]	Y[4]
CSIx_DAT15	B[3], R[0]	R[0],G[1],B[0]	R/G/B[1]	R/G/B[3]	Y/C[3]	R[0]	Y[3]	Y[3]	Y[5]
CSIx_DAT16	B[4], R[1]	R[1],G[2],B[1]	R/G/B[2]	R/G/B[4]	Y/C[4]	R[1]	Y[4]	Y[4]	Y[6]
CSIx_DAT17	G[0], R[2]	R[2],G[3],B[2]	R/G/B[3]	R/G/B[5]	Y/C[5]	R[2]	Y[5]	Y[5]	Y[7]
CSIx_DAT18	G[1], R[3]	R[3],G[4],B[3]	R/G/B[4]	R/G/B[6]	Y/C[6]	R[3]	Y[6]	Y[6]	Y[8]
CSIx_DAT19	G[2], R[4]	R[4],G[5],B[4]	R/G/B[5]	R/G/B[7]	Y/C[7]	R[4]	Y[7]	Y[7]	Y[9]

[1] CSIx stands for CSI1 or CSI2.

4.7.8.6 Synchronous Interfaces to Standard Active Matrix TFT LCD Panels

4.7.8.6.1 IPU Display Operating Signals

The IPU uses four control signals and data to operate a standard synchronous interface:

- IPP_DISP_CLK—Clock to display
- HSYNC—Horizontal synchronization
- VSYNC—Vertical synchronization
- DRDY—Active data

All synchronous display controls are generated on the base of an internally generated “local start point”. The synchronous display controls can be placed on time axis with DI’s offset, up and down parameters. The display access can be whole number of DI clock (Tdiclk) only. The IPP_DATA can not be moved relative to the local start point. The data bus of the synchronous interface is output direction only.

4.7.8.6.2 LCD Interface Functional Description

Figure 47 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DI_CLK internal DI clock, used for calculation of other controls.
- IPP_DISP_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, IPP_DISP_CLK runs continuously.
- HSYNC causes the panel to start a new line. (Usually IPP_PIN_2 is used as HSYNC.)
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse. (Usually IPP_PIN_3 is used as VSYNC.)
- DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.
(DRDY can be used either synchronous or asynchronous generic purpose pin as well.)

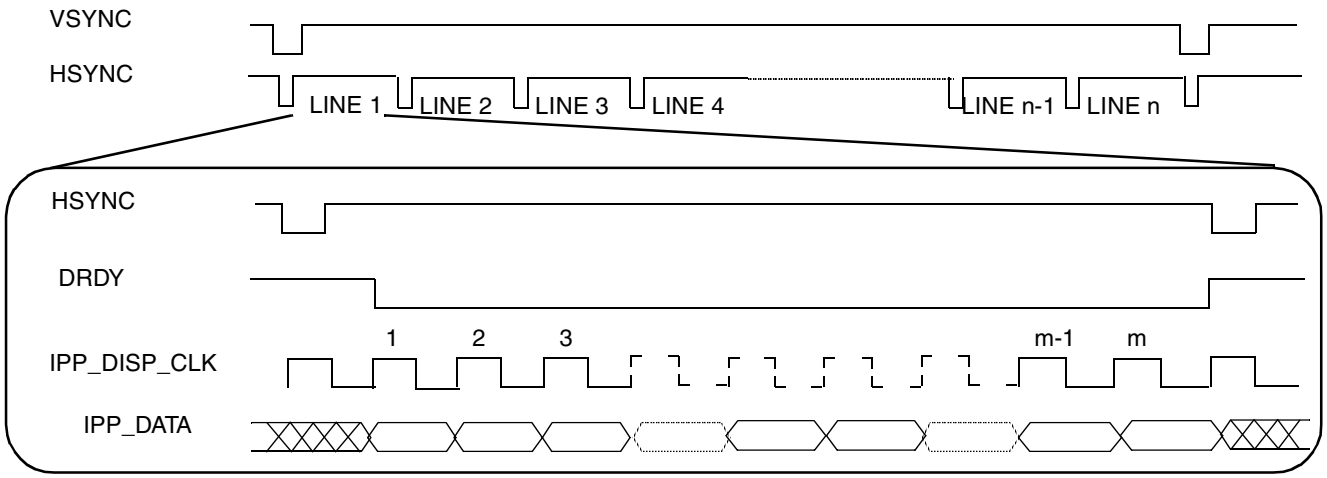

Figure 47. Interface Timing Diagram for TFT (Active Matrix) Panels

4.7.8.6.3 TFT Panel Sync Pulse Timing Diagrams

Figure 48 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All the parameters shown in the figure are programmable. All controls are started by corresponding internal events—local start points. The timing diagrams correspond to inverse polarity of the IPP_DISP_CLK signal and active-low polarity of the HSYNC, VSYNC, and DRDY signals.

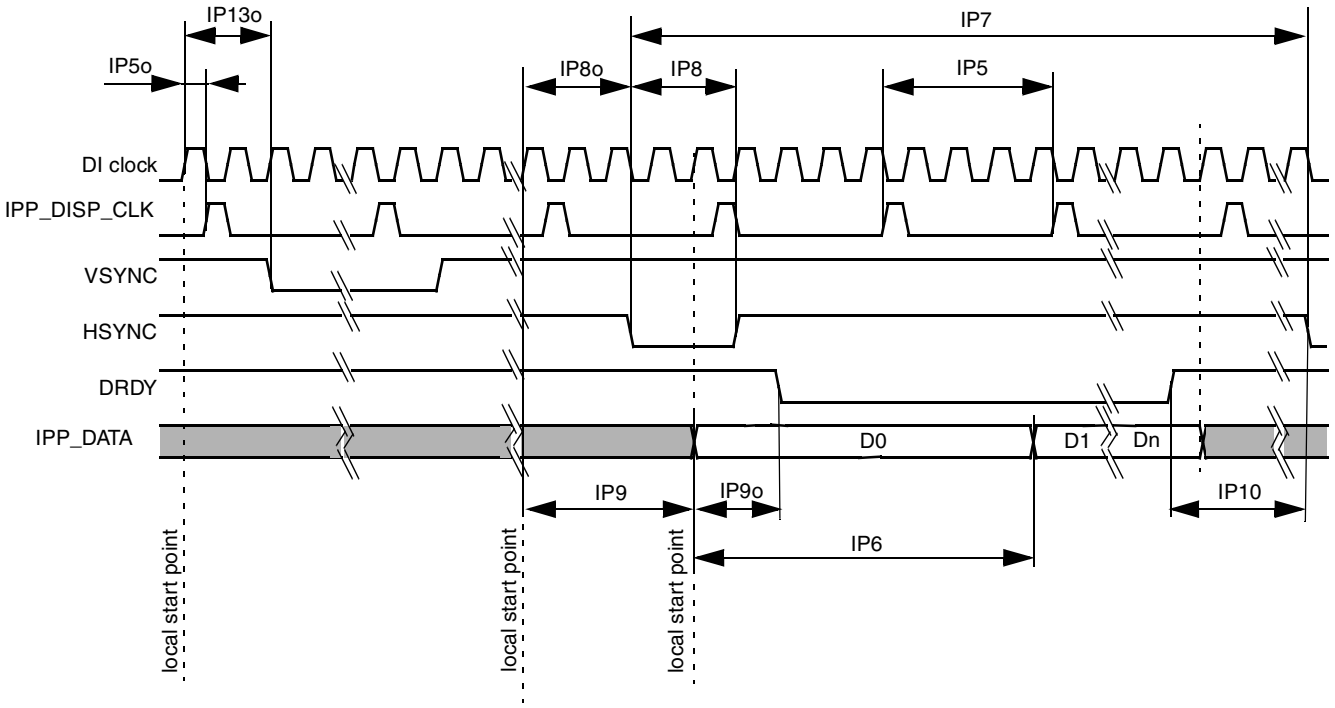

Figure 48. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 49 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.

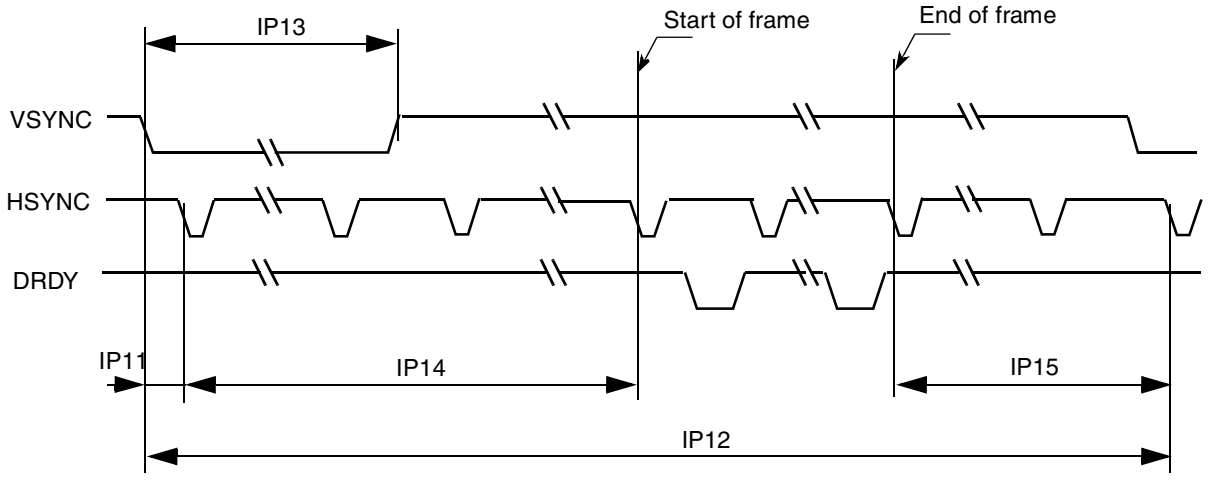

Figure 49. TFT Panels Timing Diagram—Vertical Sync Pulse

4.7.8.7.1 TVEv2 TV Encoder Performance Specifications

The TV encoder output specifications are shown in Table 62. All the parameters in the table are defined under the following conditions:

- R_{set} = 1.05 kΩ ±1%, resistor on TVDAC_VREF pin to GND
- R_{load} = 37.5 Ω ±1%, output load to the GND

Table 62. TV Encoder Video Performance Specifications

Parameter	Conditions	Min	Typ	Max	Unit
DAC STATIC PERFORMANCE					
Resolution[1]	—	—	10	—	Bits
Integral Nonlinearity (INL)[2]	—	—	1	2	LSBs
Differential Nonlinearity (DNL) [2]	—	—	0.6	1	LSBs
Channel-to-channel gain matching[2]	—	—	2	—	%
Full scale output voltage[2]	R_{set} = 1.05 kΩ ±1% R_{load} = 37.5 Ω ±1%	1.24	1.306	1.37	V
DAC DYNAMIC PERFORMANCE					
Spurious Free Dynamic Range (SFDR)	F_{out} = 3.38 MHz F_{samp} = 216 MHz	—	59	—	dBc
Spurious Free Dynamic Range (SFDR)	F_{out} = 8.3 MHz F_{samp} = 297 MHz	—	54	—	dBc
VIDEO PERFORMANCE IN SD MODE[2]					
Short Term Jitter (Line to Line)	—	—	2.5	—	±ns
Long Term Jitter (Field to Field)	—	—	3.5	—	±ns
Frequency Response	0–4.0 MHz	-0.1	—	0.1	dB
	5.75 MHz	-0.7	—	0	dB
Luminance Nonlinearity	—	—	0.5	—	±%
Differential Gain	—	—	0.35	—	%
Differential Phase	—	—	0.6	—	Degrees
Signal-to-Noise Ratio (SNR)	Flat field full bandwidth	—	75	—	dB
Hue Accuracy	—	—	0.8	—	±Degrees
Color Saturation Accuracy	—	—	1.5	—	±%
Chroma AM Noise	—	—	-70	—	dB
Chroma PM Noise	—	—	-47	—	dB
Chroma Nonlinear Phase	—	—	0.5	—	±Degrees
Chroma Nonlinear Gain	—	—	2.5	—	±%
Chroma/Luma Intermodulation	—	—	0.1	—	±%
Chroma/Luma Gain Inequality	—	—	1.0	—	±%

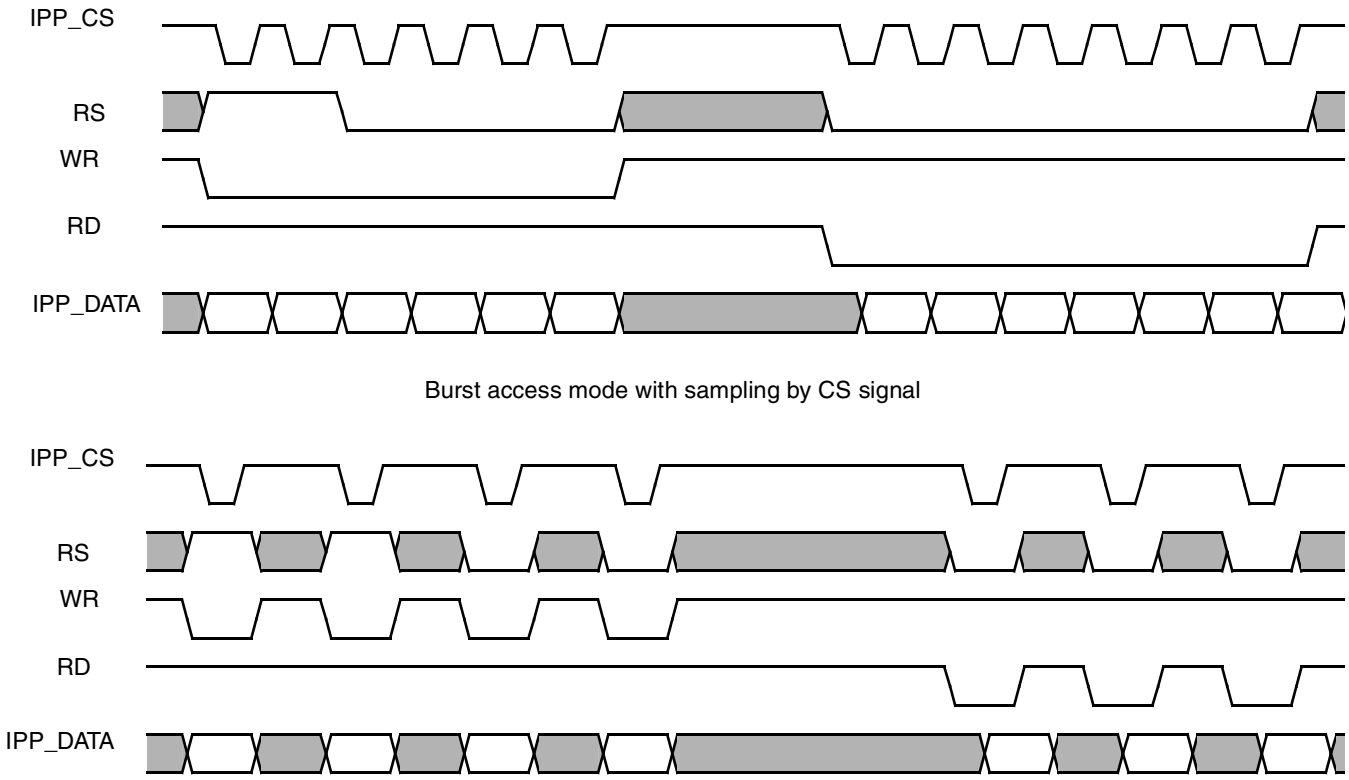

Figure 52. Asynchronous Parallel System 80 Interface (Type 1) Timing Diagram

In the timing equations, some timing parameters are used. These parameters depend on the implementation of the i.MX53 PATA interface on silicon, the bus buffer used, the cable delay and cable skew. Table 70 shows ATA timing parameters.

Table 70. PATA Timing Parameters

Name	Description	Value/ Contributing Factor[1]
T	Bus clock period (AHB_CLK_ROOT)	Peripheral clock frequency (7.5 ns for 133 MHz clock)
ti_ds	Set-up time ata_data to ata_iordy edge (UDMA-in only) UDMA0 UDMA1 UDMA2, UDMA3 UDMA4 UDMA5	 15 ns 10 ns 7 ns 5 ns 4 ns
ti_dh	Hold time ata_iordy edge to ata_data (UDMA-in only) UDMA0, UDMA1, UDMA2, UDMA3, UDMA4 UDMA5	 5.0 ns 4.6 ns
tco	Propagation delay bus clock L-to-H to ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data, ata_buffer_en	12.0 ns
tsu	Set-up time ata_data to bus clock L-to-H	8.5 ns
tsui	Set-up time ata_iordy to bus clock H-to-L	8.5 ns
thi	Hold time ata_iordy to bus clock H to L	2.5 ns
tskew1	Max difference in propagation delay bus clock L-to-H to any of following signals ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en	7 ns
tskew2	Max difference in buffer propagation delay for any of following signals: ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en	Transceiver
tskew3	Max difference in buffer propagation delay for any of following signals ata_iordy, ata_data (read)	Transceiver
tbuf	Max buffer propagation delay	Transceiver
tcable1	Cable propagation delay for ata_data	Cable
tcable2	Cable propagation delay for control signals ata_dior, ata_diow, ata_iordy, ata_dmack	Cable
tskew4	Max difference in cable propagation delay between ata_iordy and ata_data (read)	Cable
tskew5	Max difference in cable propagation delay between (ata_dior, ata_diow, ata_dmack) and ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_data(write)	Cable
tskew6	Max difference in cable propagation delay without accounting for ground bounce	Cable

[1] Values provided where applicable.

Table 75. UDMA Out Burst Timing Parameters (continued)

ATA Parameter	Parameter from Figure 71, Figure 72, Figure 73	Value	Controlling Variable
trfs1	trfs	trfs = 1.6 × T + tsui + tco + tbuf + tbuf	—
—	tdzfs	tdzfs = time_dzfs × T - (tskew1)	time_dzfs
tss	tss	tss = time_ss × T - (tskew1 + tskew2)	time_ss
tmli	tdzfs_mli	tdzfs_mli =max (time_dzfs, time_mli) × T - (tskew1 + tskew2)	—
tli	tli1	tli1 > 0	—
tli	tli2	tli2 > 0	—
tli	tli3	tli3 > 0	—
tcvh	tcvh	tcvh = (time_cvh ×T) - (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on × T - tskew1 toff = time_off × T - tskew1	—

4.7.13 SATA PHY Parameters

This section describes SATA PHY electrical specifications.

4.7.13.1 Reference Clock Electrical and Jitter Specifications

The refclk signal is differential and supports frequencies of 25 MHz or 50-156.25 MHz (100 MHz and 125 MHz are common frequencies). The frequency is pin-selectable (for more information about the signal, see “Per-Transceiver Control and Status Signals” in the SATA PHY chapter in the Reference Manual).

Table 76 provides the SATA PHY reference clock specifications.

Table 76. Reference Clock Specifications

Parameters	Test Conditions	Min	Max	Unit
Differential peak voltage (typically 0.71 V)	—	350	850	mV
Common mode voltage (refclk_p + refclk_m) / 2	—	175	2,000	mV
Total phase jitter	For information about total phase jitter, see following section	—	3	ps RMS
Minimum/maximum duty cycle	—	40	60	% UI
Frequency range	—	25	156.25	MHz

4.7.13.2.2 SATA PHY Receiver Characteristics

Table 78 provides specifications for SATA PHY receiver characteristics.

Table 78. SATA PHY Receiver Characteristics

Parameters	Symbol	Min	Typ	Max	Unit
Minimum Rx eye height (differential peak-to-peak)	$V_{MIN\_RX\_EYE\_HEIGHT}$	—	—	175	mV
Tolerance	PPM	-400	—	400	ppm

4.7.13.3 SATA_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 191 Ω 1% precision resistor on SATA_REXT pad to ground.

Resistor calibration consists of learning which state of the internal Resistor Calibration register causes an internal, digitally trimmed calibration resistor to best match the impedance applied to the SATA_REXT pin. The calibration register value is then supplied to all Tx and Rx termination resistors.

During the calibration process (for a few tens of microseconds), up to 0.3 mW can be dissipated in the external SATA_REXT resistor. At other times, no power is dissipated by the SATA_REXT resistor.

4.7.13.4 SATA Connectivity When Not in Use

NOTE

The Temperature Sensor is part of the SATA module. If SATA IP is disabled, the Temperature Sensor will not work as well. Temperature Sensor functionality is important in supporting high performance applications without overheating the device (at high ambient temp).

When both SATA and thermal sensor are not required, connect VP and VPH supplies to ground. The rest of the ports, both inputs and outputs (SATA_REFCLKM, SATA_REFCLKP, SATA_REXT, SATA_RXM, SATA_RXP, SATA_TXM) can be left floating. It is not recommended to turn off the VPH while the VP is active.

When SATA is not in use but thermal sensor is still required, both VP and VPH supplies must be powered on according to their nominal voltage levels. The reference clock input frequency must fall within the specified range of 25 MHz to 156.25 MHz. SATA_REXT does not need to be connected, as the termination impedance is not of consequence.

Table 79. JTAG Timing (continued)

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ9	TMS, TDI data hold time	25	—	ns
SJ10	TCK low to TDO data valid	—	44	ns
SJ11	TCK low to TDO high impedance	—	44	ns
SJ12	$\overline{\text{TRST}}$ assert time	100	—	ns
SJ13	$\overline{\text{TRST}}$ set-up time to TCK low	40	—	ns

1 T_{DC} = target frequency of SJC
2 V_M = mid-point voltage

4.7.15 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 80 and Figures , show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SRCK) for SPDIF in Rx mode and the timing of the modulating Tx clock (STCLK) for SPDIF in Tx mode.

Table 80. SPDIF Timing Parameters

Characteristics	Symbol	Timing Parameter Range		Units
		Min	Max	
SPDIFIN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIFOUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIFOUT1 output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SRCK) period	srckp	40.0	—	ns
SRCK high period	srckph	16.0	—	ns
SRCK low period	srckpl	16.0	—	ns
Modulating Tx clock (STCLK) period	stclkp	40.0	—	ns
STCLK high period	stclkph	16.0	—	ns
STCLK low period	stclkpl	16.0	—	ns

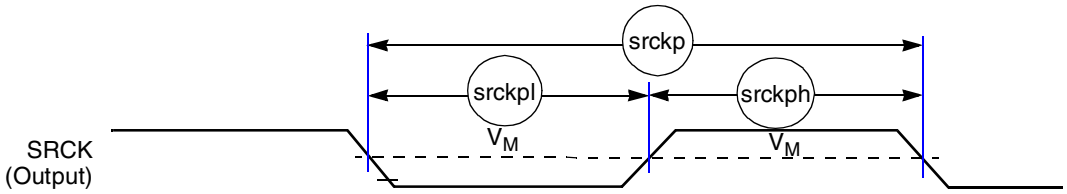

Figure 79. SPDIF Timing Diagram

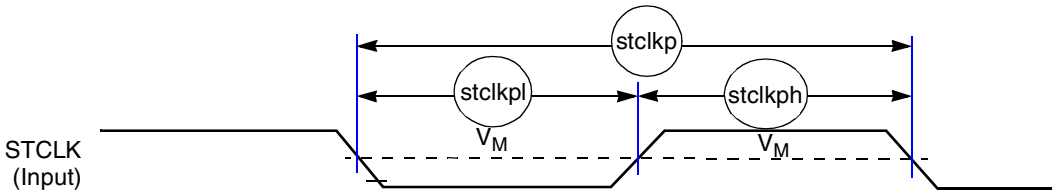

Figure 80. STCLK Timing

4.7.16 SSI Timing Parameters

This section describes the timing parameters of the SSI module. The connectivity of the serial synchronous interfaces are summarized in Table 81.

Table 81. AUDMUX Port Allocation

Port	Signal Nomenclature	Type and Access
AUDMUX port 1	SSI 1	Internal
AUDMUX port 2	SSI 2	Internal
AUDMUX port 3	AUD3	External— AUD3 I/O
AUDMUX port 4	AUD4	External— EIM or CSPI1 I/O through IOMUXC
AUDMUX port 5	AUD5	External— EIM or SD1 I/O through IOMUXC
AUDMUX port 6	AUD6	External— EIM or DISP2 through IOMUXC
AUDMUX port 7	SSI 3	Internal

NOTE

- The terms WL and BL used in the timing diagrams and tables refer to Word Length (WL) and Bit Length (BL).
- The SSI timing diagrams use generic signal names wherein the names used in the i.MX53 Reference Manual are channel specific signal names. For example, a channel clock referenced in the IOMUXC chapter as AUD3_TXC appears in the timing diagram as TXC.

4.7.16.3 SSI Transmitter Timing with External Clock

Figure 83 depicts the SSI transmitter external clock timing and Table 84 lists the timing parameters for the transmitter timing with the external clock

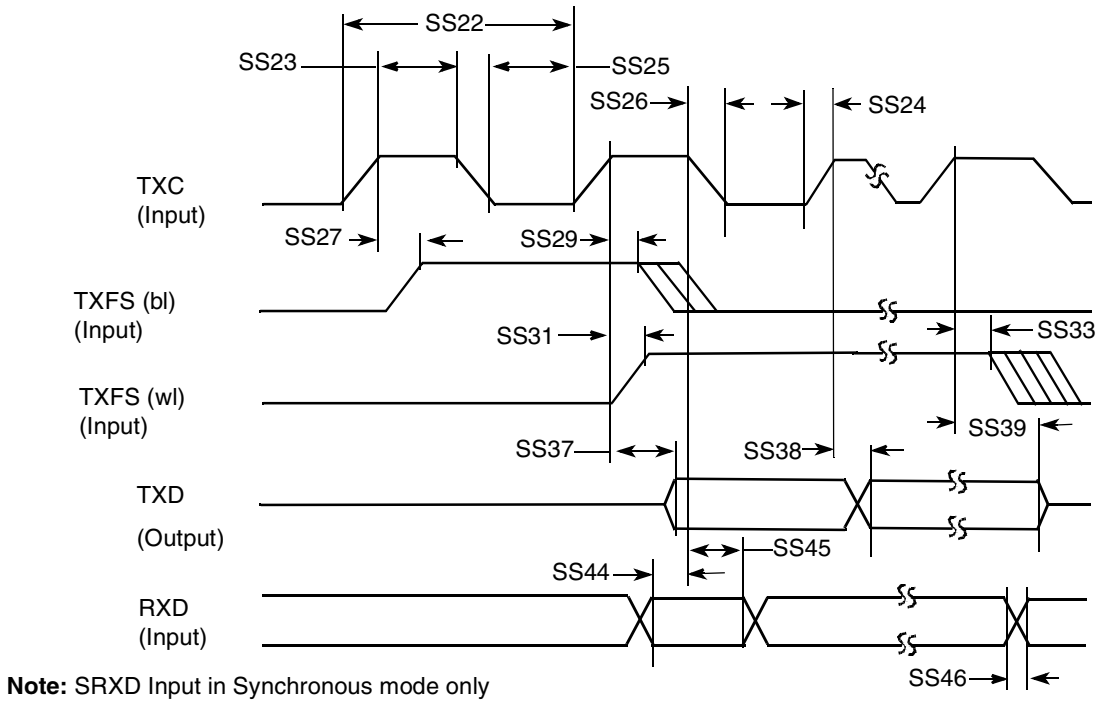

Figure 83. SSI Transmitter External Clock Timing Diagram

Table 84. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	-10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	-10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns

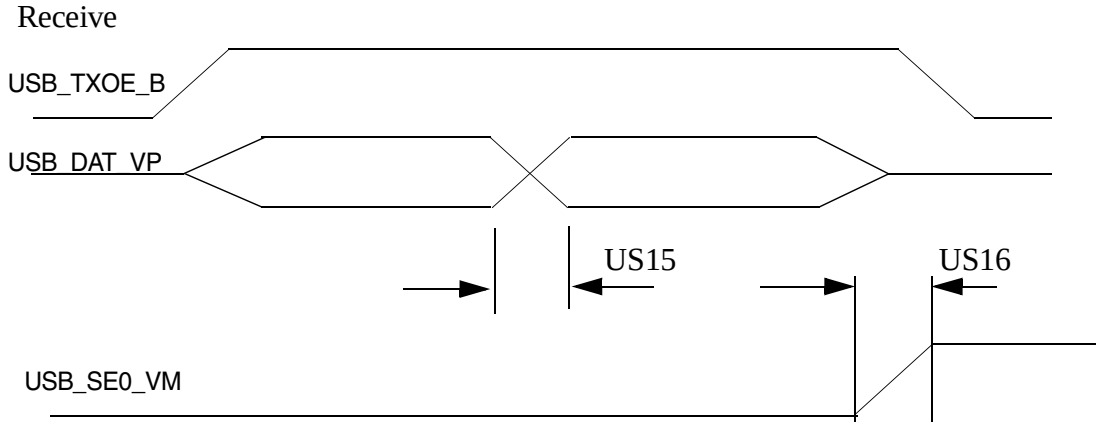

Figure 92. USB Receive Waveform in DAT_SE0 Unidirectional Mode

Table 94. USB Port Timing Specification in DAT_SE0 Unidirectional Mode

No.	Parameter	Signal Name	Signal Source	Min	Max	Unit	Condition / Reference Signal
US9	TX Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US10	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US11	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US12	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US15	RX Rise/Fall Time	USB_VP1	In	—	3.0	ns	35 pF
US16	RX Rise/Fall Time	USB_VM1	In	—	3.0	ns	35 pF

Table 108. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at Reset	eFUSE Name	Details
EIM_A22	Input	BOOT_CFG1[7]/Test Mode Selection	Boot Options, Pin value overrides fuse settings for **BT_FUSE_SEL = '0'**. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.
EIM_A21	Input	BOOT_CFG1[6]/Test Mode Selection	
EIM_A20	Input	BOOT_CFG1[5]/Test Mode Selection	
EIM_A19	Input	BOOT_CFG1[4]	
EIM_A18	Input	BOOT_CFG1[3]	
EIM_A17	Input	BOOT_CFG1[2]	
EIM_A16	Input	BOOT_CFG1[1]	
EIM_LBA	Input	BOOT_CFG1[0]	
EIM_EB0	Input	BOOT_CFG2[7]	
EIM_EB1	Input	BOOT_CFG2[6]	
EIM_DA0	Input	BOOT_CFG2[5]	
EIM_DA1	Input	BOOT_CFG2[4]	
EIM_DA2	Input	BOOT_CFG2[3]	
EIM_DA3	Input	BOOT_CFG2[2]	
EIM_DA4	Input	BOOT_CFG3[7]	
EIM_DA5	Input	BOOT_CFG3[6]	
EIM_DA6	Input	BOOT_CFG3[5]	
EIM_DA7	Input	BOOT_CFG3[4]	
EIM_DA8	Input	BOOT_CFG3[3]	
EIM_DA9	Input	BOOT_CFG3[2]	
EIM_DA10	Input	BOOT_CFG3[1]	

5.2 Boot Devices Interfaces Allocation

Table 109 lists the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 109. Interfaces Allocation During Boot

Interface	IP Instance	Allocated Pads During Boot	Comment
SPI	CSPI	EIM_A25, EIM_D21, EIM_D22, EIM_D28	Only SS1 is supported
SPI	ECSPI-1	EIM_D[19:16]	Only SS1 is supported
SPI	ECSPI-2	CSI_DAT[10:8], EIM_LBA	Only SS1 is supported

Table 111. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config. Value
DISP0_DAT20	F4	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[14]	Input	100 KΩ PU
DISP0_DAT21	C1	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[15]	Input	100 KΩ PU
DISP0_DAT22	E3	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[16]	Input	100 KΩ PU
DISP0_DAT23	C3	NVCC_LCD	GPIO	ALT1	GPIO-5	gpio5_GPIO[17]	Input	100 KΩ PU
DISP0_DAT3	F1	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[24]	Input	100 KΩ PD
DISP0_DAT4	G2	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[25]	Input	100 KΩ PD
DISP0_DAT5	H3	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[26]	Input	100 KΩ PD
DISP0_DAT6	G1	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[27]	Input	100 KΩ PD
DISP0_DAT7	H6	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[28]	Input	100 KΩ PD
DISP0_DAT8	G6	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[29]	Input	100 KΩ PU
DISP0_DAT9	E2	NVCC_LCD	GPIO	ALT1	GPIO-4	gpio4_GPIO[30]	Input	100 KΩ PU
DRAM_A0	M19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[0]	Output	Low
DRAM_A1	L21	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[1]	Output	Low
DRAM_A10	K19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[10]	Output	Low
DRAM_A11	L22	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[11]	Output	Low
DRAM_A12	L20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[12]	Output	Low
DRAM_A13	L23	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[13]	Output	Low
DRAM_A14	N18	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[14]	Output	Low
DRAM_A15	M18	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[15]	Output	Low
DRAM_A2	M20	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_A[2]	Output	Low

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