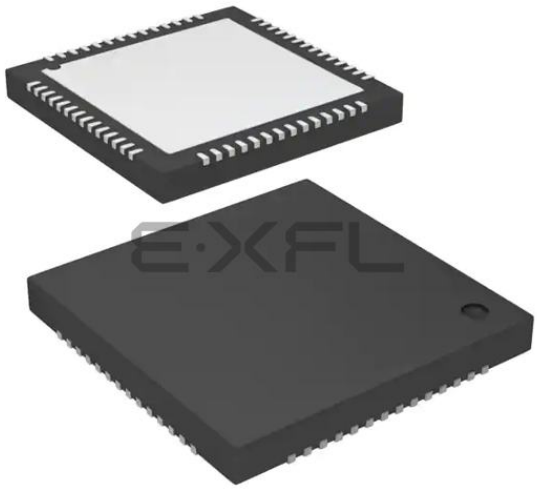

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Intelligent LED Driver
Core Processor	M8C
Program Memory Type	FLASH (16KB)
Controller Series	CY8CLED
RAM Size	1K x 8
Interface	DALI, DMX512, I²C, IrDA, SPI, UART/USART
Number of I/O	14
Voltage - Supply	4.75V ~ 5.25V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad
Supplier Device Package	56-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8cled01d01-56ltxi

3. Logic Block Diagrams

Figure 3-1. CY8CLED04D0x Logic Block Diagram

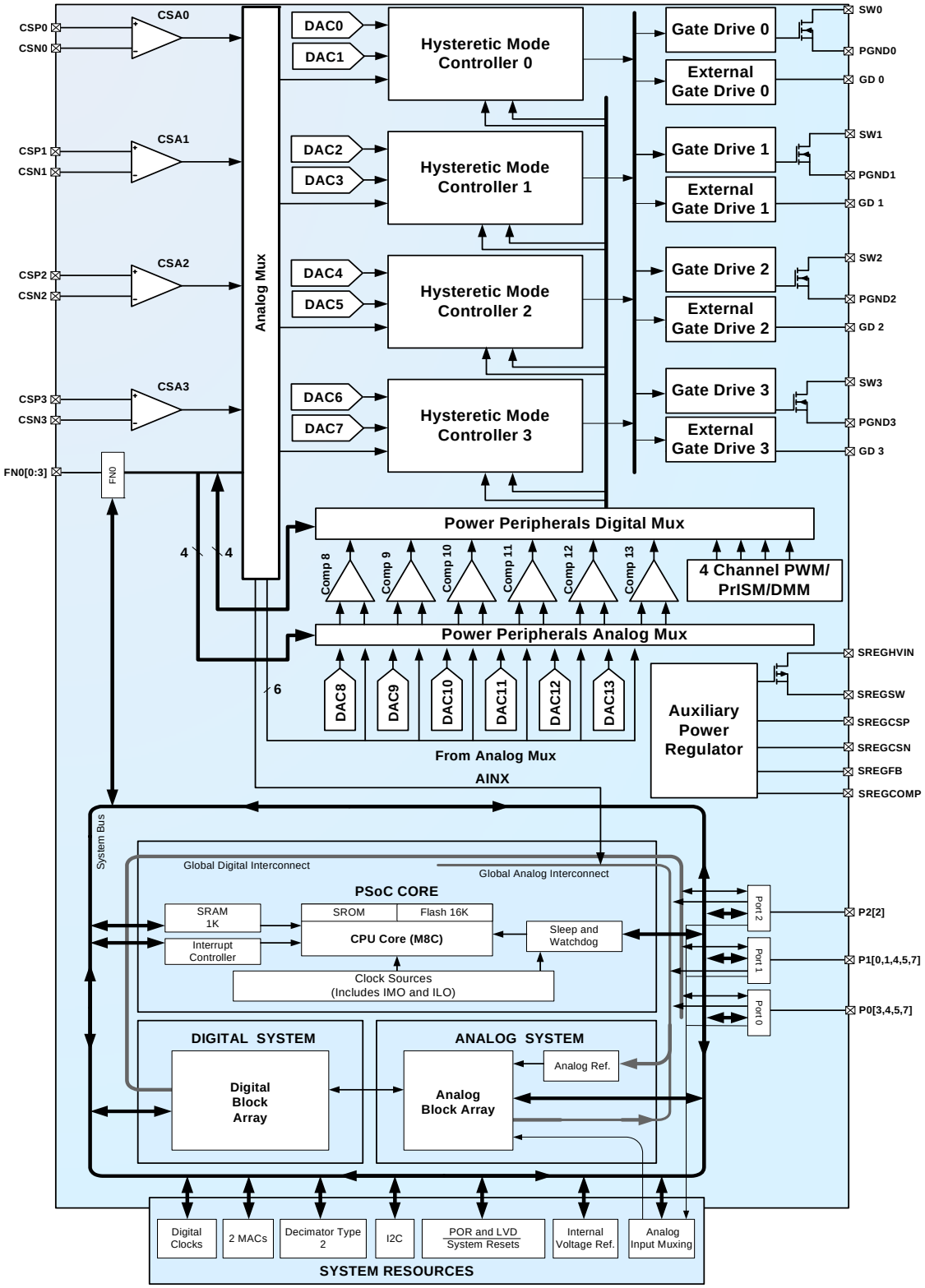
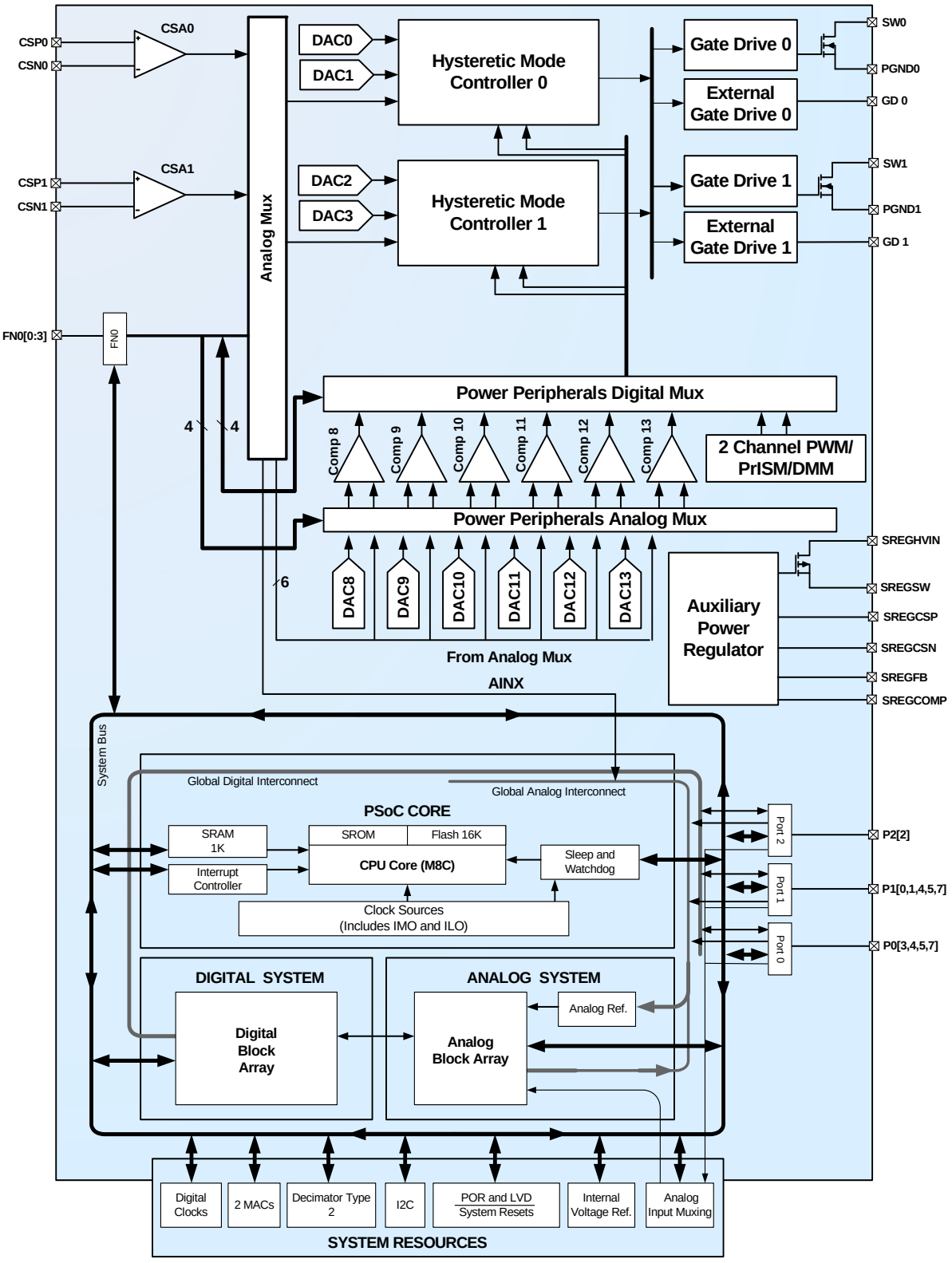


Figure 3-5. CY8CLED02D01 Logic Block Diagram



4. PowerPSoC® Functional Overview

The PowerPSoC family incorporates programmable system-on-chip technology with the best in class power electronics controllers and switching devices to create easy to use power-system-on-chip solutions for lighting applications.

All PowerPSoC family devices are designed to replace traditional MCUs, system ICs, and the numerous discrete components that surround them. PowerPSoC devices feature high performance power electronics including 1 ampere 2 MHz power FETs, hysteretic controllers, current sense amplifiers, and PrISM/PWM modulators to create a complete power electronics solution for LED power management. Configurable power, analog, digital, and interconnect circuitry enables a high level of integration in a host of industrial, commercial, and consumer LED lighting applications.

This architecture integrates programmable analog and digital blocks to enable you to create customized peripheral configurations that match the requirements of each individual application. Additionally, the device includes a 24 MHz CPU, Flash program memory, SRAM data memory, and configurable I/O in a range of convenient pinouts and packages.

The PowerPSoC architecture, as illustrated in the block diagrams, consists of five main areas: PSoC core, digital system, analog system, system resources, and power peripherals, which include power FETs, hysteretic controllers, current sense amplifiers, and PrISM/PWM modulators. Configurable global busing combines all of the device resources into a complete custom system. The PowerPSoC family of devices have 10-port I/Os that connect to the global digital and analog interconnects, providing access to eight digital blocks and six analog blocks.

5. Power Peripherals

PowerPSoC is designed to operate at voltages from 7 V to 32 V, drive up to 1 ampere of current using internal MOSFET switches, and over 1 ampere with external MOSFETs.

This family of devices (CY8CLED0xD/G0y) combines up to four independent channels of constant current drivers. These drivers feature hysteretic controllers with the Programmable System-on-Chip (PSoC) that contains an 8-bit microcontroller, configurable digital and analog peripherals, and embedded flash memory.

The CY8CLED0xD/G0y is the first product in the PowerPSoC family to integrate power peripherals to add further integration for your power electronics applications.The PowerPSoC family of intelligent power controller ICs are used in lighting applications that need traditional MCUs and discrete power electronics support. The power peripherals of the CY8CLED0xD/G0y include up to four 32 volt power MOSFETs with current ratings up to 1 ampere each. It also integrates gate drivers that enable applications to drive external MOSFETs for higher current and voltage capabilities. The controller is a programmable threshold hysteretic controller, with user-selectable feedback paths that uses the IC in current mode floating load buck, floating load buck-boost, and boost configurations.

5.1 Hysteretic Controllers

The PowerPSoC contains four hysteretic controllers. There is one hysteretic controller for each channel of the device.

The hysteretic controllers provide cycle by cycle switch control with fast transient response, which simplifies system design by requiring no external compensation. The hysteretic controllers include the following key features:

- Four independent channels
- DAC configurable thresholds
- Wide switching frequency range from 20 kHz to 2 MHz
- Programmable minimum on and off time
- Floating load buck, floating load buck-boost and boost topology controller

The reference inputs (REF_A and REF_B in Figure 5-1.) of the hysteretic controller are provided by the reference DACs as illustrated in the top level block diagram (see Figure 3-1. on page 3).

The hysteretic control function output is generated by comparing the feedback value to two thresholds. Going below the lower threshold turns the switch ON and exceeding the upper threshold turns the switch OFF as shown in Figure 5-1. The output current waveforms are shown in Figure 5-2.

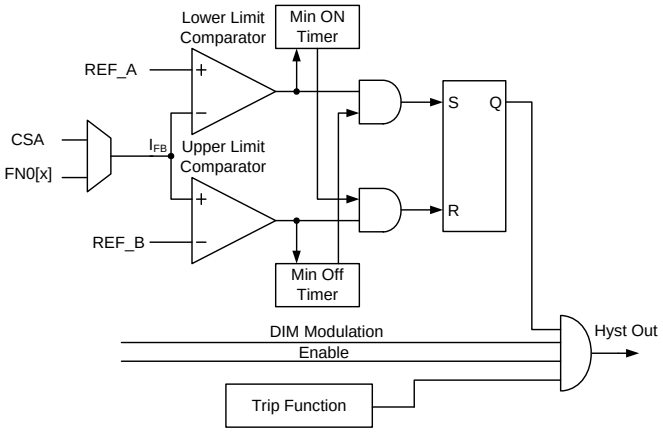
The hysteretic controller also controls the minimum on-time and off-time. This circuit prevents oscillation at very high frequencies; which can be very destructive to output switches.

The output to the gate drivers is gated by the Trip, DIM and Enable signals. The Enable signal is a direct result of the enable bit in the control register for the hysteretic controller.

The Trip signal can be any digital signal that follows TTL logic (logic high and logic low). It is an active high input.

The DIM Modulation signal is the output of the dedicated modulators that are present in the power peripherals, or any other digital modulation signal.

Figure 5-1. Generating Hysteretic Control Function Output



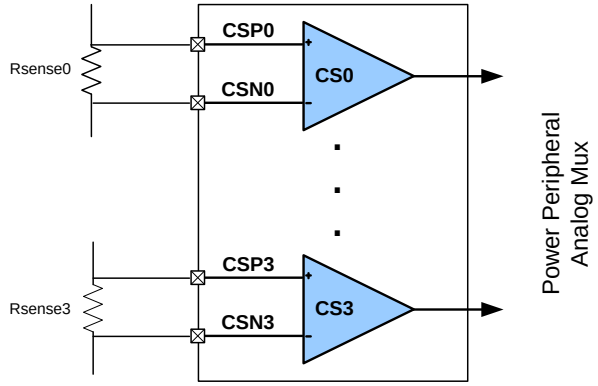
the routing is done. Table 5-1 illustrates example values of R_{sense} for different currents.

The method to calculate the R_{sense} value for a desired average current is explained in the application note CY8CLED0xx0x: Topology and Design Guide for Circuits using PowerPSoC - AN52699

Table 5-1. R_{sense} Values for Different Currents

Max Load Current (mA)	Typical R_{sense} (mΩ)
1000	100
750	130
500	200
350	300

Figure 5-3. High Side Current Measurement



5.6 Voltage Comparators

There are six comparators that provide high speed comparator operation for over voltage, over current, and various other system event detections. For example, the comparators may be used for zero crossing detection for an AC input line or monitoring total DC bus current. Programmable internal analog routing enables these comparators to monitor various analog signals. These comparators include the following key features:

- High speed comparator operation: 100 ns response time
- Programmable interrupt generation
- Low input offset voltage and input bias currents

Six precision voltage comparators are available. The differential positive and negative inputs of the comparators are routed from the analog multiplexer and the output goes to the digital multiplexer. A programmable inverter is used to select the output polarity. User-selectable hysteresis can be enabled or disabled to trade-off noise immunity versus comparator sensitivity.

5.7 Reference DACs

The reference DACs are used to generate set points for various analog modules such as Hysteretic controllers and comparators. The reference DACs include the following key features:

- 8-bit resolution
- Guaranteed monotonic operation
- Low gain errors
- 10 us settling time

These DACs are available to provide programmable references for the various analog and comparator functions and are controlled by memory mapped registers.

DAC[0:7] are embedded in the hysteretic controllers and are required to set the upper and lower thresholds for channel 0 to 3.

DAC [8:13] are connected to the Power Peripherals Analog Multiplexer and provide programmable references to the comparator bank. These are used to set trip points which enable over voltage, over current, and other system event detection.

5.8 Built-in Switching Regulator

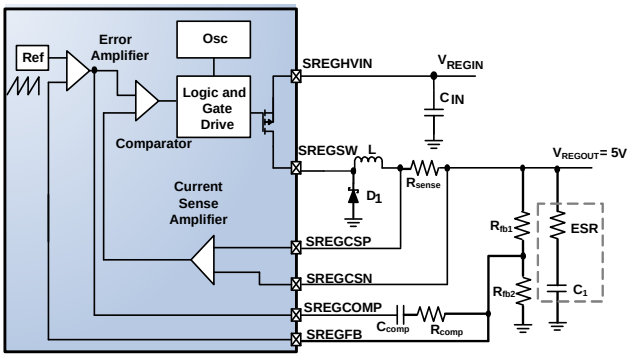
The switching regulator is used to power the low voltage (5 V portion of the PowerPSoC) from the input line. This regulator is based upon a peak current control loop which can support up to 250 mA of output current. The current not being consumed by PowerPSoC is used to power additional system peripherals. The key features of the built-in switching regulator include:

- Ability to self power device from input line
- Small filter component sizes
- Fast response to transients

Refer to Table 15-20 for component values.

The 'Ref' signal that forms the reference to the Error Amplifier is internally generated and there is no user control over it.

Figure 5-4. Built-in Switching Regulator



5.9 Analog Multiplexer

The PowerPSoC family's analog MUX is designed to route signals from the CSA output, function I/O pins and the DACs to comparator inputs and the current sense inputs of the hysteretic controllers. Additionally, CSA outputs can be routed to the AINX block using this MUX.

For a full matrix representation of all possible routing using this MUX, refer to the PowerPSoC Technical Reference Manual.

The CPU configures the Power Peripherals Analog Multiplexer connections using memory mapped registers. The analog multiplexer includes the following key features:

- Signal integrity for minimum signal corruption

5.10 Digital Multiplexer

The PowerPSoC family's digital MUX is a configurable switching matrix that connects the power peripheral digital resources.

For a full matrix representation of all possible routing using this MUX, refer to the PowerPSoC Technical Reference Manual.

This power peripheral digital multiplexer is independent of the main PSoC digital buses or global interconnect of the PSoC core. The digital multiplexer includes the following key features:

- Connect signals to ensure needed flexibility

5.11 Function Pins (FN0[0:3])

The function I/O pins are a set of dedicated control pins used to perform system level functions with the power peripheral blocks of the PowerPSoC. These pins are dynamically configurable, enabling them to perform a multitude of input and output functions. These I/Os have direct access to the input and output of the voltage comparators, input of the hysteretic controller, and output of the digital PWM blocks for the device. The function I/O pins are register mapped. The microcontroller can control and read the state of these pins and the interrupt function.

Some of the key system benefits of the function I/O are:

- Enabling an external higher voltage current-sense amplifier as shown in Figure 5-5.
- Synchronizing dimming of multiple PowerPSoC controllers as shown in Figure 5-6.
- Programmable fail-safe monitor and dedicated shutdown of hysteretic controller as shown in Figure 5-7.

Along with the these functions, these I/Os also provide interrupt functionality, enabling intelligent system responses to power control lighting system status.

Figure 5-5. External CSA and FET Application

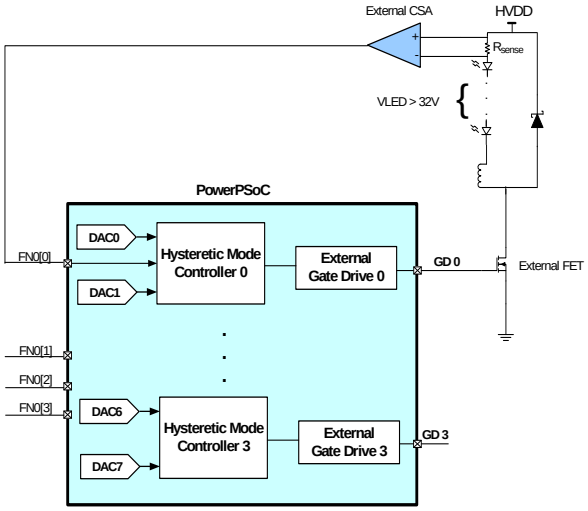


Figure 5-6. PowerPSoC in Master/Slave Configuration

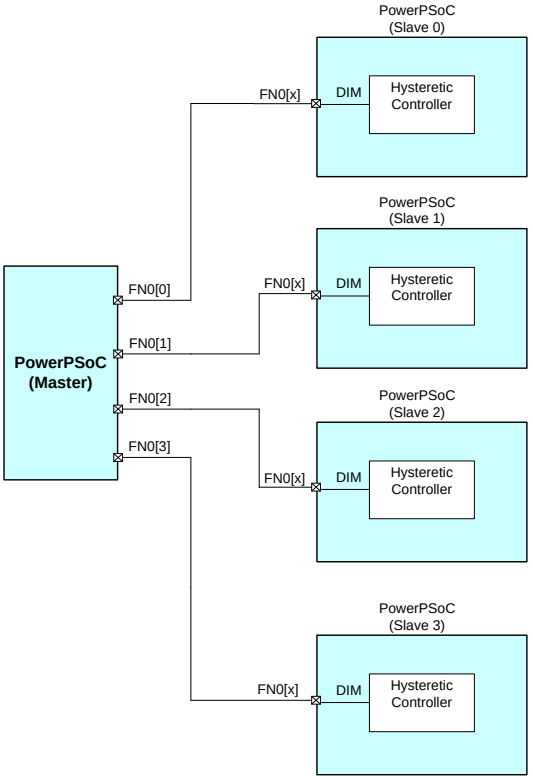
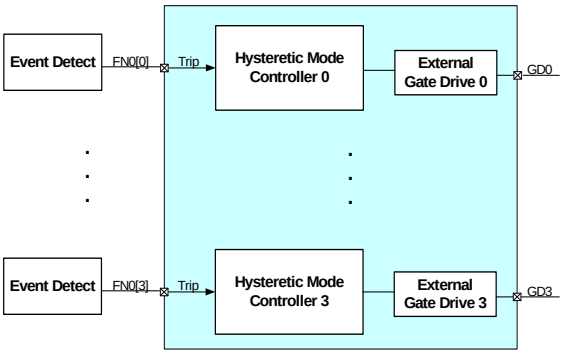


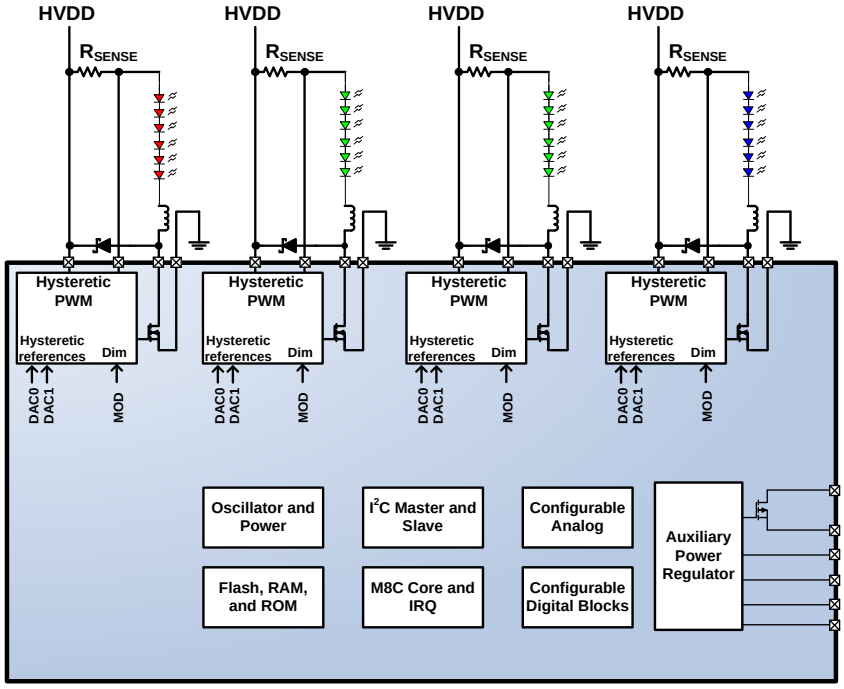
Figure 5-7. Event Detection



7. Applications

The PowerPSoC family of devices can be used to add hysteretic current control capability to power applications. The devices can be used to control current in devices such as LEDs, heating elements, and solenoids. For LED applications, all high-brightness LEDs (HBLEDs) can be controlled using the PowerPSoC. The following figures show examples of applications in which the PowerPSoC family of devices adds intelligent power control for power applications.

Figure 7-1. LED Lighting with RGGB Color Mixing Configured as Floating Load Buck Converter



8. PowerPSoC Device Characteristics

There are two major groups of devices in the PowerPSoC family. One group is a 4-channel 56-pin QFN and the other is a 3-channel 56-pin QFN. These are summarized in the following table.

Table 8-1. PowerPSoC Device Characteristics

Device Group	Internal Power FETs	External Gate Drivers	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8CLED04D01-56LTXI	4X1.0 A	4	14	2	8	14	2	2	6	1 K	16 K
CY8CLED04D02-56LTXI	4X0.5 A	4	14	2	8	14	2	2	6	1 K	16 K
CY8CLED04G01-56LTXI	0	4	14	2	8	14	2	2	6	1 K	16 K
CY8CLED03D01-56LTXI	3X1.0 A	3	14	2	8	14	2	2	6	1 K	16 K
CY8CLED03D02-56LTXI	3X0.5 A	3	14	2	8	14	2	2	6	1 K	16 K
CY8CLED03G01-56LTXI	0	3	14	2	8	14	2	2	6	1 K	16 K
CY8CLED02D01-56LTXI	2X1.0 A	2	14	2	8	14	2	2	6	1 K	16 K
CY8CLED01D01-56LTXI	1X1.0 A	1	14	2	8	14	2	2	6	1 K	16 K
CY8CLED01D01-56LTXQ	1X1.0 A	1	14	2	8	14	2	2	6	1 K	16 K

10.2 In-Circuit Emulator

A low cost, high functionality in-circuit emulator (ICE) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PowerPSoC devices.

11. Designing with User Modules

The development process for the PowerPSoC device differs from that of a traditional fixed function microprocessor. The configurable power, analog, and digital hardware blocks give the PowerPSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PowerPSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PowerPSOC development process can be summarized in the following four steps:

1. Select components
2. Configure components
3. Organize and connect
4. Generate, Verify and debug

Select Components. In the chip-level view the components are called “user modules”. User modules make selecting and implementing peripheral devices simple and come in power, analog, digital, and mixed signal varieties. The standard user module library contains over 50 common peripherals such as current sense amplifiers, PrISM, PWM, DMM, Floating Buck, Boost, ADCs, DACs, Timers, Counters, UARTs, and other not so common peripherals such as DTMF generators and Bi-Quad analog filter sections.

Configure Components. Each of the components selected establishes the basic register settings that implement the selected function. They also provide parameters allowing precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

The chip-level user modules are documented in datasheets that are viewed directly in PSoC Designer. These datasheets explain the internal operation of the component and provide performance specifications. Each datasheet describes the use of each user module parameter and other information needed to successfully implement your design.

Organize and Connect. Signal chains can be built at the chip level by interconnecting user modules to each other and the I/O pins. In the chip-level view, perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

Generate, Verify, and Debug. When ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Application” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the high level user module API functions.

The chip-level designs generate software based on your design. The chip-level view provides application programming interfaces (APIs) with high level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed.

A complete code development environment allows development and customization of your applications in C, assembly language, or both.

The last step in the development process takes place inside the PSoC Designer’s Debugger subsystem. The Debugger downloads the HEX image to the ICE where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

12.4 CY8CLED03D0x 56-Pin Part Pinout (without OCD)

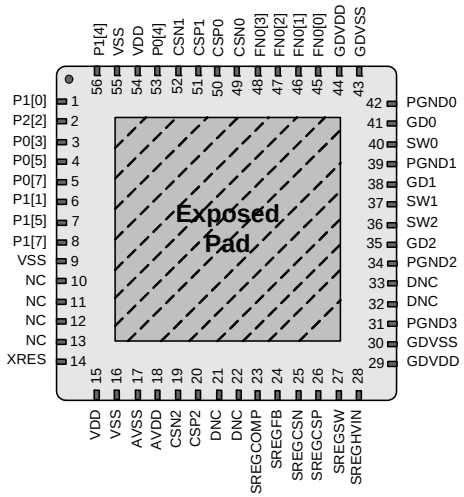
The CY8CLED03D01 and CY8CLED03D02 PowerPSoC devices are available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-4. CY8CLED03D0x 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I2C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCL (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I2C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I2C SCL (Primary)
9				V_{SS}	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19			I	CSN2	Current Sense Negative Input - CSA2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				DNC[5]	Do Not Connect
22				DNC[5]	Do Not Connect
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[6]	Power FET Ground 3
32				DNC[5]	Do Not Connect
33				DNC[5]	Do Not Connect
34				PGND2[6]	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				SW2	Power Switch 2
37				SW1	Power Switch 1
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[6]	Power FET Ground 1
40				SW0	Power Switch 0
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[6]	Power FETGround 0
43				GDV_{SS}	Gate Driver Ground

Figure 12-4. CY8CLED03D0x 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Notes
5. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
6. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

12.5 CY8CLED03G01 56-Pin Part Pinout (without OCD)

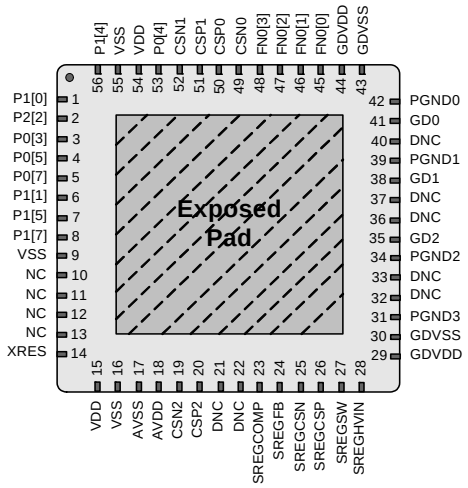
The CY8CLED03G01 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-5. CY8CLED03G01 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I2C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCL (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I2C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I2C SCL (Primary)
9				V_{SS}	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19			I	CSN2	Current Sense Negative Input 2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				DNC[7]	Do Not Connect
22				DNC[7]	Do Not Connect
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[8]	Power FET Ground 3
32				DNC[7]	Do Not Connect
33				DNC[7]	Do Not Connect
34				PGND2[8]	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				DNC[7]	Do Not Connect
37				DNC[7]	Do Not Connect
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[8]	Power FET Ground 1
40				DNC[7]	Do Not Connect
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[8]	Power FET Ground 0
43				GDV_{SS}	Gate Driver Ground

Figure 12-5. CY8CLED03G01 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Notes
7. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
8. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

15.7 Power Peripheral Current Sense Amplifier

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to V_{DD} of 5 V and HV_{DD} of 32 V at 25 °C. These are for design guidance only.

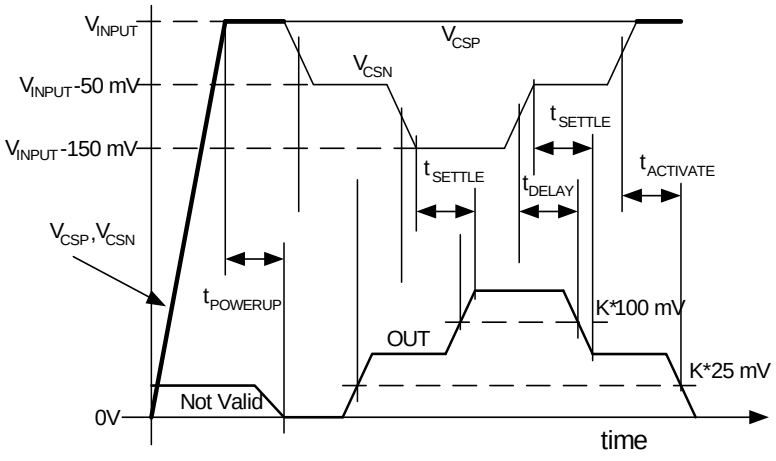
Table 15-12. Current Sense Amplifier DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ICM}	Input common mode voltage operating range	7	–	32	V	Either terminal of the amplifier must not exceed this range for functionality
$V_{ICM(Tolerant)}$	Non functional operating range	0	–	32		Absolute maximum rating for V_{SENSE} should never be exceeded. See Absolute Maximum Ratings on page 30
V_{SENSE}	Input differential voltage range	0	–	150	mV	
$I_{S,CSA}$	Supply current - CSA	–	–	1	mA	Enabling CSA causes an incremental draw of 1 mA on the AV_{DD} rail.
I_{BIASP}	Input bias current (+)	–	–	600	µA	
I_{BIASN}	Input bias current (-)	–	–	1	µA	
PSR_{HV}	Power supply rejection (CSP pin)	–	–	–25	dB	$f_{SW} < 2$ MHz
K	Gain	19.7 19.4	20 20	20.3 20.6	V/V V/V	V_{SENSE} = 50 mV to 130 mV (Industrial rated) V_{SENSE} = 50 mV to 130 mV (Extended Temperature rated)
V_{IOS}	Input offset	–	2	4	mV	V_{SENSE} = 50 mV to 130 mV
C_{IN_CSP}	CSP input capacitance	–	–	5	pF	
C_{IN_CSN}	CSN input capacitance	–	–	2	pF	

Table 15-13. Current Sense Amplifier AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{SETTLE}	Output settling time to 1% of final value	–	–	5	µs	
$t_{POWERUP}$	Power up time to 1% of final value	–	–	5	µs	

Figure 15-4. Current Sense Amplifier Timing Diagram



15.9 Power Peripheral Reference DAC Specification

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-16. Reference DAC DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{SDAC}	Supply current - reference DAC	–	–	600	µA	Mode 0 and Mode1
INL	Integral non linearity	–1 –1.5	– –	1 1.5	LSB LSB	Mode 0 Mode 1
DNL	Differential non linearity	–0.5	–	0.5	LSB	Mode 0 and Mode1
A_{ERROR}	Gain error	–5 –7	– –	5 7	LSB LSB	Mode 0 Mode 1
OS_{ERROR}	Offset error	–	–	1	LSB	Mode 0 and Mode1
V_{DACFS}	Fullscale voltage - reference DAC	– –	– –	2.6 1.3	LSB LSB	Mode 0 Mode 1
V_{DACMM}	Fullscale voltage mismatch (pair of reference DACs - even and odd)	– – – –	– – – –	9 14 10.5 15.5	LSB LSB LSB LSB	Mode 0 (DAC0 through DAC7) Mode 1 (DAC0 through DAC7) Mode 0 (DAC8 through DAC13) Mode 1 (DAC8 through DAC13)

Table 15-17. Reference DAC AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{SETTLE}	Output settling time to 0.5 LSB of final value	–	–	10	µs	Mode 0 and Mode1
$t_{STARTUP}$	Startup time to within 0.5 LSB of final value	–	–	10.5	µs	Mode 0 and Mode1

15.10 Power Peripheral Built-in Switching Regulator

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-18. Built-in Switching Regulator DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REGIN}	Input supply voltage range	7 8	– –	32 32	V V	Industrial rated Extended temperature rated See Absolute Maximum Ratings on page 30
V_{REGOUT}	Output voltage range	4.8	5.0	5.2	V	Does not include V_{RIPPLE}
V_{RIPPLE}	Output ripple	–	–	100	mV	
V_{UVLO}	Under voltage lockout voltage	5.5	–	6.5	V	$V_{REGIN} < V_{UVLO}$: Power down mode $V_{REGIN} > V_{UVLO}$: Active mode
I_{LOAD}	DC output current -active mode	0.01	–	250	mA	–
$I_{S,BSR}$	Supply current - built-in switching regulator	–	–	4	mA	–
$I_{SB,HV}$	Standby current (high voltage)	–	–	250	µA	–
I_{INRUSH}	Inrush current	– –	– –	1.2 1.5	A A	V_{REGIN} = 32 V, SR_{REGIN} = 32 V/ms (Industrial rated) V_{REGIN} = 32 V, SR_{REGIN} = 32 V/ms (Extended Temperature rated)
$R_{DS(ON),PFET}$	PFET drain to source ON resistance	–	2.5	–	Ω	
$Line_{REG}$	Line regulation	–	1	–	mV	I_{LOAD} = 250 mA, V_{REGIN} = 7 V to 32 V

Table 15-18. Built-in Switching Regulator DC Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
$Load_{REG}$	Load regulation	–	1	–	mV	V_{REGIN} = 24 V, I_{LOAD} = 2.5 mA to 250 mA
PSRR	Power supply rejection ratio	–	–60	–	dB	V_{RIPPLE} = 0.2 * V_{REGIN}, f_{RIPPLE} = 1 kHz to 10 kHz
E_{BSR}	Built-in switching regulator efficiency	80	–	–	%	V_{REGIN} = 24 V, I_{LOAD} = 250 mA

Table 15-19. Built-in Switching Regulator AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
f_{SW}	Switching frequency	0.956	1	1.04	MHz	–
t_{RESP}	Response time to within 0.5% of final value	–	10	–	µs	–
t_{SU}	Startup time	–	–	1	ms	–
t_{PD}	Power down time	–	–	100	µs	–
t_{PD_ACT}	Time from power down to active mode	–	–	1	ms	–
t_{ACT_PD}	Time from active mode to power down mode	–	–	50	µs	–
SR_{REGIN}	Ramp rate for the SREGHVIN pin	–	–	32	V/µs	See Absolute Maximum Ratings on page 30

Table 15-20. Built-in Switching Regulator Recommended Components

Component Name	Value	Unit	Notes
R_{fb1}	2	kΩ	Tolerance 1% and 0.05-W rated or better
R_{fb2}	0.698	kΩ	Tolerance 1% and 0.05-W rated or better
C_{comp}	2200	pF	Tolerance 20% and 6.3-V rated or better
R_{comp}	20	kΩ	Tolerance 5% and 0.05-W rated or better
L	47	µH	Tolerance 20% or better, Saturation current rating of 1.5 A or higher
R_{sense}	0.5	Ω	Tolerance 1% and 0.05 W (I_{LOAD} = 0.250 A) rated or better
C_1	10	µF	Ceramic, X7R grade, Minimum ESR of 0.1 Ω, 6.3-V rated
C_{in}	1	µF	Ceramic, X7R grade, 50-V rated (V_{REGIN} = 32 V)
D1	40/0.5	V/A	Schottky diode - Reverse voltage 40 V, average rectified forward current 0.5 A (V_{REGIN} = 32 V)

Note If the built-in switching regulator is not being used in a design, it must be configured as per the following instructions to ensure it is disabled in a safe state.

SREGFB: 5 V

SREGCSN: 5 V

SREGCSP: 5 V

SREGCOMP: Floating

SREGHVIN: ≥ VDD rail

SREGSW: Floating/Tie to SREGHVIN

If the switching regulator is disabled through wiring its input pins (as previously explained) then it must be disabled through software as well (bit SREG_TST[0] = 1), which is set in the Global Resources in the Interconnect View of PSoC Designer.

Figure 15-5. Built-in Switching Regulator Timing Diagram

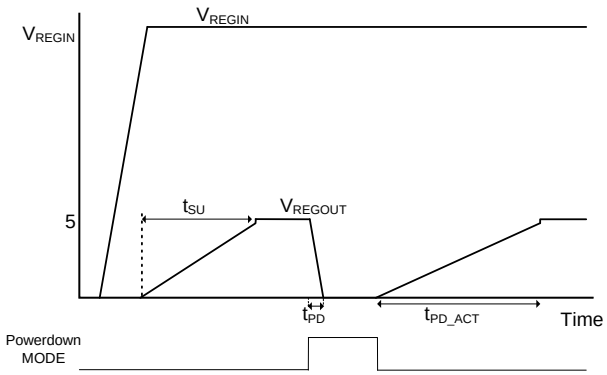
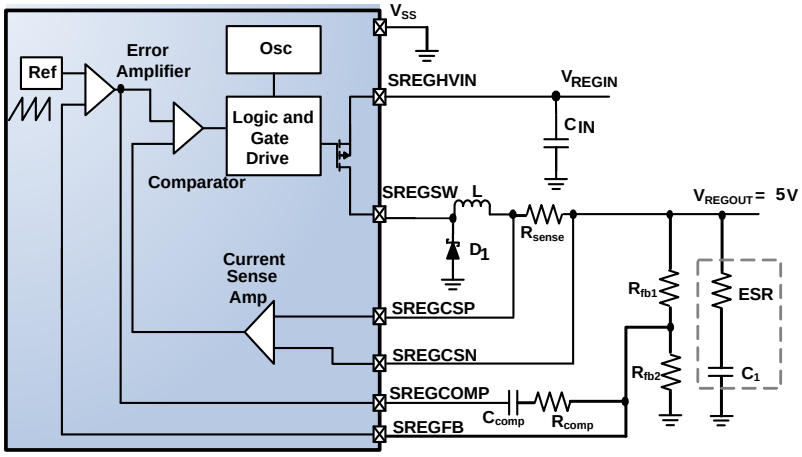


Figure 15-6. Built-in Switching Regulator



15.12 PSoC Core Operational Amplifier Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Capacitor PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block.

Table 15-23. Operational Amplifier DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 – – – – – –	 1.6 1.6 1.3 1.3 1.2 1.2	 10 15 8 13 7.5 12	 mV mV mV mV mV mV	 Industrial rated Extended temperature rated Industrial rated Extended temperature rated Industrial rated Extended temperature rated
TCV_{OSOA}	Average input offset voltage drift	–	7.0	35.0	µV / °C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	T_J = 25 °C.
V_{CMOA}	Common mode voltage range Common mode voltage range (high power or high opamp bias)	0.0 0.5	– –	V_{DD} V_{DD} – 0.5	V V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 60 60 80	 – – –	 – – –	 dB dB dB	–
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.5	 – – –	 – – –	 V V V	–
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 – – –	 – – –	 0.2 0.2 0.5	 V V V	–
I_{SOA}	Supply current (including associated analog output buffer) Power = low, opamp bias = low Power = low, opamp bias = high Power = medium, opamp bias = low Power = medium, opamp bias = high Power = high, opamp bias = low Power = high, opamp bias = high	 – – – – – –	 400 500 800 1200 2400 4600	 800 900 1000 1600 3200 6400	 µA µA µA µA µA µA	–
$PSRR_{OA}$	Supply voltage rejection ratio	52	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$.

15.14 PSoC Core Analog Output Buffer

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-27. Analog Output Buffer DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input offset voltage (absolute value) 	– –	3 3	12 18	mV mV	Industrial rated Extended Temperature rated
TCV_{OSOB}	Average input offset voltage drift	–	+6	–	µV/°C	–
V_{CMOB}	Common-mode input voltage range	0.5	–	V_{DD} – 1.0	V	–
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 0.6 0.6	 – –	 Ω Ω	–
$V_{OHIGHOB}$	High output voltage swing (load = 32 ohms to $V_{DD}/2$) Power = low Power = high	0.5 x V_{DD} + 1.1 0.5 x V_{DD} + 1.1	– –	– –	V V	–
V_{OLOWOB}	Low output voltage swing (load = 32 ohms to $V_{DD}/2$) Power = low Power = high	– –	– –	0.5 x V_{DD} – 1.3 0.5 x V_{DD} – 1.3	V V	–
I_{SOB}	Supply current including bias cell (no load) Power = low Power = high	 – –	 1.1 2.6	 5.1 8.8	 mA mA	–
$PSRR_{OB}$	Supply voltage rejection ratio	52	64	–	dB	(0.5 x V_{DD} – 1.3) ≤ V_{OUT} ≤ (V_{DD} – 2.3).

Table 15-28. Analog Output Buffer AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROB}	Rising settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high	 – –	 – –	 2.5 2.5	 µs µs	–
t_{SOB}	Falling settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high	 – –	 – –	 2.2 2.2	 µs µs	–

15.15 PSoC Core Analog Reference

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for extended temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the analog continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Table 15-29. Analog Reference DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
BG	Bandgap voltage reference	1.28 1.27	1.30 1.30	1.32 1.33	V V	Industrial rated Extended Temperature rated
–	AGND = $V_{DD}/2$[16]	$V_{DD}/2 - 0.04$ $V_{DD}/2 - 0.02$	$V_{DD}/2 - 0.01$ $V_{DD}/2$	$V_{DD}/2 + 0.007$ $V_{DD}/2 + 0.02$	V V	Industrial rated Extended Temperature rated
–	AGND = 2 x BandGap[16]	2 x BG – 0.048	2 x BG – 0.030	2 x BG + 0.024	V	
–	AGND = BandGap[16]	BG – 0.009	BG + 0.008	BG + 0.016	V	
–	AGND = 1.6 x BandGap[16]	1.6 x BG – 0.022	1.6 x BG – 0.010	1.6 x BG + 0.018	V	
–	AGND Block to Block Variation (AGND = $V_{DD}/2$)[16]	–0.034	0.000	0.034	V	
–	RefHi = $V_{DD}/2$ + BandGap	$V_{DD}/2$ + BG – 0.10	$V_{DD}/2$ + BG	$V_{DD}/2$ + BG + 0.10	V	
–	RefHi = 3 x BandGap	3 x BG – 0.06	3 x BG	3 x BG + 0.06	V	
–	RefHi = 3.2 x BandGap	3.2 x BG – 0.112	3.2 x BG	3.2 x BG + 0.076	V	
–	RefLo = $V_{DD}/2$ – BandGap	$V_{DD}/2$ – BG – 0.04 $V_{DD}/2$ – BG – 0.06	$V_{DD}/2$ – BG + 0.024 $V_{DD}/2$ – BG	$V_{DD}/2$ – BG + 0.04 $V_{DD}/2$ – BG + 0.06	V V	Industrial rated Extended Temperature rated
–	RefLo = BandGap	BG – 0.06	BG	BG + 0.06	V	

15.16 PSoC Core Analog Block

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-30. Analog Block DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor unit value (continuous time)	–	12.2	–	kΩ	
C_{SC}	Capacitor unit value (switched capacitor)	–	80	–	fF	

Notes
16. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3 V ± 0.02 V.

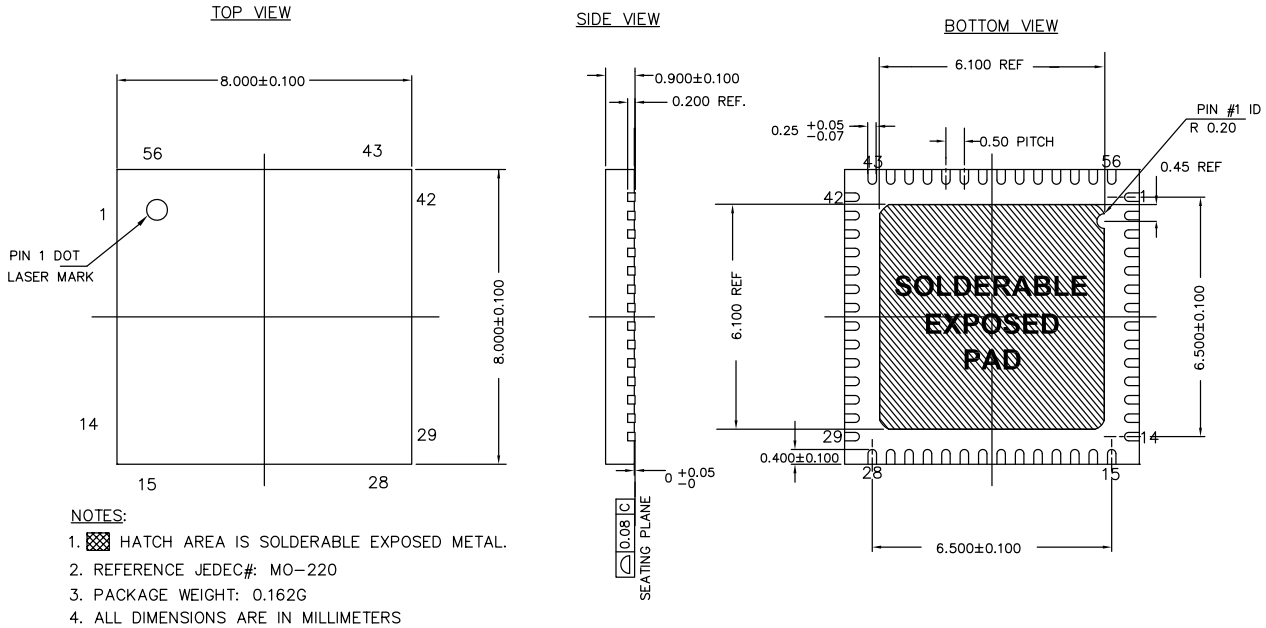
17. Packaging Information

Packaging Dimensions

This section illustrates the package specification for the CY8CLED04D0X, CY8CLED04G01, CY8CLED03D0X, CY8CLED03G01, CY8CLED02D01, and CY8CLED01D01 along with the thermal impedance for the package and solder reflow peak temperatures.

Important Note For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

Figure 17-1. 56-Pin QFN (8 × 8 × 1.0 mm)



51-85187 *G

17.1 Thermal Impedance

Package	Typical θ_{JA} [22]
56 QFN[23]	16.6 °C/W

17.2 Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Package	Minimum Peak Temperature[24]	Maximum Peak Temperature
56 QFN	240 °C	260 °C

Notes

22. $T_J = T_A + POWER \times \theta_{JA}$
23. To achieve the thermal impedance specified for the QFN package, the center thermal pad should be soldered to the PCB ground plane. The thermal model for Cypress's PowerPSoC family was simulated using a JESD51-7 standard FR4 PCB with four metal layers, 2 oz copper weight on outer layers, and 1 oz on inner layers. Thermal via array below the device is laid out according to package manufacturers' recommendations.
24. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

18. Acronyms

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CSA	current sense amplifier
CT	continuous time
DAC	digital-to-analog converter
DALI	digital addressable lighting interface
DC	direct current
DMM	delta sigma modulation mode
DMX	digital multiplexing
DSM	delta sigma modulator
DTMF	dual-tone multi frequency
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
FAQ	frequently asked questions
FET	field effect transistor
FSR	full scale range
GPIO	general purpose i/o
GUI	graphical user interface
HBM	human body model
IC	integrated circuit
ICE	in-circuit emulator
IDE	integrated development environment
ILO	internal low-speed oscillator
IMO	internal main oscillator
ISSP	in-system serial programming
I/O	input/output
IPOR	imprecise power on reset
LED	light emitting diode
LSB	least-significant bit
LVD	low voltage detect
MCU	microcontroller
MOSFET	metal-oxide-semiconductor field effect transistor
MSB	most-significant bit
OCD	on chip debugger
PC	program counter
POR	power on reset
PPOR	precision power on reset
PowerPSoC	power programmable system-on-chip™
PrISM	precise intensity signal modulation
PSoC	programmable system-on-chip™
PWM	pulse width modulator
QFN	quad flat no leads package
RGBA	red, green, blue, amber
RGGB	red, green, green, blue
SAR	successive approximation register
SC	switched capacitor
SCL	serial I^2C
SCLK	serial issp clock
SDA	serial i^2c data
SDATA	serial issp data
SPI	serial peripheral interface
SRAM	static random access memory
TRM	technical reference manual
UART	universal asynchronous receiver/transmitter
USB	universal serial bus
WDT	watch dog timer

19. Document Conventions

19.1 Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibels
Hz	Hertz
pp	peak-to-peak
σ	sigma:one standard deviation
V	volt
Ω	ohm
KB	1024 bytes
ppm	parts per million
sps	samples per second
W	watt
A	ampere
Kbit	1024 bits
KHz	kilohertz
KΩ	kilohm
MHz	megahertz
MΩ	megaohm
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µVrms	microvolts root-mean-square

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