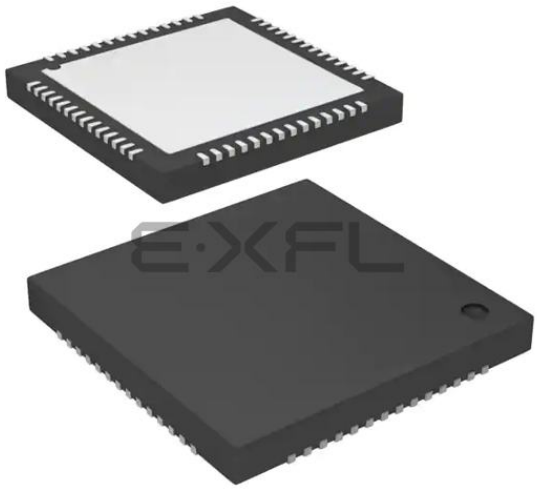


Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Intelligent LED Driver
Core Processor	M8C
Program Memory Type	FLASH (16KB)
Controller Series	CY8CLED
RAM Size	1K x 8
Interface	DALI, DMX512, I²C, IrDA, SPI, UART/USART
Number of I/O	14
Voltage - Supply	4.75V ~ 5.25V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad
Supplier Device Package	56-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8cled01d01-56ltxq

2. Contents

Figure 3-2. CY8CLED04G01 Logic Block Diagram

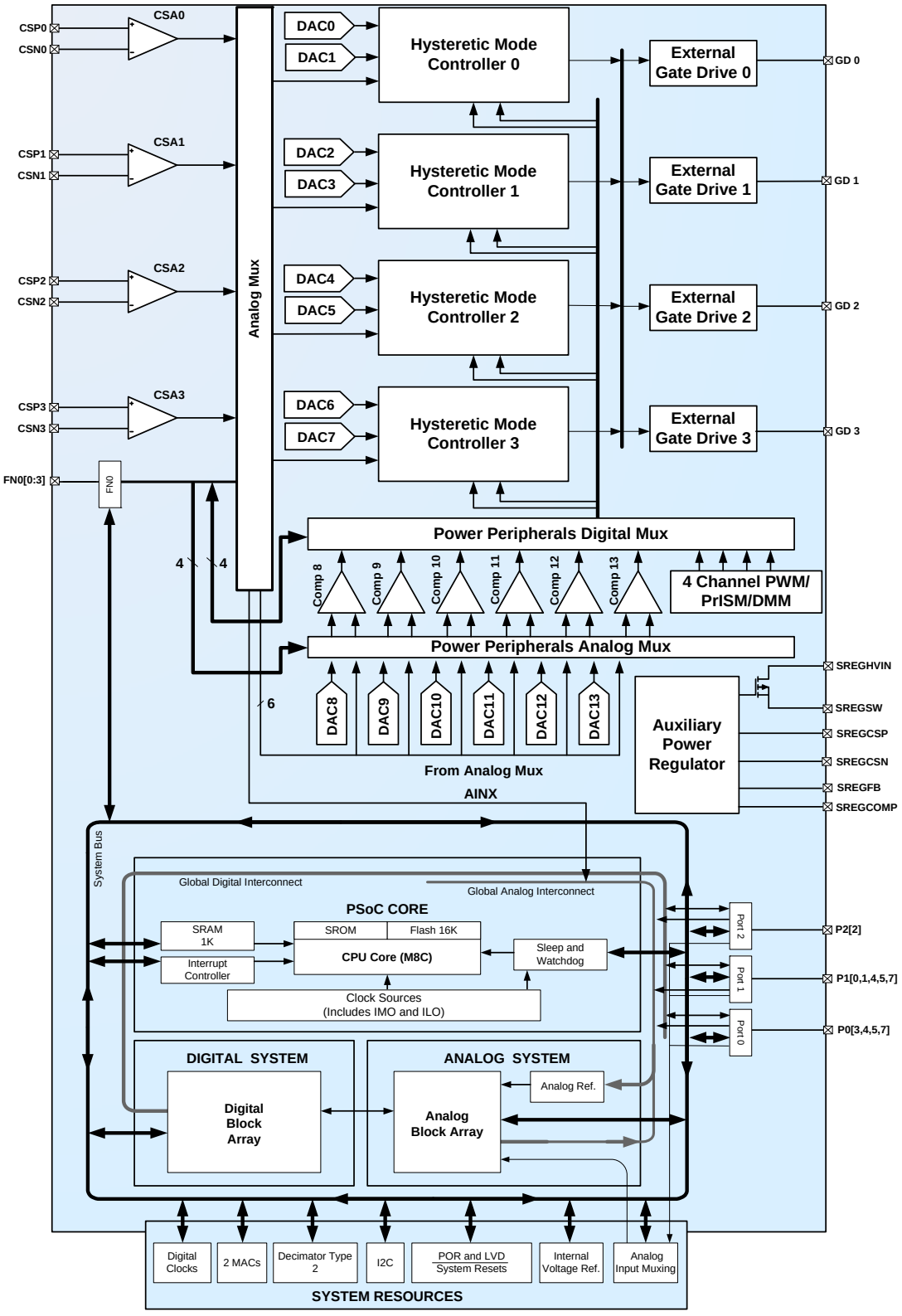


Figure 3-5. CY8CLED02D01 Logic Block Diagram

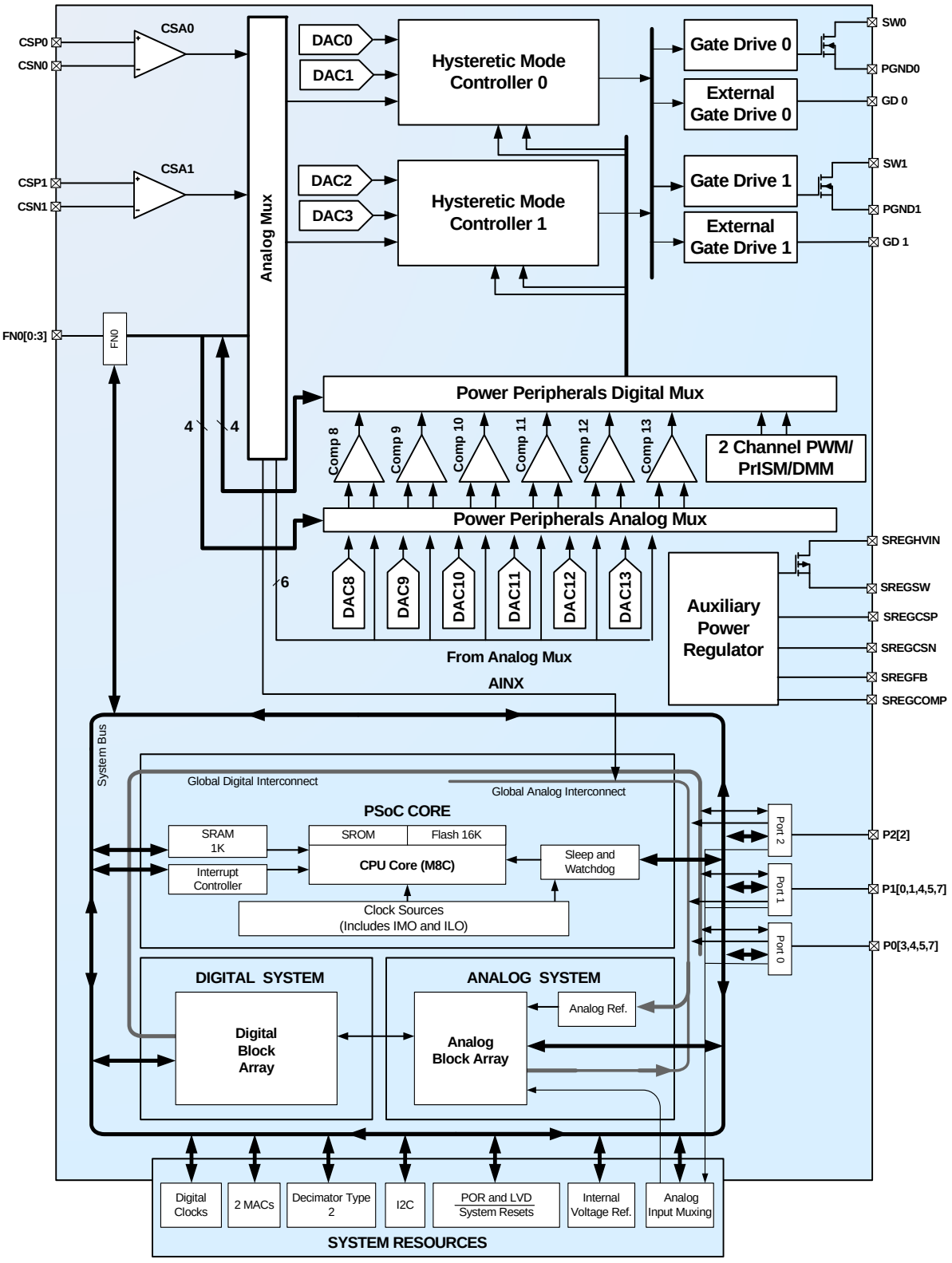
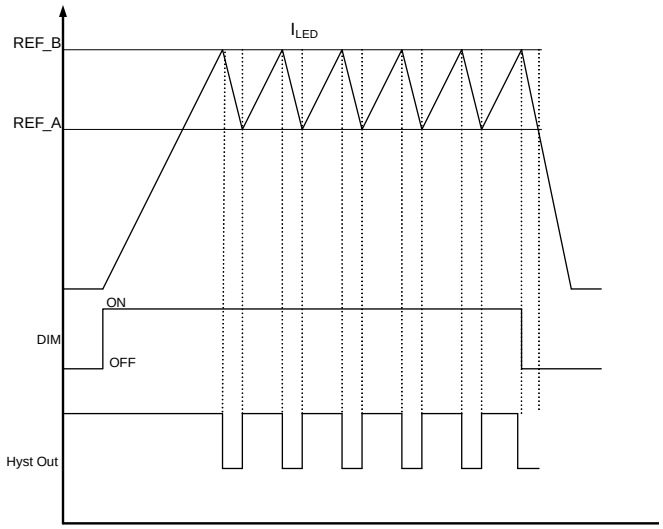


Figure 5-2. Current Waveforms



The minimum on-time and off-time circuits in the PowerPSoC prevent oscillations at very high frequencies, which can be very destructive to output switches.

5.2 Low Side N-Channel FETs

The internal low side N-Channel FETs are designed to enhance system integration. The low side N-Channel FETs include the following key features:

- Drive capability up to 1 A
- Switching times of 20 ns (rise and fall times) to ensure high efficiency (more than 90%)
- Drain source voltage rating 32 V
- Low $R_{DS(ON)}$ to ensure high efficiency
- Switching frequency up to 2 MHz

5.3 External Gate Drivers

These gate drivers enable the use of external FETs with higher current capabilities or lower $R_{DS(ON)}$. The external gate drivers directly drive MOSFETs that are used in switching applications. The gate driver provides multiple programmable drive strength steps to enable improved EMI management. The external gate drivers include the following key features:

- Programmable drive strength options (25%, 50%, 75%, 100%) for EMI management
- Rise and fall times at 55 ns with 4 nF load

5.4 Dimming Modulation Schemes

There are three dimming modulation schemes available with the PowerPSoC. The configurable modulation schemes are:

- Precise intensity signal modulation (PrISM)
- Delta Sigma modulation mode (DMM)
- Pulse-width modulation (PWM)

5.4.1 PrISM Mode Configuration

- High resolution operation up to 16 bits
- Dedicated PrISM module enables customers to use core PSoC digital blocks for other needs
- Clocking up to 48 MHz
- Selectable output signal density
- Reduced EMI

The PrISM mode compares the output of a pseudo-random counter with a signal density value. The comparator output asserts when the count value is less than or equal to the value in the signal density register.

5.4.2 DMM Mode Configuration

- High resolution operation up to 16 bits
- Configurable output frequency and delta sigma modulator width to trade off repeat rates versus resolution
- Dedicated DMM module enables customers to use PSoC digital blocks for other uses
- Clocking up to 48 MHz

The DMM modulator consists of a 12-bit PWM block and a 4-bit delta sigma modulator (DSM) block. The width of the PWM, the width of the DMM, and the clock defines the output frequency. The duty cycle of the PWM output is dithered by using the DSM block which has a user-selectable resolution up to 4 bits.

5.4.3 PWM Mode Configuration

- High resolution operation up to 16 bits
- User programmable period from 1 to 65535 clocks
- Dedicated PWM module enables customers to use core PSoC digital blocks for other use
- Interrupt on rising edge of the output or terminal count
- Precise PWM phase control to manage system current edges
- Phase synchronization among the four channels
- PWM output can be aligned to left, right, or center

The PWM features a down counter and a pulse width register. A comparator output is asserted when the count value is less than or equal to the value in the pulse width register.

5.5 Current Sense Amplifier

The high side current sense amplifiers provide a differential sense capability to sense the voltage across current sense resistors in lighting systems. The current sense amplifier includes the following key features:

- Operation with high common mode voltage to 32 V
- High common mode rejection ratio
- Programmable bandwidth to optimize system noise immunity

An off-chip resistor R_{sense} is used for high side current measurement as shown in Figure 5-3. on page 11. The output of the current sense amplifier goes to the power peripherals analog multiplexer where, you select the hysteretic controller to which

6. PSoC Core

The PSoC core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable general purpose I/O(GPIO).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with up to 20 vectors to simplify programming of real time embedded events. The program execution is timed and protected using the included sleep and watchdog timers (WDT) time and protect program execution.

Memory encompasses 16 K of flash for program storage, 1 K of SRAM for data storage, and up to 2 K of EEPROM emulated using the flash. Program flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

The PSoC device incorporates flexible internal clock generators, including a 24 MHz internal main oscillator (IMO) accurate to 4 percent over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz internal low-speed oscillator (ILO) is provided for the sleep timer and WDT. The clocks, together with programmable clock dividers (as a system resource), provide the flexibility to integrate almost any timing requirement into the PowerPSoC device.

PowerPSoC GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

6.1 Digital System

The digital system contains eight digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

Digital peripheral configurations include:

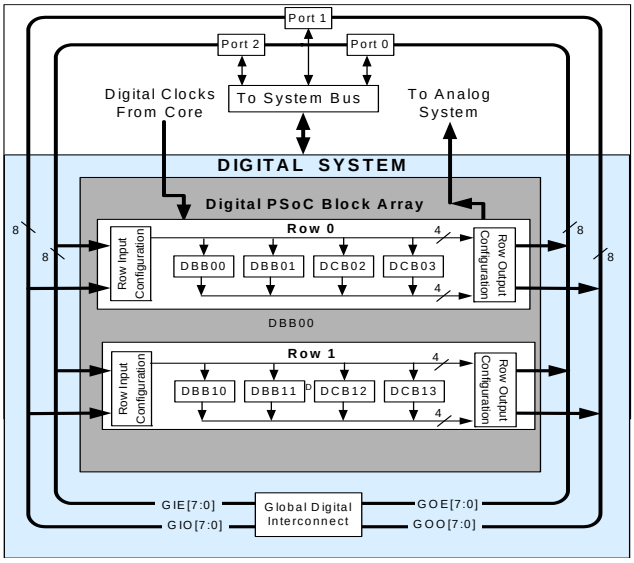
- DMX512
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8-bit with selectable parity
- SPI master and slave
- I^2C master, slave, and multi-master
- Cyclical redundancy checker/generator (8 to 32 bit)
- IrDA
- Pseudo random sequence generators (8 to 32 bit)

Note The DALI interface is supported through the use of a combination of the above mentioned user modules. For more details on the exact configuration and an example project, refer to the application note, PowerPSoC Firmware Design Guidelines, Lighting Control Interfaces - AN51012.

The digital blocks can be connected to any GPIO through a series of global buses that route any signal to any pin. The buses also allow signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

There are four digital blocks in each row. This allows optimum choice of system resources for your application.

Figure 6-1. Digital System Block Diagram



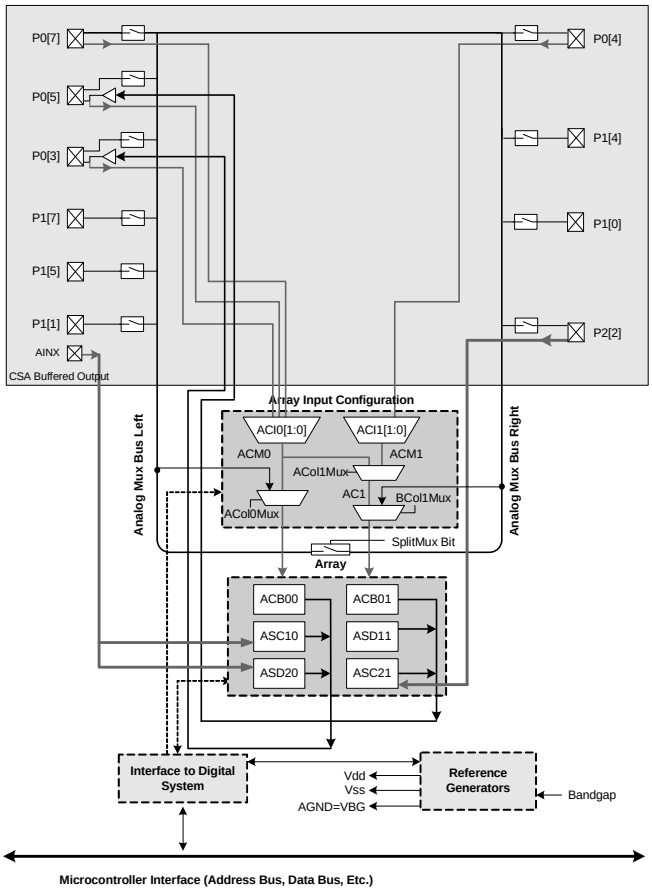
6.2 Analog System

The analog system contains six configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PowerPSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (up to 2, with 6 to 12-bit resolution, selectable as incremental, Delta Sigma, and SAR)
- Filters (2 and 4 pole band-pass, low-pass, and notch)
- Amplifiers (up to 2, with selectable gain to 48x)
- Instrumentation amplifiers (1 with selectable gain to 93x)
- Comparators (up to 2, with 16 selectable thresholds)
- DACs (up to 2, with 6 to 9-bit resolution)
- Multiplying DACs (up to 2, with 6 to 9-bit resolution)
- High current output drivers (two with 30 mA drive as a PSoC core resource)
- 1.3 V reference (as a system resource)
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are arranged in two columns of three blocks each, which includes one continuous time (CT) and two switched capacitor (SC) blocks, as shown in Figure 6-2. on page 14.

Figure 6-2. Analog System Block Diagram



6.3 Analog Multiplexer System

The Analog Mux Bus connects to every GPIO pin in ports 0 to 2. Pins can be connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters. It can be split into two sections for simultaneous dual-channel processing. An additional analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Track pad, finger sensing
- Crosspoint connection between any I/O pin combinations

Like other PSoC devices, PowerPSoC has specific pins allocated to the reference capacitor (Ref Cap) and modulation resistor (Mod resistor). These are indicated in the device pinouts (Section 13). For more details on capacitive sensing, see the design guide, Getting Started With CapSense. Apart from these, there are a number of application notes on Capacitive Sensing on the Cypress webbiest. The PowerPSoC Technical Reference Manual provides details on the analog system configuration that enables all I/Os in the device to be CapSense inputs.

6.4 Additional System Resources

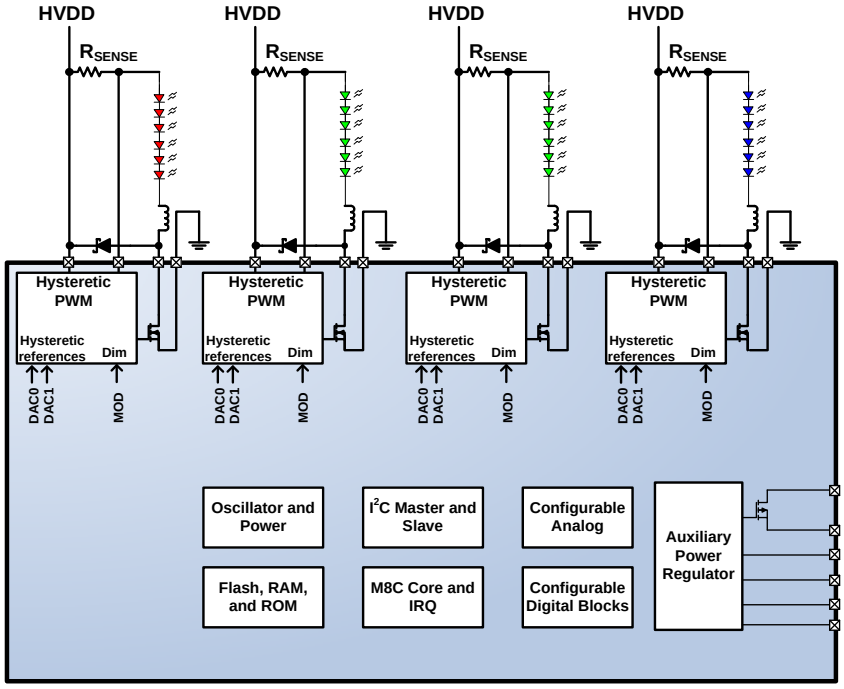
System resources provide additional capability useful in complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power on reset. Brief statements describing the merits of each resource follow.

- Two multiply accumulates (MACs) provide fast 8-bit multipliers with 32-bit accumulate, to assist in both general math and digital filters.
- A decimator provides a custom hardware filter for digital signal processing applications including creation of delta sigma ADCs.
- Low-voltage detection (LVD) interrupts signal the application of falling voltage levels, while the advanced POR (power on reset) circuit eliminates the need for a system supervisor.
- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. The designer can generate additional clocks using digital PSoC blocks as clock dividers.
- The I^2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master applications are supported.
- An internal 1.3 V reference provides an absolute reference for the analog system, including ADCs and DACs.
- Versatile analog multiplexer system.

7. Applications

The PowerPSoC family of devices can be used to add hysteretic current control capability to power applications. The devices can be used to control current in devices such as LEDs, heating elements, and solenoids. For LED applications, all high-brightness LEDs (HBLEDs) can be controlled using the PowerPSoC. The following figures show examples of applications in which the PowerPSoC family of devices adds intelligent power control for power applications.

Figure 7-1. LED Lighting with RGGB Color Mixing Configured as Floating Load Buck Converter



12.2 CY8CLED04G01 56-Pin Part Pinout (without OCD)

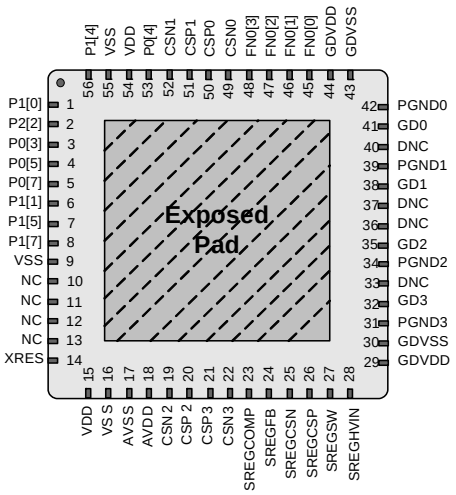
The CY8CLED04G01 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-2. CY8CLED04G01 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I^{2}C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I^{2}C SCL (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I^{2}C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I^{2}C SCL (Primary)
9				V_{SS}	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19			I	CSN2	Current Sense Negative Input 2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				CSP3	Current Sense Positive Input and Power Supply - CSA3
22			I	CSN3	Current Sense Negative Input 3
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[3]	Power FET Ground 3
32			O	GD3	External Low Side Gate Driver 3
33				DNC[2]	Do Not Connect
34				PGND2[3]	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				DNC[2]	Do Not Connect
37				DNC[2]	Do Not Connect
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[3]	Power FET Ground 1
40				DNC[2]	Do Not Connect
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[3]	Power FET Ground 0
43				GDV_{SS}	Gate Driver Ground
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Figure 12-2. CY8CLED04G01 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Notes
2. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
3. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

12.3 CY8CLED04DOCD1 56-Pin Part Pinout (with OCD)

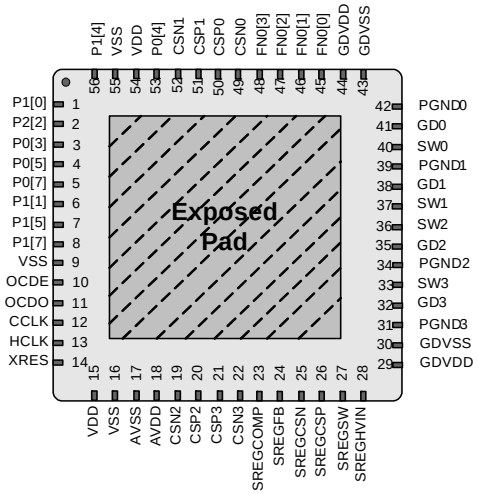
The CY8CLED04DOCD1 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-3. CY8CLED04DOCD1 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I2C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1) / Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCL (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I2C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I2C SCL (Primary)
9				V_{SS}	Digital Ground
10	I/O			OCDE	On Chip Debugger Port
11	I/O			OCDO	On Chip Debugger Port
12	I/O			CCLK	On Chip Debugger Port
13	I/O			HCLK	On Chip Debugger Port
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19			I	CSN2	Current Sense Negative Input 2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				CSP3	Current Sense Positive Input and Power Supply - CSA3
22			I	CSN3	Current Sense Negative Input 3
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[4]	Power FET Ground 3
32			O	GD3	External Low Side Gate Driver 3
33				SW3	Power Switch 3
34				PGND2[4]	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				SW2	Power Switch 2
37				SW1	Power Switch 1
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[4]	Power FET Ground 1
40				SW0	Power Switch 0
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[4]	Power FET Ground 0
43				GDV_{SS}	Gate Driver Ground
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Figure 12-3. CY8CLED04DOCD1 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Note
4. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

14. Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CLED04D0X, CY8CLED04G01, CY8CLED03D0X, CY8CLED03G01, CY8CLED02D01, and CY8CLED01D01 of the PowerPSoC device family. For the most up to date electrical specifications, confirm that you have the most recent datasheet by going to the web at http://www.cypress.com/powerpsoc. Specifications for Industrial rated devices are valid for –40 °C ≤ T_A ≤ 85 °C, T_J ≤ 115 °C and for Extended Temperature rated devices for –40 °C ≤ T_A ≤ 105 °C, T_J ≤ 125 °C, except where noted.

14.1 Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. Not all user guidelines are production tested.

Table 14-1. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	–	+115	°C	Higher storage temperatures reduces data retention time. Recommended storage temperature is 0 °C to 50 °C.
T_A	Ambient temperature with power applied	–40 –40	– –	+85 +105	°C °C	T_J ≤ 115 °C (industrial rated) T_J ≤ 125 °C (extended temperature rated)
V_{DD}, AV_{DD}, GDV_{DD}	Supply voltage on V_{DD}, AV_{DD}, and GDV_{DD}	–0.5	–	+6.0	V	Relative to V_{SS}, AV_{SS}, and GDV_{SS} respectively
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	Applies only to GPIO and FN0 pins
V_{IO2}	DC voltage applied to tristate	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{FET}	Maximum voltage from power Switch (SWx) to Power FET Ground (PGNDx)	–	–	36[13]	V	PGNDx is connected to GDV_{SS}
V_{REGIN}	Maximum voltage on SREGHVIN Pin relative to V_{SS}	–	–	36[13]	V	
V_{CSP},V_{CSN}	Maximum voltage applied to CSA pins relative to V_{SS}	–0.5	–	36[13]	V	
V_{SENSE}	Maximum input differential voltage across CSA input	–1.0	–	1.0	V	
I_{MAIO}	Maximum current into any port pin configured as analog driver	–50	–	+50	mA	
I_{MIO}	Maximum current into any port and function pin	–25	–	+50	mA	
LU	Latch up current	200	–	–	mA	JESD78A Conformal
ESD	Electrostatic discharge voltage	2000	–	–	V	Human Body Model ESD.
SR_{REGIN}	Ramp rate for the SREGHVIN pin	–	–	32	V/µs	
SR_{CSP}	Ramp rate for the CSPx pins	–	–	3.2	V/µs	
$SR_H V_{DD-FLB}$	High voltage supply ramp rate for floating load buck configuration	–	–	15	V/ms	For other topologies, to enable operation with faster ramp rates, or if the LED string voltage is < 6.5 V, see the *PowerPSoC Technical Reference Manual*.
SRV_{DD-EXT}	External V_{DD} supply ramp rate (V_{DD}, AV_{DD}, and GDV_{DD} pins)	–	–	0.2	V/µs	Applies only when powered by a source other than the Built-in Switching Regulator

Note
13. Stresses beyond the "Absolute Maximum Ratings" on page 30 may cause permanent damage to the device. You must ensure that the absolute maximum ratings are NEVER exceeded. Functional operation is not implied under any conditions beyond the "Electrical Characteristics" on page 31 onwards. Extended exposure to "Absolute Maximum Ratings" on page 30 may affect reliability of the device.

14.2 Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	–40 –40	– –	+85 +105	°C °C	$T_J \le 115$ °C (Industrial rated) $T_J \le 125$ °C (extended temperature rated)
T_J	Junction temperature	–40 –40	– –	+115 +125	°C °C	Industrial rated Extended Temperature rated

15. Electrical Characteristics

15.1 System Level

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-1. System Level Operating Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
f_{SW}	Circuit switching frequency range for hysteretic control loop	0.02	–	2	MHz	
$t_{D,MAX}$	Maximum delay time from CSA input to FET state change	– –	– –	100 115	ns ns	HV_{DD} = 24 V, I_D = 1 A, f_{SW} = 2 MHz (Industrial rated) HV_{DD} = 24 V, I_D = 1 A, f_{SW} = 2 MHz (Extended Temperature rated)
D	Output duty cycle for hysteretic controllers	5	–	95	%	f_{SW} < 0.25 MHz
E	Power converter efficiency	90	95	–	%	HV_{DD} = 24 V, I_D = 1 A, f_{SW} = 2 MHz

15.2 Chip Level

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Note See the *PowerPSoC Technical Reference Manual* for more information on the DPWMxPCF register

Table 15-2. Chip Level DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}, AV_{DD}, GDV_{DD}	Digital, analog, and gate driver supply voltage range	4.75	–	5.25	V	All should be powered from the same source.
HV_{DD}	Power converter high voltage supply range	7	–	32	V	
HV_{PINS}	Voltage range for the CSPx and SREGHVIN pins	7	–	32	V	Not all pins need to be at the same voltage level.
IV_{DD}	Supply current (V_{DD} pins), IMO = 24 MHz	–	16	50	mA	Conditions are V_{DD} = 5 V, T_J = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off.
I_AV_{DD}	Supply current (AV_{DD} pin)	–	–	25	mA	Conditions are V_{DD} = 5 V, T_J = 25 °C,

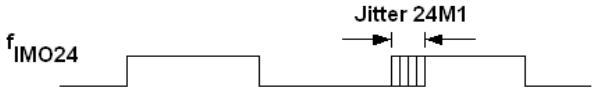
Table 15-2. Chip Level DC Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
$I_{GD}V_{DD}$	Supply current per channel (GDV_{DD} pins)	– –	– –	25 100	mA mA	Internal Power FET at 2 MHz External Gate Driver at 1 MHz, C_L = 4 nF at V_{DD} = 5 V
I_{SB}	Sleep (mode) current with POR, LVD, sleep timer, and WDT.	– –	18 30	25 550	µA µA	T_J = 25 °C, Built-in Switching Regulator disabled, DPWMxPCF = 0, Power Peripherals disabled, analog power = off T_J = 115 °C (Industrial rated) and T_J = 125 °C (Extended Temperature rated), Built-in Switching Regulator disabled, DPWMxPCF = 0, Power Peripherals disabled, analog power = OFF

Table 15-3. Chip Level AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
f_{IMO24}[15]	Internal main oscillator frequency for 24 MHz	23.04	24	24.96	MHz	–
f_{CPU1}	CPU frequency	0.093	24	24.96	MHz	–
f_{BLK}	Digital PSoC Block frequency	0	48	49.92[14]	MHz	Refer to "PSoC Core Digital Block Specifications" on page 48.
f_{32K1}	Internal low-speed oscillator frequency	15	32	64	kHz	
f_{32K_U}	Internal low-speed oscillator (ILO) untrimmed frequency	5	–	–	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PowerPSoC Technical Reference Manual for details on timing this.
DC_{ILO}	Internal low speed oscillator duty cycle	20	50	80	%	–
$Jitter_{32K}$	32 kHz period jitter	–	100	–	ns	–
$Jitter_{24M1}$	24 MHz period jitter (IMO) peak-to-peak	–	600	–	ps	–
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	30	100	ms	Power up from 0 V. See the System Resets section of the PowerPSoC Technical Reference Manual.

Figure 15-1. 24 MHz Period Jitter (IMO) Timing Diagram



Notes
14. See the individual user module datasheets for information on maximum frequencies for user modules.
15. The accuracy of the internal 24/48 MHz clocks is ± 5% over temperature variation and a voltage range of 5.0 V ± 0.25 V. No external components are required to achieve this level of accuracy. Refer to the Internal Main Oscillator (IMO) section in the PowerPSoC Technical Reference Manual.

15.3 Power Peripheral Low Side N-Channel FET

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-4. Low Side N-Channel FET DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DS}	Operating drain to source voltage	–	–	32	V	
$V_{DS,INST}$	Instantaneous drain source voltage	–	–	36	V	
I_D	Average drain current	– –	– –	1 0.5	A A	CY8CLED04/3/2/1D01 devices CY8CLED04/3D02 devices
I_{DMAX}	Maximum instantaneous repetitive pulsed current	– –	– –	3 1.5	A A	Less than 33% duty cycle for an average current of 1 A, f_{SW} = 0.1 MHz. CY8CLED04/3/2/1D01 devices Less than 33% duty cycle for an average current of 0.5 A, f_{SW} = 0.1 MHz. CY8CLED04/3D02 devices
$R_{DS(ON)}$	Drain to source ON resistance	– –	– –	0.5 1	Ω Ω	I_D = 1 A, GDV_{DD} = 5 V, T_J = 25 °C CY8CLED04/3/2/1D01 devices I_D = 0.5 A, GDV_{DD} = 5 V, T_J = 25 °C CY8CLED04/3D02 devices
I_{DSS}	Switching node to PGND leakage	– –	– –	10 250	µA µA	T_J = 25 °C T_J = 115 °C (Industrial rated) and T_J = 125 °C (Extended Temperature rated)
I_{SFET}	Supply current per channel - FET (internal gate driver)	–	–	6.25	mA	f_{SW} = 2 MHz

Table 15-5. Low Side N-Channel FET AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_R	Rise time	–	–	20	ns	I_D = 1 A, R_D = 32 Ω
t_F	Fall time	–	–	20	ns	I_D = 1 A, R_D = 32 Ω

Figure 15-2. Low Side N-Channel FET Test Circuit for I_{DSS}, $t_{R, and}$ t_F

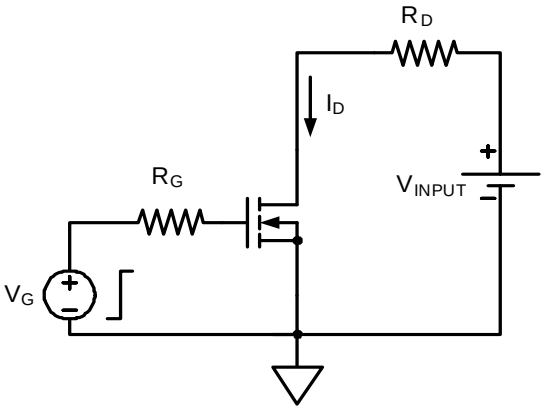


Table 15-9. Hysteretic Controller AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ON} / t_{OFF}	Minimum ON/OFF timer					
	MONOSHOT<1:0> = 00	10	–	30	ns	
	MONOSHOT<1:0> = 01	20	–	60	ns	
	MONOSHOT<1:0> = 10	40	–	110	ns	
	MONOSHOT<1:0> = 11	–	–	–	ns	Timers disabled

15.6 Power Peripheral Comparator

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

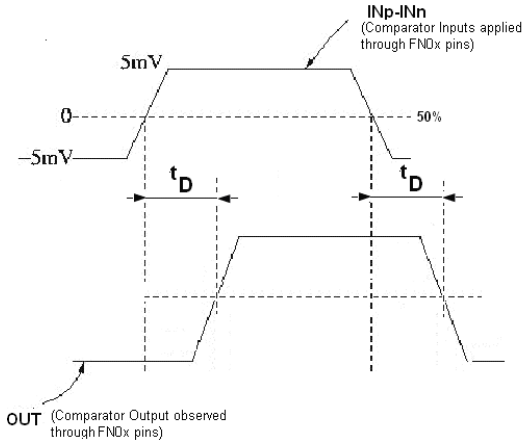
Table 15-10. Comparator DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{IN}	Input voltage range	0	–	V_{DD}	V	–
V_{IO}	Comparator input offset voltage	– – –	– – –	7.5 10 15	mV mV mV	1 V ≤ V_{ICM} ≤ 3 V (Industrial rated) 1 V ≤ V_{ICM} ≤ 3 V (Extended Temperature rated) 0 V ≤ V_{ICM} ≤ V_{DD}
V_{HYS}	Hysteresis voltage	2.5 4.5 4.5	– – –	30 11 13	mV mV mV	0 V < V_{ICM} < V_{DD} 1.5 V ≤ V_{ICM} ≤ 2.5 V (Industrial rated) 1.5 V ≤ V_{ICM} ≤ 2.5 V (Extended Temperature rated)
V_{OVDRV}	Overdrive voltage	5	–	–	mV	–
I_{SCOMP}	Supply current - comparator	–	–	650	µA	–
$V_{ICM,COMP}$	Comparator input common mode voltage range	0	–	V_{DD}	V	–

Table 15-11. Comparator AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_D	Comparator delay time (FN0[x] pin to FN0[x] pin)	–	150	–	ns	V_{OVDRV} = 5 mV, C_L = 10 pF at V_{DD} = 5 V

Figure 15-3. Comparator Timing Diagram



15.8 Power Peripheral PWM/PrISM/DMM Specification Table

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only. See the *PowerPSoC Technical Reference Manual* for more information on PWM/PrISM/DMM.

Table 15-14. PWM/PrISM/DMM DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$I_{S,Modulation}$	Supply current - PWM, PrISM, or DMM	–	–	5	mA	

Table 15-15. PWM/PrISM/DMM AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
PWM Mode						
$f_{RANGE16}$	PWM output frequency range 16-bit period	24,000,000/(256*2^{16})	–	48,000,000/2^{16}	Hz	Period value = 2^{16} –1, Min: N = 255, Max: N = 0
f_{RANGE8}	PWM output frequency range 8-bit period	24,000,000/(256*2^{8})	–	48,000,000/2^{8}	Hz	Period value = 2^{8} –1, Min: N = 255, Max: N = 0
PrISM Mode						
f_{RANGE}	PrISM output frequency range	24,000,000/(256*(2^{M}–1)	–	48,000,000/2	Hz	Min: N = 255, Maqx: N = 0, M = 2 to 16
DMM Mode						
$f_{RANGE,Dimming}$	DMM dimming frequency range	24,000,000/ (256*Max DMM Period)	–	48,000,000/(Min DMM Period)	Hz	Min DMM Period: 2 (Right Aligned), 3 (Center Aligned), 4(Left Aligned) Max DMM Period: 2^{12} (Right Aligned), 8190 (Center Aligned), 2^{12} (Left Aligned)
$f_{RANGE,Dither}$	DMM dither frequency range	(1/16)*(Min $f_{RANGE,Dimming}$)	–	(15/16)*(Max $f_{RANGE,Dimming}$)	Hz	

Figure 15-5. Built-in Switching Regulator Timing Diagram

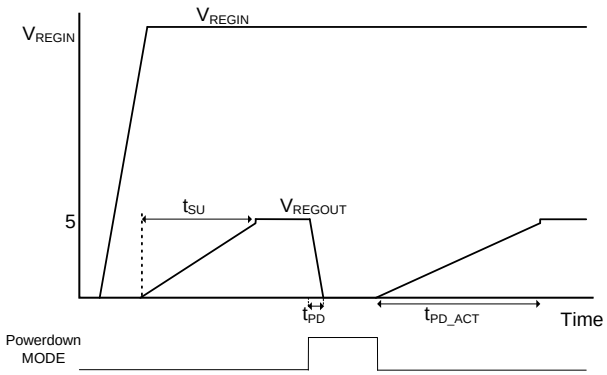
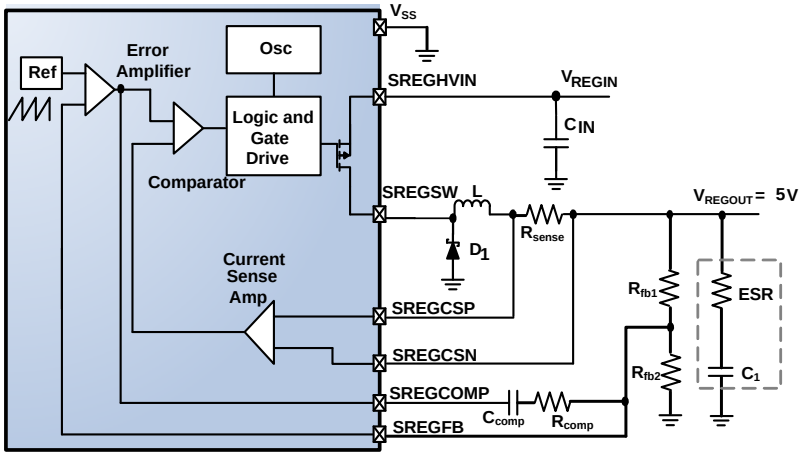


Figure 15-6. Built-in Switching Regulator



15.12 PSoC Core Operational Amplifier Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Capacitor PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block.

Table 15-23. Operational Amplifier DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 – – – – – –	 1.6 1.6 1.3 1.3 1.2 1.2	 10 15 8 13 7.5 12	 mV mV mV mV mV mV	 Industrial rated Extended temperature rated Industrial rated Extended temperature rated Industrial rated Extended temperature rated
TCV_{OSOA}	Average input offset voltage drift	–	7.0	35.0	µV / °C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	T_J = 25 °C.
V_{CMOA}	Common mode voltage range Common mode voltage range (high power or high opamp bias)	0.0 0.5	– –	V_{DD} V_{DD} – 0.5	V V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 60 60 80	 – – –	 – – –	 dB dB dB	–
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.5	 – – –	 – – –	 V V V	–
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 – – –	 – – –	 0.2 0.2 0.5	 V V V	–
I_{SOA}	Supply current (including associated analog output buffer) Power = low, opamp bias = low Power = low, opamp bias = high Power = medium, opamp bias = low Power = medium, opamp bias = high Power = high, opamp bias = low Power = high, opamp bias = high	 – – – – – –	 400 500 800 1200 2400 4600	 800 900 1000 1600 3200 6400	 µA µA µA µA µA µA	–
$PSRR_{OA}$	Supply voltage rejection ratio	52	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$.

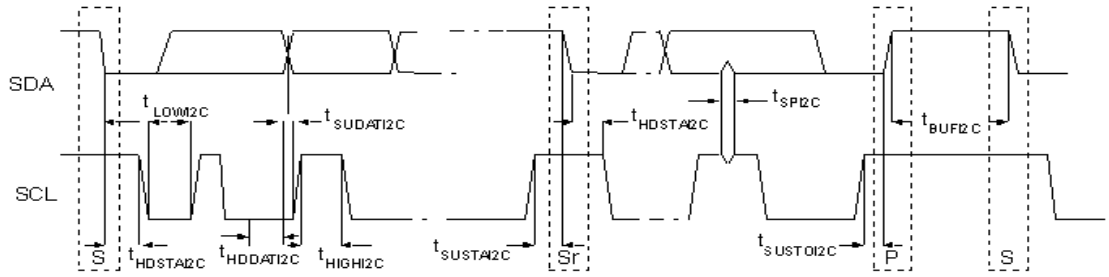
15.20 PSoC Core I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-35. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
f_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz	–
$t_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	–
t_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs	–
$t_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs	–
$t_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs	–
$t_{HDDATI2C}$	Data hold time	0	–	0	–	µs	–
$t_{SUDATI2C}$	Data setup time	250	–	100[21]	–	ns	–
$t_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs	–
t_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs	–
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	0	50	ns	–

Figure 15-8. Definition of Timing for Fast/Standard Mode on the I²C Bus



Note

21. A fast mode I²C bus device can be used in a standard mode I²C bus system, but the requirement $t_{SUDATI2} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line trmax + $t_{SUDATI2}$ = 1000 + 250 = 1250 ns (according to the standard mode I²C bus specification) before the SCL line is released.

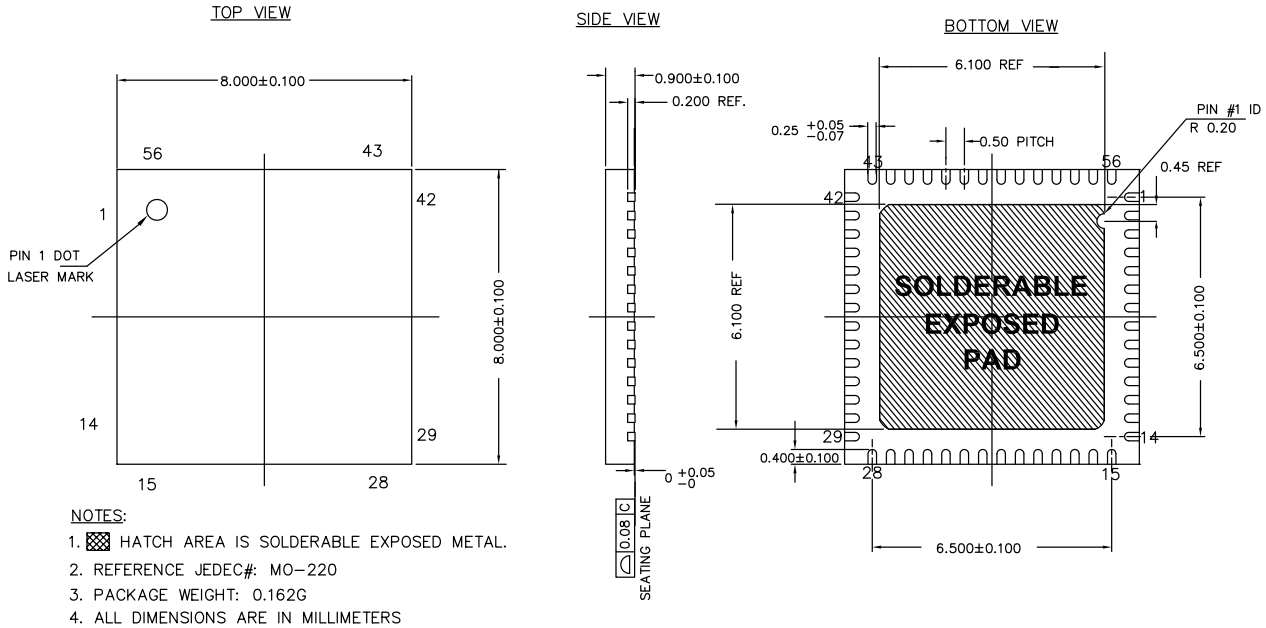
17. Packaging Information

Packaging Dimensions

This section illustrates the package specification for the CY8CLED04D0X, CY8CLED04G01, CY8CLED03D0X, CY8CLED03G01, CY8CLED02D01, and CY8CLED01D01 along with the thermal impedance for the package and solder reflow peak temperatures.

Important Note For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

Figure 17-1. 56-Pin QFN (8 × 8 × 1.0 mm)



51-85187 *G

17.1 Thermal Impedance

Package	Typical θ_{JA} [22]
56 QFN[23]	16.6 °C/W

17.2 Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Package	Minimum Peak Temperature[24]	Maximum Peak Temperature
56 QFN	240 °C	260 °C

Notes

22. $T_J = T_A + POWER \times \theta_{JA}$
23. To achieve the thermal impedance specified for the QFN package, the center thermal pad should be soldered to the PCB ground plane. The thermal model for Cypress's PowerPSoC family was simulated using a JESD51-7 standard FR4 PCB with four metal layers, 2 oz copper weight on outer layers, and 1 oz on inner layers. Thermal via array below the device is laid out according to package manufacturers' recommendations.
24. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

20. Document History Page

Document Title: CY8CLED04D01/CY8CLED04D02/CY8CLED04G01/CY8CLED03D01/CY8CLED03D02/CY8CLED03G01/ CY8CLED02D01/CY8CLED01D01, PowerPSoC® Intelligent LED Driver Document Number: 001-46319				
Revision	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2506500	ANWA/ DSG	05/20/08	New datasheet.
*A	2575708	ANWA/ AESA	10/01/08	1) Updated Logic Block Diagram with AINX label and SREGFB pin. 2) Updated Current Sense Amplifier Specification Table. 3) Updated External Gate Driver Specification Table. 4) Updated Register Table.
*B	2662774	KJV	02/19/09	Extensive changes made to content and electrical specifications.
*C	2665155	KJV/PYRS	02/25/09	Updated Notes in electrical specifications.
*D	2671254	KJV/PYRS	03/10/09	Updated sections 8, 9, and 10 on pages 14, 15, and 16.
*E	2683506	VED	04/03/09	Release to the external web site.
*F	2698529	KJV/PYRS	04/27/09	Updated Figure 15-2., and Figure 15-4..
*G	2735072	KJV	07/10/09	Added 1 and 2 channel part information.
*H	2765369	KJV	09/17/09	Updated electrical specifications.
*I	2870389	FRE/PYRS	02/01/10	Updated Absolute Maximum Ratings, DC GPIO, AC Chip-Level, and AC Programming Specifications as follows: Added $V_{REGINMAX}$ absolute maximum specification. Modified t_{WRITE} specification. Added I_{OH}, I_{OL}, DC_{ILO}, f_{32K_U}, $t_{POWERUP}$, $t_{ERASEALL}$, $t_{PROGRAM\_HOT}$, and $t_{PROGRAM\_COLD}$ specifications Updated package diagram
*J	2952677	FRE/UKK	06/15/10	Datasheet reviewed and updated with a view to improve clarity, readability and customer-friendliness. This includes language, consistency in terminology to match software and other PowerPSoC documentation, changes to reflect major changes in software such as removal of system level design addition of links to relevant collateral such as kits, technical reference manuals and application notes.
*K	3031567	FRE/UKK	09/16/10	Removed DALI in Page 1 and Page 13, and added the DALI note in Page 13. Added a note to Section 15.10 after Table 15-20 on page 38. Updated as per the new Cypress Style and datasheet template.
*L	3073506	KJV	11/08/2010	Updated datasheet to add Extended Temperature rated device CY8CLED01D01-56LTXQ
*M	3178540	KJV	02/28/2011	Updated certain specifications for Extended Temperature rated device
*N	3244595	KJV	05/04/2011	Updated description for Symbol V_{REGIN} and V_{CSP},V_{CSN} in Table 14-1. Updated Figure 15-6.
*O	3355306	KJV	08/29/2011	Replaced Table 16-20 with Table 15-20 in Built-in Switching Regulator
*P	3597060	GULA	04/24/2012	Updated Packaging Information (51-85187 from Rev *E to *F). Completing Sunset Review.
*Q	4374000	SNVN	05/08/2014	Added D1 and updated notes for the other components in Table 15-20. Updated links to reference documents in Current Sense Amplifier, Digital System, and Analog Multiplexer System sections. Added note for F_{IMO24} parameter in Table 15-3. Updated links in Worldwide Sales and Design Support based on the template.
*R	4727870	SNVN	04/16/2015	Updated Electrical Characteristics: Updated Table 15-34 (Updated details in Description column). Updated Packaging Information: spec 51-85187 – Changed revision from *F to *G. Updated Note 23. Completing Sunset Review.