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Details

XF

Product Status	Discontinued at Digi-Key
Applications	Intelligent LED Driver
Core Processor	M8C
Program Memory Type	FLASH (16KB)
Controller Series	CY8CLED
RAM Size	1K x 8
Interface	DALI, DMX512, I ² C, IrDA, SPI, UART/USART
Number of I/O	-
Voltage - Supply	4.75V ~ 5.25V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad
Supplier Device Package	56-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8cled01d01-56ltxqt

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Figure 3-2. CY8CLED04G01 Logic Block Diagram



4. PowerPSoC[®] Functional Overview

The PowerPSoC family incorporates programmable system-on-chip technology with the best in class power electronics controllers and switching devices to create easy to use power-system-on-chip solutions for lighting applications.

All PowerPSoC family devices are designed to replace traditional MCUs, system ICs, and the numerous discrete components that surround them. PowerPSoC devices feature high performance power electronics including 1 ampere 2 MHz power FETs, hysteretic controllers, current sense amplifiers, and PrISM/PWM modulators to create a complete power electronics solution for LED power management. Configurable power, analog, digital, and interconnect circuitry enables a high level of integration in a host of industrial, commercial, and consumer LED lighting applications.

This architecture integrates programmable analog and digital blocks to enable you to create customized peripheral configurations that match the requirements of each individual application. Additionally, the device includes a 24 MHz CPU, Flash program memory, SRAM data memory, and configurable I/O in a range of convenient pinouts and packages.

The PowerPSoC architecture, as illustrated in the block diagrams, consists of five main areas: PSoC core, digital system, analog system, system resources, and power peripherals, which include power FETs, hysteretic controllers, current sense amplifiers, and PrISM/PWM modulators. Configurable global busing combines all of the device resources into a complete custom system. The PowerPSoC family of devices have 10-port I/Os that connect to the global digital and analog interconnects, providing access to eight digital blocks and six analog blocks.

5. Power Peripherals

PowerPSoC is designed to operate at voltages from 7 V to 32 V, drive up to 1 ampere of current using internal MOSFET switches, and over 1 ampere with external MOSFETs.

This family of devices (CY8CLED0xD/G0y) combines up to four independent channels of constant current drivers. These drivers feature hysteretic controllers with the Programmable

System-on-Chip (PSoC) that contains an 8-bit microcontroller, configurable digital and analog peripherals, and embedded flash memory.

The CY8CLED0xD/G0y is the first product in the PowerPSoC family to integrate power peripherals to add further integration for your power electronics applications. The PowerPSoC family of intelligent power controller ICs are used in lighting applications that need traditional MCUs and discrete power electronics support. The power peripherals of the CY8CLED0xD/G0y include up to four 32 volt power MOSFETs with current ratings up to 1 ampere each. It also integrates gate drivers that enable applications to drive external MOSFETs for higher current and voltage capabilities. The controller is a programmable threshold hysteretic controller, with user-selectable feedback paths that uses the IC in current mode floating load buck, floating load buck-boost, and boost configurations.

5.1 Hysteretic Controllers

The PowerPSoC contains four hysteretic controllers. There is one hysteretic controller for each channel of the device.

The hysteretic controllers provide cycle by cycle switch control with fast transient response, which simplifies system design by requiring no external compensation. The hysteretic controllers include the following key features:

- Four independent channels
- DAC configurable thresholds
- Wide switching frequency range from 20 kHz to 2 MHz
- Programmable minimum on and off time
- Floating load buck, floating load buck-boost and boost topology controller

The reference inputs (REF_A and REF_B in Figure 5-1.) of the hysteretic controller are provided by the reference DACs as illustrated in the top level block diagram (see Figure 3-1. on page 3).

The hysteretic control function output is generated by comparing the feedback value to two thresholds. Going below the lower threshold turns the switch ON and exceeding the upper threshold turns the switch OFF as shown in Figure 5-1. The output current waveforms are shown in Figure 5-2.

The hysteretic controller also controls the minimum on-time and off-time. This circuit prevents oscillation at very high frequencies; which can be very destructive to output switches.

The output to the gate drivers is gated by the Trip, DIM and Enable signals. The Enable signal is a direct result of the enable bit in the control register for the hysteretic controller.

The Trip signal can be any digital signal that follows TTL logic (logic high and logic low). It is an active high input.

The DIM Modulation signal is the output of the dedicated modulators that are present in the power peripherals, or any other digital modulation signal.

Figure 5-1. Generating Hysteretic Control Function Output





6. PSoC Core

The PSoC core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable general purpose I/O(GPIO).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with up to 20 vectors to simplify programming of real time embedded events. The program execution is timed and protected using the included sleep and watchdog timers (WDT) time and protect program execution.

Memory encompasses 16 K of flash for program storage, 1 K of SRAM for data storage, and up to 2 K of EEPROM emulated using the flash. Program flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

The PSoC device incorporates flexible internal clock generators, including a 24 MHz internal main oscillator (IMO) accurate to 4 percent over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz internal low-speed oscillator (ILO) is provided for the sleep timer and WDT. The clocks, together with programmable clock dividers (as a system resource), provide the flexibility to integrate almost any timing requirement into the PowerPSoC device.

PowerPSoC GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

6.1 Digital System

The digital system contains eight digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

Digital peripheral configurations include:

- DMX512
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8-bit with selectable parity
- SPI master and slave
- I²C master, slave, and multi-master
- Cyclical redundancy checker/generator (8 to 32 bit)
- IrDA
- Pseudo random sequence generators (8 to 32 bit)

Note The DALI interface is supported through the use of a combination of the above mentioned user modules. For more details on the exact configuration and an example project, refer to the application note, PowerPSoC Firmware Design Guidelines, Lighting Control Interfaces - AN51012.

The digital blocks can be connected to any GPIO through a series of global buses that route any signal to any pin. The buses

also allow signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

There are four digital blocks in each row. This allows optimum choice of system resources for your application.





6.2 Analog System

The analog system contains six configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PowerPSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (up to 2, with 6 to 12-bit resolution, selectable as incremental, Delta Sigma, and SAR)
- Filters (2 and 4 pole band-pass, low-pass, and notch)
- Amplifiers (up to 2, with selectable gain to 48x)
- Instrumentation amplifiers (1 with selectable gain to 93x)
- Comparators (up to 2, with 16 selectable thresholds)
- DACs (up to 2, with 6 to 9-bit resolution)
- Multiplying DACs (up to 2, with 6 to 9-bit resolution)
- High current output drivers (two with 30 mA drive as a PSoC core resource)
- 1.3 V reference (as a system resource)
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible



7. Applications

The PowerPSoC family of devices can be used to add hysteretic current control capability to power applications. The devices can be used to control current in devices such as LEDs, heating elements, and solenoids. For LED applications, all high-brightness LEDs (HBLEDs) can be controlled using the PowerPSoC. The following figures show examples of applications in which the PowerPSoC family of devices adds intelligent power control for power applications.



Figure 7-1. LED Lighting with RGGB Color Mixing Configured as Floating Load Buck Converter



12. Pin Information

12.1 CY8CLED04D0x 56-Pin Part Pinout (without OCD)

The CY8CLED04D01 and CY8CLED04D02 PowerPSoC devices are available with the following pinout information. Every port pin (labeled with a "P" and "FN0") is capable of Digital I/O.

Table 12-1. CY8CLED04D0x 56-Pin Part Pinout (QFN)

Pin	Pin Type		- Nama Description F	Figure 12-1. CY8CLED04D0x 56-Pin PowerPSoC Device								
No.	Digital Rows	Analog Columns	Power Peripherals	Name	Description							
1	I/O	I		P1[0]	GPIO/I ² C SDA (Secondary)/ ISSP SDATA				QF	N Тор	View	
2	I/O	-		P2[2]	GPIO/Direct Switch Cap connection							
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)							
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap				1[4] SS 7[DD	EP 1NS 1NS 1NS 1NS 1NS 1NS 1NS 1NS 1NS 1NS	NNC NNC NNC NNC NNC NNC NNC NNC NNC NNC	
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap			ĺ				
6	I/O	I		P1[1]	GPIO/I ² C SCL (Secondary)/ISSP SCLK			P1[0] P2[2]			42 P GND0 41 G D0	
7	I/O	I		P1[5]	GPIO/I ² C SDA (Primary)			P0[3] P0[5]		111	40 SW0 39 PGND1	
8	I/O	I		P1[7]	GPIO/I ² C SCL (Primary)			P0[7]	5	111	38 G D1	
9				V _{SS}	Digital Ground			P1[1]	= 6	/Exno	sed 37 SW1	
10				NC	No Connect			P 1[5] P1[7]		6	36 SW2	
11				NC	No Connect			VSS		/ Fai	33 GD2 34 GD2	
12				NC	No Connect			NC	1 0		33 = SW3	
13				NC	No Connect			NC NC		! / /	32 GD3	
14	Ι			XRES	External Reset	1		NC		///	31 PGND3 30 GDVSS	
15				V _{DD}	Digital Power Supply	1		XRES	■14 ■14			
16				V _{SS}	Digital Ground	1						
17				AV _{SS}	Analog Ground				_ v v c	9 0 0 C		
18				AVDD	Analog Power Supply					CSF	BHVIE BEGE	
19			I	CSN2	Current Sense Negative Input - CSA2			* ~	onnoot E	vneed		
20				CSP2	Current Sense Positive Input and Power Supply - CSA2		* Connect Exposed Pad to				rad to FGNDX	
21				CSP3	Current Sense Positive Input and Power Supply - CSA3							
22			I	CSN3	Current Sense Negative Input 3							
23				SREGCOMP	Voltage Regulator Error Amp Comp							
24			I	SREGFB	Regulator Voltage Mode Feedback Node							
25			I	SREGCSN	Current Mode Feedback Negative							
26			I	SREGCSP	Current Mode Feedback Positive							
27			0	SREGSW	Switch Mode Regulator OUT							
28				SREGHVIN	Switch Mode Regulator IN							
29				GDV _{DD}	Gate Driver Power Supply	Din		Туре	•			
30				GDV _{SS}	Gate Driver Ground	No.	Digital Rows	Analog Columns	Power Peripherals	Name	Description	
31				PGND3 ^[1]	Power FET Ground 3	44				GDV _{DD}	Gate Driver Power Supply	
32			0	GD3	External Low Side Gate Driver 3	45			I/O	FN0[0]	Function I/O	
33				SW3	Power Switch 3	46			I/O	FN0[1]	Function I/O	
34				PGND2 ^[1]	Power FET Ground 2	47			I/O	FN0[2]	Function I/O	
35			0	GD2	External Low Side Gate Driver 2	48			I/O	FN0[3]	Function I/O	
36				SW2	Power Switch 2	49				CSN0	Current Sense Negative Input 0	
37				SW1	Power Switch 1	50				CSP0	Current Sense Positive Input and Power Supply - CSA0	
38			0	GD1	External Low Side Gate Driver 1	51				CSP1	Current Sense Positive Input and Power Supply - CSA1	
39				PGND1 ^[1]	Power FET Ground 1	52		I	CSN1	Current Sense Negative Input 1		
40				SW0	Power Switch 0	53	I/O	Ι		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output	
41			0	GD0	External Low Side Gate Driver 0	54				V _{DD}	Digital Power Supply	
42				PGND0 ^[1]	Power FETGround 0	55				V _{SS}	Digital Ground	
43				GDV _{SS}	Gate Driver Ground	56	I/O	I		P1[4]	GPIO / External Clock Input	

Note

1. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.



12.2 CY8CLED04G01 56-Pin Part Pinout (without OCD)

The CY8CLED04G01 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a "P" and "FN0") is capable of Digital I/O.

Pin		Туре	l.			Fig	6-Pin PowerPSoC Device				
No.	Digital Rows	Analog Columns	Power Peripherals	Name	Description						
1	I/O	I		P1[0]	GPIO/I ² C SDA (Secondary)/ ISSP SDATA						
2	I/O	-		P2[2]	GPIO/Direct Switch Cap connection				QF	N Top	View
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)					•	0. %
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap			_	P1[4] VSS VDD P0[4] CSN1	CSP1 CSP0 CSN0 FN0[3]	E FN0[2] FN0[0] E FN0[0] E FN0
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap			P1[0] = 1	56 6 55 54 53 53	51 5 50 1 49 1 48 1	4 9 9 9 7 7 8 42 PGND0
6	I/O	I		P1[1]	GPIO/I ² C SCL (Secondary)/ ISSP SCLK			P2[2] = 2 P0[3] = 3	111		41= GD0 40= DNC
7	I/O	1		P1[5]	GPIO/I ² C SDA (Primary)	-		P0[5] = 4	111		39= PGND1
8	I/O			P1[7]	GPIO/I ² C SCL (Primary)			P1[1] = 6	111		38 GDT 37 DNC
9				Vee	Digital Ground			P1[5] 🗖 7	E CONTRACTOR	xpose	d 36 DNC
10				NC	No Connect	-		P1[7] = 8		⁄ Þ,ad,⁄	35 = GD2
11				NC	No Connect	-				/ / /	
12				NC	No Connect	-			111	111	33 DNC 32 GD3
13				NC	No Connect	-		NC = 12	111	' / / /	31 PGND3
14	1			XRES	External Reset	-		NC 13			30 GDVSS
15				Vaa	Digital Power Supply	-		ARES 14	1515	3 5 5 5	29 = GDVDD
16				VDD Vaa	Digital Ground	-				0 0 0 0	
17				VSS AV/	Analog Ground	-			/DD /S S /S S /S S /S S /D D	SP3 SN3 MP	SSN
18				AV _{SS}	Analog Bround	-			° ĕ ≩ ö	ប៉ ប៉ ប៉ ប្តូ	E C C C C C C C C C C C C C C C C C C C
10			1	CSN2	Current Sense Negative Input 2	-				REC	S S S S S S S S S S S S S S S S S S S
20			I		Current Sense Regative Input and	-				S	
20				0052	Power Supply - CSA2					_	
21				CSP3	Current Sense Positive Input and Power Supply - CSA3			* C	Connect E	xposed	d Pad to PGNDx
22			I	CSN3	Current Sense Negative Input 3						
23				SREGCOMP	Voltage Regulator Error Amp Comp						
24			I	SREGFB	Regulator Voltage Mode Feedback Node						
25			I	SREGCSN	Current Mode Feedback Negative						
26			I	SREGCSP	Current Mode Feedback Positive						
27			0	SREGSW	Switch Mode Regulator OUT						
28				SREGHVIN	Switch Mode Regulator IN						
29				GDV _{DD}	Gate Driver Power Supply	Pin		Туре	1		
30				GDV _{SS}	Gate Driver Ground	No.	Digital Rows	Analog Columns	Power Peripherals	Name	Description
31				PGND3 ^[3]	Power FET Ground 3	44	L	ļ		GDV _{DD}	Gate Driver Power Supply
32			0	GD3	External Low Side Gate Driver 3	45			I/O	FN0[0]	Function I/O
33				DNC ^[2]	Do Not Connect	46			I/O	FN0[1]	Function I/O
34				PGND2 ^[3]	Power FET Ground 2	47			I/O	FN0[2]	Function I/O
35			0	GD2	External Low Side Gate Driver 2	48			I/O	FN0[3]	Function I/O
36				DNC ^[2]	Do Not Connect	49	49 I CSN0 Current Sense Neg			Current Sense Negative Input 0	
37				DNC ^[2]	Do Not Connect	50 CSP0 Current Sense Positive Power Supply - CSA0			Current Sense Positive Input and Power Supply - CSA0		
38			0	GD1	External Low Side Gate Driver 1	51 CSP1 Current Sense Positive II Power Supply - CSA1				Current Sense Positive Input and Power Supply - CSA1	
39				PGND1 ^[3]	Power FET Ground 1	52 I CSN1 Current Sense Negative			Current Sense Negative Input 1		
40				DNC ^[2]	Do Not Connect	53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
41			0	GD0	External Low Side Gate Driver 0	54		İ		V _{DD}	Digital Power Supply
42				PGND0 ^[3]	Power FET Ground 0	55				V _{SS}	Digital Ground
43				GDV _{SS}	Gate Driver Ground	56	I/O	I		P1[4]	GPIO / External Clock Input

Table 12-2. CY8CLED04G01 56-Pin Part Pinout (QFN)

Notes

Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
 All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.



12.4 CY8CLED03D0x 56-Pin Part Pinout (without OCD)

The CY8CLED03D01 and CY8CLED03D02 PowerPSoC devices are available with the following pinout information. Every port pin (labeled with a "P" and "FN0") is capable of Digital I/O.

Table 12-4. CY8CLED03D0x 56-Pin Part Pinout (QFN)

Din		Туре	•			Fig	ure 1	2-4
No.	Digital Rows	Analog Columns	Power Peripherals	Name	Description	-		
1	I/O	1		P1[0]	GPIO/I ² C SDA (Secondary)/ ISSP SDATA			
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection			
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)			
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap			D4
5	I/O	Ι		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap			P1[0 P2[2
6	I/O	I	P1[1] GPIO/I ² C SCL (Secondary)/ ISSP SCLK				P0[: P0[: P0[]	
7	I/O	I	P1[5] GPIO/I ² C SDA (Primary)		1		P1[
8	I/O	I	P1[5] GPI0/I ⁺ C SDA (Primary) P1[7] GPI0/I ² C SCL (Primary)		1		P1[
9			P1[7] GPIO/I ² C SCL (Primary) V _{SS} Digital Ground		1		P1[7	
10				NC	No Connect	1		N
11				NC	No Connect	1		N
12				NC	No Connect			N
13				NC	No Connect			XRE
14	I			XRES	External Reset	1		/
15				V _{DD}	Digital Power Supply	1		
16				V _{SS}	Digital Ground	1		
17				AV _{SS}	Analog Ground			
18				AV _{DD}	Analog Power Supply	1		
19	19 I		I	CSN2	Current Sense Negative Input - CSA2			
20				CSP2	Current Sense Positive Input and Power Supply - CSA2			
21				DNC ^[5]	Do Not Connect			
22				DNC ^[5]	Do Not Connect			
23				SREGCOMP	Voltage Regulator Error Amp Comp			
24			I	SREGFB	Regulator Voltage Mode Feedback Node			
25			I	SREGCSN	Current Mode Feedback Negative			
26			I	SREGCSP	Current Mode Feedback Positive			
27			0	SREGSW	Switch Mode Regulator OUT			
28				SREGHVIN	Switch Mode Regulator IN			
29				GDV _{DD}	Gate Driver Power Supply	Pin		
30				GDV _{SS}	Gate Driver Ground	No.	Digital Rows	An: Colu
31				PGND3 ^[0]	Power FET Ground 3	44		
32				DNC ^[5]	Do Not Connect	45		
33				DNC ^[3]	Do Not Connect	46		
34				PGND2 ^[0]	Power FET Ground 2	47		
35			0	GD2	External Low Side Gate Driver 2	48		
36				SW2	Power Switch 2	49		
37				SW1	Power Switch 1	50		
38			0	GD1	External Low Side Gate Driver 1	51		
39				PGND1 ^[6]	Power FET Ground 1	52		
40				SW0	Power Switch 0	53	I/O	
41			0	GD0	External Low Side Gate Driver 0	54		
42		PGND0 ^[6] Power FETGround 0				55		
12				GDVaa	Gate Driver Ground	56	1/0	

CY8CLED03D0x 56-Pin PowerPSoC Device

QFN Top View



* Connect Exposed Pad to PGNDx

-										
29		GDV _{DD}	Gate Driver Power Supply	Pin		Туре				
30		GDV _{SS}	Gate Driver Ground		Digital Rows	Analog Power Columns Periphera		Name	Description	
31		PGND3 ^[6]	Power FET Ground 3	44				GDV_{DD}	Gate Driver Power Supply	
32		DNC ^[5]	Do Not Connect	45			I/O	FN0[0]	Function I/O	
33		DNC ^[5]	Do Not Connect	46			I/O	FN0[1]	Function I/O	
34		PGND2 ^[6]	Power FET Ground 2	47			I/O	FN0[2]	Function I/O	
35	0	GD2	External Low Side Gate Driver 2	48			I/O	FN0[3]	Function I/O	
36		SW2	Power Switch 2	49			-	CSN0	Current Sense Negative Input 0	
37		SW1	Power Switch 1	50				CSP0	Current Sense Positive Input and Power Supply - CSA0	
38	0	GD1	External Low Side Gate Driver 1	51				CSP1	Current Sense Positive Input and Power Supply - CSA1	
39		PGND1 ^[6]	Power FET Ground 1	52			-	CSN1	Current Sense Negative Input 1	
40		SW0	Power Switch 0	53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output	
41	0	GD0	External Low Side Gate Driver 0	54				V _{DD}	Digital Power Supply	
42		PGND0 ^[6]	Power FETGround 0	55				V _{SS}	Digital Ground	
43		GDV _{SS}	Gate Driver Ground	56	I/O	I		P1[4]	GPIO / External Clock Input	

Notes

6. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

^{5.} Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.



12.6 CY8CLED02D01 56-Pin Part Pinout (without OCD)

The CY8CLED02D01 PowerPSoC devices are available with the following pinout information. Every port pin (labeled with a "P" and "FN0") is capable of Digital I/O.

Pin	Туре			Fig	ure		
No.	Digital Rows	Analog Columns	Power Peripherals	Name	Description		
1	I/O	Ι		P1[0]	GPIO/I ² C SDA (Secondary)/ ISSP SDATA		
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection		
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)		
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap		
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap		
6	I/O	I		P1[1]	GPIO/I ² C SCLK (Secondary)/ ISSP SCLK		
7	I/O	1		P1[5]	GPIO/I ² C SDA (Primary)		
8	I/O			P1[7]	GPIO/I ² C SCL (Primary)		
9				V _{SS}	Digital Ground		
10				NC	No Connect		
11				NC	No Connect		
12			NC	No Connect			
13				NC	No Connect		
14	1	1		XRES	External Reset		
15				Vpp	Digital Power Supply		
16				Voc	Digital Ground		
17				AVec	Analog Ground		
18				AVpp	Analog Power Supply		
19				DNC ^[9]	Do Not Connect		
20				DNC ^[9]	Do Not Connect		
21				DNC ^[9]	Do Not Connect		
22				DNC ^[9]	Do Not Connect		
23				SREGCOMP	Voltage Regulator Error Amp Comp		
24			I	SREGFB	Regulator Voltage Mode Feedback Node		
25			I	SREGCSN	Current Mode Feedback Negative		
26			I	SREGCSP	Current Mode Feedback Positive		
27			0	SREGSW	Switch Mode Regulator OUT		
28				SREGHVIN	Switch Mode Regulator IN		
29				GDV _{DD}	Gate Driver Power Supply	Din	
30				GDV _{SS}	Gate Driver Ground	No.	Dig Ro
31				PGND3 ^[10]	Power FET Ground 3	44	
32				DNC ^[9]	Do Not Connect	45	
33				DNC ^[9]	Do Not Connect	46	
34				PGND2 ^[10]	Power FET Ground 2	47	
35				DNC ^[9]	Do Not Connect	48	
36				DNC ^[9]	Do Not Connect	49	
37				SW1	Power Switch 1	50	
38			0	GD1	External Low Side Gate Driver 1	51	
39				PGND1 ^[10]	Power FET Ground 1	52	
40				SW0	Power Switch 0	53	I/
41			0	GD0	External Low Side Gate Driver 0	54	
42				PGND0 ¹¹⁰	Power FETGround 0	55	

Table 12-6. CY8CLED02D01 56-Pin Part Pinout (QFN)

e 12-6. CY8CLED02D01 56-Pin PowerPSoC Device





* Connect Exposed Pad to PGNDx

~ '		0	01120011	ountoir modo regulator oor						
28			SREGHVIN	Switch Mode Regulator IN						
29			GDV _{DD}	Gate Driver Power Supply	Pin Type					
30			GDV _{SS}	Gate Driver Ground	No.	Digital Rows	Analog Columns	Power Peripherals	Name	Description
31			PGND3 ^[10]	Power FET Ground 3	44				GDV _{DD}	Gate Driver Power Supply
32			DNC ^[9]	Do Not Connect	45			I/O	FN0[0]	Function I/O
33			DNC ^[9]	Do Not Connect	46			I/O	FN0[1]	Function I/O
34			PGND2 ^[10]	Power FET Ground 2	47			I/O	FN0[2]	Function I/O
35			DNC ^[9]	Do Not Connect	48	18 I/O FN0[3] Funct		Function I/O		
36			DNC ^[9]	Do Not Connect	49			I	CSN0	Current Sense Negative Input 0
37			SW1	Power Switch 1	50				CSP0	Current Sense Positive Input and Power Supply - CSA0
38		0	GD1	External Low Side Gate Driver 1	51				CSP1	Current Sense Positive Input and Power Supply - CSA1
39			PGND1 ^[10]	Power FET Ground 1	52				CSN1	Current Sense Negative Input 1
40			SW0	Power Switch 0	53	I/O	Ι		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
41		0	GD0	External Low Side Gate Driver 0	54				V _{DD}	Digital Power Supply
42			PGND0 ^[10]	Power FETGround 0	55				V _{SS}	Digital Ground
43			GDV _{SS}	Gate Driver Ground	56	I/O			P1[4]	GPIO / External Clock Input

Notes

9. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device. 10. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.



12.7 CY8CLED01D01 56-Pin Part Pinout (without OCD)

The CY8CLED01D01 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a "P" and "FN0") is capable of Digital I/O.

Table 12-7. CY8CLED01D01 56-Pin Part Pinout (QFN)

Din		Туре				Fig	ure
No.	Digital Rows	Analog Columns	Power Peripherals	Name	Description		
1	I/O	I	-	P1[0]	GPIO/I ² C SDA (Secondary)/ ISSP SDATA		
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection		
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)		
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap		
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap		
6	I/O	I		P1[1]	GPIO/I ² C SCLK (Secondary)/ ISSP SCLK		
7	I/O	I		P1[5]	GPIO/I ² C SDA (Primary)		
8	I/O	I		P1[7]	GPIO/I ² C SCL (Primary)		
9		V _{SS} Digital Ground NC No Connect					
10				NC	No Connect		
11				NC	No Connect		
12				NC	No Connect		
13				NC	No Connect		
14	Ι			XRES	External Reset		
15				V _{DD}	Digital Power Supply		
16				V _{SS}	Digital Ground		
17	AV _{SS}		AV _{SS}	Analog Ground			
18				AV _{DD}	Analog Power Supply		
19			DNC ^[11]	Do Not Connect			
20		DNC ^[11] Do Not Connect DNC ^[11] Do Not Connect DNC ^[11] Do Not Connect		Do Not Connect			
21				DNC ^[11]	Do Not Connect		
22				DNC ^[11]	Do Not Connect		
23				SREGCOMP	Voltage Regulator Error Amp Comp		
24			I	SREGFB	Regulator Voltage Mode Feedback Node		
25			I	SREGCSN	Current Mode Feedback Negative		
26			I	SREGCSP	Current Mode Feedback Positive		
27			0	SREGSW	Switch Mode Regulator OUT		
28				SREGHVIN	Switch Mode Regulator IN		
29				GDV _{DD}	Gate Driver Power Supply	Pin	
30				GDV _{SS}	Gate Driver Ground	No.	Digit Row
31				PGND3 ^[12]	Power FET Ground 3	44	
32				DNC ^[11]	Do Not Connect	45	
33				DNC ^[11]	Do Not Connect	46	
34				PGND2 ^[12]	Power FET Ground 2	47	
35				DNC ^[11]	Do Not Connect	48	
36				DNC ^[11]	Do Not Connect	49	
37				DNC ^[11]	Do Not Connect	50	
38				DNC ^[11]	Do Not Connect	51	
39				PGND1 ^[12]	Power FET Ground 1	52	
40				SW0	Power Switch 0	53	I/O
41			0	GD0	External Low Side Gate Driver 0	54	
42				PGND0 ^[12]	Power FET Ground 0	55	

12-7. CY8CLED01D01 56-Pin PowerPSoC Device

QFN Top View



* Connect Exposed Pad to PGNDx

28	SREGHVIN	Switch Mode Regulator IN						
29	GDV _{DD}	Gate Driver Power Supply	Pin		Туре	•		
30	GDV _{SS}	GDV _{SS} Gate Driver Ground		Digital Rows	Analog Columns	Power Peripherals	Name	Description
31	PGND3 ^[12]	Power FET Ground 3	44				GDV_{DD}	Gate Driver Power Supply
32	DNC ^[11]	Do Not Connect	45			I/O	FN0[0]	Function I/O
33	DNC ^[11]	Do Not Connect	46			I/O	FN0[1]	Function I/O
34	PGND2 ^[12]	Power FET Ground 2	47			I/O	FN0[2]	Function I/O
35	DNC ^[11]	Do Not Connect	48			I/O	FN0[3]	Function I/O
36	DNC ^[11]	Do Not Connect	49				CSN0	Current Sense Negative Input 0
37	DNC ^[11]	Do Not Connect	50				CSP0	Current Sense Positive Input and Power Supply - CSA0
38	DNC ^[11]	Do Not Connect	51				DNC ^[11]	Do Not Connect
39	PGND1 ^[12]	Power FET Ground 1	52				DNC ^[11]	Do Not Connect
40	SW0	Power Switch 0	53	I/O	Ι		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
41	O GD0	External Low Side Gate Driver 0	54				V _{DD}	Digital Power Supply
42	PGND0 ^[12]	Power FET Ground 0	55				V _{SS}	Digital Ground
43	GDV _{SS}	Gate Driver Ground	56	I/O	I		P1[4]	GPIO / External Clock Input

Notes

11. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device. 12. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.



13.5 Register Map Bank 1 Table: User Space

PRTGOM 00 RW CSA0_CR 40 RW ASCICGEN 801 RW CMPCH2 CR C0 RW PRTGOM 00 RW 42 ASCICGEN 82 RW CMPCH2 CR C2 RW PRTGOM 00 RW CSA1_CR 42 ASCICGEN 83 RW CMPCH2 CR C2 RW PRTGOM 06 RW CSA1_CR 46 RW ASSICTCEN 86 RW CMPENTLOCR C6 RW PRTTCOM 06 RW CSA1_CR 46 RW ASSICTCEN 86 RW CMPENTLOCR C6 RW PRTZOM 06 RW CSA1_CR 48 RW ASSICTCEN 87 RW CMPENTLOCR C6 RW PRTZOM 06 RW CSA1_CR 46 RW ASSICTCEN 87 CMPENTLOCR C6 RW PRTZOM 06 RW CSA1_CR 46 RW CM	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PHTCOM 01 RW LMM 41 ASCICACE 81 RW CMMPCH2_CR C1 RW PHTCOD 03 RW CASNI_CR 42 ASCICACE 82 RW CMMPCH2_CR C3 RW PHTCOD 03 RW CASNI_CR 44 RW ASCICACE 82 RW CMMPGH2_CR C3 RW PHTICO 03 RW CASNI_CR 46 RW ASDITCHS 88 RW CMMPGHX1_CR C6 RW PHTICO 06 RW CASA_CR 46 RW ASDITCHS 89 RW CMMPGHX1_CR C6 RW PHTICO 06 RW CASA_CR 46 RW ASDITCHS 88 CMMPGHX1_CR CA RW PHTICO 06 RW CASA_CR 46 RW ASDITCHS 88 CMMPGHX1_CR CA CA PHTICO 06 RW CASA_CASA RW ASDITCHS	PRT0DM0	00	RW	CSA0_CR	40	RW	ASC10CR0	80	RW	CMPCH0_CR	C0	RW
PHTGC0 0.0 RW 42 ASCIC/ASC 82 RW CMP/CH2, CR C2 RW PHTGC1 0.6 RW CSA1_CR 44 RW ASCIC/ASC 83 RW CMP/CH2, CR 64 RW PHTIC01 0.6 RW CSA1_CR 44 RW ASCIC/ASC 83 RW CMP/SHX/CR C6 RW PHTIC01 0.6 RW CMA 44 RW ASSIC/ASC 87 RW CMP/SHX/CR C6 RW PHTIC01 0.0 RW CSA2_CR 48 RW RM CA RW CMA RW CA CA CA CA RW CA CA RW CA	PRT0DM1	01	RW		41		ASC10CR1	81	RW	CMPCH2_CR	C1	RW
PPRTOCI 03 RW CAM_COR 43 RW CAMPARADE, CR C3 RW PRTICOL 06 RW CAM_COR 46 RW CAMPARADE, CR C3 RW PRTICOL 06 RW CAMPARADE, CR C6 RW CAMPARADE, CR C6 RW PRTICOL 06 RW CAMPARADE, CR C6 RW CAMPARADE, CR C6 RW PRTICOL 06 RW CAAPAC, CR 48 RW ASDITCR2 68 CAMPARAT, CR C8 RW PRTICOL 06 RW CAAA RW RW CAA CAA RW RW CAA CAA RW RW CAA CAA RW RW CAA CAA CAA CAA CAA RW <td< td=""><td>PRT0IC0</td><td>02</td><td>RW</td><td></td><td>42</td><td></td><td>ASC10CR2</td><td>82</td><td>RW</td><td>CMPCH4_CR</td><td>C2</td><td>RW</td></td<>	PRT0IC0	02	RW		42		ASC10CR2	82	RW	CMPCH4_CR	C2	RW
PHITION BM DOM CAMILOR BM PM ASSITTAN BM DOM DATA PHTTION GO RW AS AS GO RW CMPBANCLOR CG RW PHTTION GO RW CAS AS AS CMPBANCLOR CF RW PHTZON GO RW CAS CAS RW CMPBANCLOR CF RW PHTZON GO RW CAS CAS RW CMPBANCLOR CG RW PHTZOS GO RW CAS CAS RW AS CAS CMPANCLOR CAS CAS </td <td>PRT0IC1</td> <td>03</td> <td>RW</td> <td>0011.05</td> <td>43</td> <td>514</td> <td>ASC10CR3</td> <td>83</td> <td>RW</td> <td>CMPCH6_CR</td> <td>C3</td> <td>RW</td>	PRT0IC1	03	RW	0011.05	43	514	ASC10CR3	83	RW	CMPCH6_CR	C3	RW
metrical des Des Des Des Rev Cale Cale Cale Cale <t< td=""><td>PRI1DM0</td><td>04</td><td>RW</td><td>CSA1_CR</td><td>44</td><td>RW</td><td>ASD11CR0</td><td>84</td><td>RW</td><td>CMPBNK8_CR</td><td>C4</td><td>RW</td></t<>	PRI1DM0	04	RW	CSA1_CR	44	RW	ASD11CR0	84	RW	CMPBNK8_CR	C4	RW
PRTTOCIO OF PM CAD ADDITION BP TW CADEWORD COL NW PRTTZOM OF RW CSA2 CR 48 RW BB CADEWORD CSA RW PRTZOM OF RW CSA2 CR 48 RW CAD RA RW CAD CAD RW CAD CAD RW CAD CAD CAD RW CAD CA	PRT1DM1	05	RW		45		ASD11CR1	85	RW	CMPBNK9_CR	05	RW
PRITODIN Gold RW CADICAS BN RW CADICAS BN RW CADICAS BN CADIPARX3.CR CG RW PRIZON 40 RW 48 PN BN CADIPARX3.CR CG RW PRIZON 40 RW 48 PN BN CADIPARX3.CR CG RW PN00M 00 RW CASA_CR 46 PN BN C CD CD PN00M 00 RW CASA_CR 40 PN BN C CD	PRTICU PRTIC1	06	RW		46		ASDITCR2	80 97	RW	CMPBINK10_CR	C6	RW
PHT2GC 0 RW Conc. 4 NN A NN A CMPPRIA CR CMPPRIA PHT2GC 06 RW AA FW AA FW AA FW AA FW AA FW AA FW CA CC FW CC CC FW CC CC FW FW CC CC FW CC CC FW FW CC CC FW FW CC FW FW CC FW	PRT2DM0	07	RW	CSA2 CR	47	RW/	ASDITCKS	88	NVV	CMPBNK12_CR	C8	RW
PRT3C10 DA FW AA PA PA SA PA CA TO PRT3C1 DB FW	PRT2DM0	00	RW	OOA2_OIX	40	1.00		89		CMPBNK13_CR	00 C9	RW
PRTAID 0B NW CB CB CB CB CC CB PNDDMI 0C RW CS3_CR 4C FW 86 - CC CC PNDCC 0E RW CS3_CR 4D FW 86 - CC CF FNDCC 0F RW CA 4F - 88 - CC CF FNDCC 0F RW CA 51 ASD20CR0 90 RW CD_L N 00 RW 11 C CC S3 ASD20CR0 91 RW GDL_L 01 RW 13 C C S3 ASD20CR0 93 RW GDL_C.OU 02 RW 14 C S5 ASC21CR1 96 RW HYSCTRICR 06 RW 16 C S5 ASC21CR2 98 MUX_CR1 05 RW 17 C <td>PRT2IC0</td> <td>00 0A</td> <td>RW</td> <td></td> <td>4A</td> <td></td> <td></td> <td>8A</td> <td></td> <td>onn Brittio_ont</td> <td>CA</td> <td></td>	PRT2IC0	00 0A	RW		4A			8A		onn Brittio_ont	CA	
FNDOM OC RW CSAJCR 4C RW BC CC CC FNDOM OD RW 440 - 86 - CC CC FNDOC OE RW - 45 - 86 - CC - FNDC1 OF RW AF - 87 - CC - FNDC1 OF RW AF 450 - 880 RW GDL_0.N 00 RW 10 - - 53 - ASDZCR2 92 RW GDL_0.0 02 RW 11 - - 55 - ASCZCR3 93 RW HYSCTLR0CR D6 RW 16 - - 56 - ASCZCR3 97 RW HYSCTLR0CR D6 RW 16 - - 56 - ASCZCR3 97 RW AULX_CR1 D6 <td< td=""><td>PRT2IC1</td><td>0B</td><td>RW</td><td></td><td>4B</td><td></td><td></td><td>8B</td><td></td><td></td><td>CB</td><td></td></td<>	PRT2IC1	0B	RW		4B			8B			CB	
PN0001 00 RW 000 RW 440 1 850 1 CD CD FN00C1 0F RW 440 440 87 67 CF CF FN01C1 0F RW 50 A55202CR0 90 RW GDI_LN D0 RW 11 C C 53 A55202CR1 91 RW GDI_LO_LO D3 RW 13 C C 53 A55202CR3 93 RW GDI_LO D3 RW 16 C 55 A55202CR3 93 RW HYSCTRACE D4 RW 16 C 55 A5221CR3 97 RW HYSCTRACE D6 RW 17 C C 56 A5221CR3 97 RW HWSCTRACE D6 RW 18 C S50 A5221CR3 98 MUZ_CR1 D6 RW MUZ_CR1 D6 RW	FN0DM0	0C	RW	CSA3_CR	4C	RW		8C			CC	
FNOC0 0E RW 4F 1 8E 1 CC F FNOC1 0F RW 44F ASD20CR1 90 RW GDL_NN D0 RW 10 11 C 450 ASD20CR3 92 RW GDL_NN D0 RW 12 C C ASD20CR3 93 RW GDL_OU D2 RW 13 C C ASD20CR3 93 RW GDL_OU D2 RW 14 C C ASD20CR3 93 RW HYSCTR2CR D6 RW 15 C ASC21CR3 96 RW HYSCTR2CR D6 RW 16 C ASC21CR3 98 MULCRA D9 RW 170 C ASC ASC21CR3 94 MULCRA D8 RW 16 C ASC ASC21CR3 96 MULCRA D8 RW RW <td< td=""><td>FN0DM1</td><td>0D</td><td>RW</td><td></td><td>4D</td><td></td><td></td><td>8D</td><td></td><td></td><td>CD</td><td></td></td<>	FN0DM1	0D	RW		4D			8D			CD	
FNOC1 OF RW AF AF ABD20CR0 90 RW GOL_O.IN D0 RW 11 12 11 61 ABD20CR2 92 RW GOL_O.IN D0 RW 13 12 12 13 14 RW GOL_O.U D2 RW 14 14 14 14 14 14 RW HYSCTRCRC D5 RW 15 14 15 14 16 ASC10R1 95 RW HYSCTRCRC D5 RW 16 16 ASC10R3 97 RW HYSCTRCR D5 RW 17 18 17 ASC10R3 97 RW HYSCTR2R D7 RW 18 10 16 58 18 98 MUX.CR1 D9 RW 110 10 55 15 05 90 SC SCFA1 D5 RW MUX.CR1 D9 RW </td <td>FN0IC0</td> <td>0E</td> <td>RW</td> <td></td> <td>4E</td> <td></td> <td></td> <td>8E</td> <td></td> <td></td> <td>CE</td> <td></td>	FN0IC0	0E	RW		4E			8E			CE	
101010RWGOL O. N.D0RW111161ASD20CR191RWGOL O. D.D2RW121314141414141414141415160100000000000RW14141414141414161414160100100100RW1515161616161601701801001001001001001617161716618518029010010010010010010018181716016016016090100 </td <td>FN0IC1</td> <td>0F</td> <td>RW</td> <td></td> <td>4F</td> <td></td> <td></td> <td>8F</td> <td></td> <td></td> <td>CF</td> <td></td>	FN0IC1	0F	RW		4F			8F			CF	
11 11<		10			50		ASD20CR0	90	RW	GDI_O_IN	D0	RW
12 13 14 15 15 15 16 17 18 19 100 18 100 18 100 18 100 18 100 18 100 18 100 18 100 18 100 18 100 18 100 18 100 18 100 18 100 18 100 18 100 18 100 <td></td> <td>11</td> <td></td> <td></td> <td>51</td> <td></td> <td>ASD20CR1</td> <td>91</td> <td>RW</td> <td>GDI_E_IN</td> <td>D1</td> <td>RW</td>		11			51		ASD20CR1	91	RW	GDI_E_IN	D1	RW
13		12			52		ASD20CR2	92	RW	GDI_O_OU	D2	RW
14 15 15 15 16 17 16 17 16 17 18 17 18 17 18 17 18 18 19 18 19 18 19 19 19 10 19 10<		13			53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
15 16 16 16 16 16 16 16 16 16 16 16 17 18 17 18 17 18 17 18 17 18 17 18 17 18 17 18 17 18 17 18 17 18 17 19 17 10 17 10<		14			54		ASC21CR0	94	RW	HYSCTLR0CR	D4	RW
16 17 16 17 18 17 18 17 18 17 18 17 18 17 18 17 18 19 18 19 18 19 18 19 100		15			55		ASC21CR1	95	RW	HYSCILRICR	D5	RW
11 1		16			50		ASC21CR2	96	RW	HYSCILR2CR	D6	RW
19 10 20 100 20 100 200 100 200 RW 14 14 14 14 164 164 98 MUX_CR1 09 RW 18 64 64 98 MUX_CR2 0A RW 10 10 50 99 0SC.GO.EN 0D RW 110 10 55 99 90 0SC.CR3 0F RW 111 11 11 11 11 0SC.CR3 0F RW 111 11 11 11 11 0SC.CR3 0F RW 111 11 11 11 11 11 0SC.CR3 0F RW 111 11 11 11 11 11 0SC.CR3 0F RW 111 124 RW CLK.CR1 61 RW A4 VLT_CR E3 RW 111 124 RW <td></td> <td>17</td> <td></td> <td></td> <td>58</td> <td></td> <td>ASUZICKS</td> <td>97</td> <td>RW</td> <td>MUX CPO</td> <td></td> <td>RW RW</td>		17			58		ASUZICKS	97	RW	MUX CPO		RW RW
IA Image: Constraint of the second seco		10			59			90		MUX_CR1	D0 D0	RW
18 68 98 780 781 781 110 10 50 97 98 68 757 00 RW 110 10 50 99 05 C.G.G.E.N 00 RW 116 10 55 97 05C.CR4 DE RW 117 7 55 97 05C.CR4 DE RW DB8000N 21 RW CLK_CR1 61 RW A0 05C.CR3 DF RW DB8001N 21 RW CLK_CR1 61 RW A1 OSC.CR4 DE RW DB8001N 22 RW CLK_CR1 64 RW A3 VLT_CRF E3 RW DB801N 25 RW AMD_CR0 65 RW A6 E5 E6 RW CDCa2RM A8 MO_TR <td></td> <td>13 1A</td> <td></td> <td></td> <td>5A</td> <td></td> <td></td> <td>9A</td> <td></td> <td>MUX_CR2</td> <td>DA</td> <td>RW</td>		13 1A			5A			9A		MUX_CR2	DA	RW
1C IC IC<		1B			5B			9B		MIG/(_OI12	DB	
1D PD SD PD 9D OSC.GO.EN DD RW 1E SE 9F OSC.CR4 DE RW DB00FN 20 RW CLK_CR0 60 RW A0 OSC.CR3 DF RW DB000H 21 RW CLK_CR1 61 RW A1 OSC.CR2 E2 RW DB800H 21 RW AMD_CR0 62 RW A2 OSC.CR2 E2 RW DB801N 23 AMD_CR0 63 RW A3 VLT_CR E3 RW DB801N 25 RW A65 A5 E5 E6 E6 E5 E5 E6 E6 E6 E7 RW A6 E6 E7 RW DC802R A8 IMO_TR E8 RW DC802R A8 IMO_TR E8 RW DC802R A8 IMO_TR E8 RW DC802R A2 RC602R F7 <td></td> <td>10</td> <td></td> <td></td> <td>5C</td> <td></td> <td></td> <td>9C</td> <td></td> <td>SREG TST</td> <td>DC</td> <td>RW</td>		10			5C			9C		SREG TST	DC	RW
IE M 5E M 9E OSC,CR4 DE RW 1F - 5F - 9F OSC,CR3 DF RW DBB00FN 20 RW CLK_CR0 60 RW Ad OSC,CR3 DF RW DBB00DU 22 RW CLK_CR1 61 RW Ad OSC,CR2 E2 RW 23 - AMD_CR0 63 RW Ad3 VLT_CR E3 RW DBB01FN 24 RW CMP_GO_EN 64 RW Ad4 VLT_CR E3 RW DBB01FN 25 RW AMD_CR1 66 RW Ad6 - E6 - - DCC,CR2 E7 RW DCB02FN 28 RW ALT_CR1 68 RW Ad6 IMO_TR E8 RW DCB02FN 28 RW CLC,CR2 69 RW Ad8 IMO_TR E8 RW <td></td> <td>1D</td> <td></td> <td></td> <td>5D</td> <td></td> <td></td> <td>9D</td> <td></td> <td>OSC_GO_EN</td> <td>DD</td> <td>RW</td>		1D			5D			9D		OSC_GO_EN	DD	RW
IF CLK_CR0 65F CRW 9F OSC_CR3 DF RW DBB00IN 20 RW CLK_CR1 61 RW A0 OSC_CR3 E0 RW DBB00IN 21 RW CLK_CR1 61 RW A1 OSC_CR2 E2 RW DBB00IN 22 RW ABF_CR0 62 RW A2 OSC_CR2 E2 RW DBB01N 23 AMD_CR0 63 RW A3 VLT_CR E3 RW DBB01N 25 RW CMP_GO_EN 64 RW A4 VLT_CMP E4 R DBB01N 25 RW AMD_CR1 66 RW A6 CCR2 E5 DBB01N 25 RW AMD_CR1 68 RW A6 MMD_CR1 E8 RW DC002N 28 RW CLK_CR2 69 RW A6 MD_DR E0 RW		1E			5E			9E		OSC_CR4	DE	RW
DBBOOFN 20 RW CLK_CR0 60 RW A0 OSC_CR0 E0 RW DBBOON 21 RW CLK_CR1 61 RW A1 COSC_CR1 E1 RW DBBOON 22 RW ABF_CR0 62 RW A2 OSC_CR2 E2 RW DBBOTN 24 RW CMP_GO_EN 64 RW A3 VLT_CRP E3 RW DBBOTN 25 RW AMD_CR1 66 RW A5 IVT_CRP E6 IVT_CRP E5 IVT_CRP E6 RW DSOC_R2 E7 RW DBBOTN 25 RW AMD_CR1 66 RW A6 IVT_CRP E6 IVT_CRP E8 RW DCBO2N 28 RW ALT_CR1 68 RW A8 IMO_TR E8 RW DCBO2N 24 RW ALT_CR1 68 RW A6 IDO_TR E9		1F			5F			9F		OSC_CR3	DF	RW
DBB00IN 21 RW CLK_CR1 61 RW A1 OSC_CR1 E1 RW DBB00OU 22 RW AABF_CR0 62 RW A2 OSC_CR2 E2 RW 23 AMD_CR0 63 RW A3 VLT_CR E3 RW DBB01N 24 RW CM_GO_EN 64 RW A4 VLT_CR E4 R DBB01N 25 RW AMD_CR1 66 RW A4 VLT_CR E6 DB01N 25 RW AMD_CR1 66 RW A6 DEC_CR2 E7 RW DC802N 28 RW A4 A9 DEC_CR2 E7 RW DC802N 29 RW CLK_CR2 69 RW A9 ILO_TR E9 RW DC802N 20 RW TMP_DR0 6C RW AC E0 ILO_TR E9 RW	DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB000U 22 RW ABC_RO 62 RW A2 OSC_CR2 E2 RW DBB01FN 24 RW CMP_GO_EN 64 RW A3 VLT_CR E3 RW DBB01IN 25 RW CMP_GO_EN 64 RW A4 VLT_CMP E4 R DBB01D0 26 RW AMD_CR1 66 RW A6 C E6 - DBB01D1 26 RW ALT_CR1 66 RW A6 C E6 - RW C A8 IMO_TR E8 RW DCB021N 28 RW CLK_CR2 69 RW AA BDG_TR EA RW DCB021N 29 RW CLK_CR2 69 RW AA BDG_TR EA RW DCB031N 2D RW TMP_DR0 6C RW AC ED ED C DCB031N 2D RW </td <td>DBB00IN</td> <td>21</td> <td>RW</td> <td>CLK_CR1</td> <td>61</td> <td>RW</td> <td></td> <td>A1</td> <td></td> <td>OSC_CR1</td> <td>E1</td> <td>RW</td>	DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
23 AMD_CR0 63 RW A3 VLT_CR E3 RW DB601FN 24 RW CMP_GO_EN 64 RW A4 VLT_CR E3 RW DB8010U 26 RW AMD_CR1 66 RW A5 E5 DB801PN 24 RW AMD_CR1 66 RW A6 E5 DCB02FN 28 RW ALT_CR1 68 RW A7 DEC_CR2 E7 RW DCB02IN 29 RW CLK_CR2 69 RW A8 IMO_TR E8 RW DCB02OU 2A RW CLK_CR2 69 RW AA BDG_TR EA RW DCB03IN 2C RW TMP_DR1 6C RW AA BDG_TR EB DCB03IN 2C RW TMP_DR1 6C RW AE EC ED	DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
DBB01FN 24 RW CMP_GO_EN 64 RW A4 VLT_CMP E4 R DBB011N 25 RW 65 A5 E5 E5 DBB010U 26 RW AMD_CR1 66 RW A6 E6 E5 DCB02FN 28 RW ALT_CR0 67 RW A7 DEC_CR2 E7 RW DCB02IN 29 RW ALT_CR1 68 RW A8 IMO_TR E8 RW DCB02IN 29 RW CLK_CR2 69 RW AA BDG_TR EA RW DCB03IN 2D RW TMP_DR0 6C RW AD ED ED <td></td> <td>23</td> <td></td> <td>AMD_CR0</td> <td>63</td> <td>RW</td> <td></td> <td>A3</td> <td></td> <td>VLT_CR</td> <td>E3</td> <td>RW</td>		23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01IN 25 RW AMD_CR1 65 C A5 C E5 DBB01OU 26 RW AMD_CR1 66 RW A6 E6 E7 RW DCB02FN 28 RW ALT_CR1 68 RW A6 IMO_TR E8 RW DCB02IN 29 RW CLK_CR2 69 RW A8 IMO_TR E8 RW DCB02OU 2A RW CLK_CR2 69 RW A9 ILO_TR E9 RW DCB03IN 2D RW TMP_DR0 6C RW A6 ED E0 E0 <t< td=""><td>DBB01FN</td><td>24</td><td>RW</td><td>CMP_GO_EN</td><td>64</td><td>RW</td><td></td><td>A4</td><td></td><td>VLT_CMP</td><td>E4</td><td>R</td></t<>	DBB01FN	24	RW	CMP_GO_EN	64	RW		A4		VLT_CMP	E4	R
DBB0100 26 RW AMD_CK1 66 RW A6 C C E6 C DCB02FN 28 RW ALT_CR1 66 RW A8 IMO_TR E8 RW DCB02IN 29 RW CLK_CR2 69 RW A9 ILO_TR E9 RW DCB020U 2A RW CLK_CR2 69 RW A9 ILO_TR E9 RW DCB020L 2A RW CLK_CR2 69 RW AA BDG_TR EA RW DCB03N 2C RW TMP_DR0 6C RW AAC EE EC DCB03VD 2E RW TMP_DR1 6D RW AAC EE EC EC DCB03VD 2E RW TMP_DR2 6E RW AC EE EC EE	DBB01IN	25	RW		65	DW		A5			E5	
CCB02FN 28 RW ALT_CR1 68 RW AB IMO_TR E8 RW DCB02VI 29 RW CLK_CR2 69 RW A9 ILO_TR E9 RW DCB02VI 24 RW CLK_CR2 69 RW A9 ILO_TR E9 RW DCB02VI 24 RW CLK_CR2 69 RW AA BDG_TR EA RW DCB03VI 28 TMP_DR0 6C RW AA BDG_TR EA RW DCB03VI 2D RW TMP_DR1 6D RW AD EE ED DCB03VI 2E RW TMP_DR3 6F RW AD EF EF EF DB810FN 30 RW ACB00CR3 70 RW RDI0RI B0 RW F1 EF EF DB810N 31 RW ACB00CR1 72 RW RDI0RI	DBB0100	26	RW	AMD_CR1	60	RW		A6			E0 E7	DW/
DCB02PN 23 RW AL_CN1 06 RW AB IMD_IR EB RW DCB020U 2A RW CLK_CR2 69 RW AB ILO_TR E9 RW DCB020U 2A RW MP_CR2 69 RW AA BDG_TR EA RW 2B Image: CLK_CR2 69 RW AB Image: CLK_CR2 E8 RW E8 RW DCB030N 2D RW TMP_DR1 60 RW AD Image: CLC EC Image: CLC E6 Image: CLC E0 Image: CLC Image: CLC Image: CLC E6 Image: CLC E6 Image: CLC <		27	DW/		69	RW		A7 		DEC_CR2	E7	RW
DCB02IN 25 NN CLCCR 6A NN AA BC_TR EA RW DCB020U 2A RW TMP_DR0 6A AA BC_TR EA RW DCB03FN 2C RW TMP_DR0 6C RW AC EC EC DCB03IN 2D RW TMP_DR1 6D RW AC EC EC DCB03OU 2E RW TMP_DR2 6E RW AE EE EE DCB03OU 2E RW TMP_DR3 6F RW AE EE EE DB810FN 30 RW AC800CR3 70 RW RDIORI B0 RW F1 EF EE DB810N 31 RW AC800CR1 71 RW RDIORI B0 RW F1 EE EE DB810N 32 RW AC800CR1 71 RW RDIOR1 B3 RW F2 </td <td>DCB02FN DCB02IN</td> <td>20</td> <td>RW</td> <td></td> <td>60</td> <td>RW</td> <td></td> <td>Α0 ΔQ</td> <td></td> <td></td> <td>E0 EQ</td> <td>RW</td>	DCB02FN DCB02IN	20	RW		60	RW		Α0 ΔQ			E0 EQ	RW
DBDLOG DK DBDNK DBDNK DBDNK DBDNK DBDNK DK DBDNK DK	DCB020U	23 2A	RW	OLK_OKZ	6A	1.00		A3 AA		BDG TR	E3 FA	RW
DCB03FN 2C RW TMP_DR0 6C RW AC AC EC DCB03IN 2D RW TMP_DR1 6D RW AD ED ED DCB03OU 2E RW TMP_DR2 6E RW AE EE EE 2F TMP_DR3 6F RW AMUX_CLK AF RW EF DB810FN 30 RW ACB00CR3 70 RW RURN B0 RW F0 DB810IN 31 RW ACB00CR1 72 RW RDI0SYN B1 RW F1 DB810OU 32 RW ACB00CR1 72 RW RDI0IS B2 RW F3 DB811FN 34 RW ACB01CR3 74 RW RDI0R00 B5 RW F6 DB8010U 36 RW ACB01CR2 77 RW RDI0R01 B6 RW F6	0000200	2B			6B			AB			EB	
DCB03IN 2D RW TMP_DR1 6D RW AD AD ED ED DCB03OU 2E RW TMP_DR2 6E RW AE EE EE 2F TMP_DR3 6F RW AMUX_CLK AF RW EF EE DB10FN 30 RW ACB00CR3 70 RW RDI0RI B0 RW F0 EF DB10IN 31 RW ACB00CR1 72 RW RDI0SYN B1 RW F1 E DB100U 32 RW ACB00CR1 72 RW RDI0SYN B1 RW F3 E DB100U 32 RW ACB01CR3 74 RW RDI0IT1 B4 RW F4 E DB11FN 34 RW ACB01CR0 75 RW RDI0R00 B5 RW F6 E DB101U 36 RW ACB01CR1 76	DCB03FN	2C	RW	TMP DR0	6C	RW		AC			EC	
DCB03OU 2E RW TMP_DR2 6E RW AE C EE 2F TMP_DR3 6F RW AMUX_CLK AF RW EF DBB10FN 30 RW ACB00CR3 70 RW RDIORI B0 RW F0 DBB10N 31 RW ACB00CR0 71 RW RDIORI B0 RW F1 DBB10DU 32 RW ACB00CR1 72 RW RDIOIS B2 RW F2 33 ACB00CR2 73 RW RDIOITO B3 RW F4 DBB11FN 34 RW ACB01CR3 74 RW RDIOR00 B5 RW F4 DBB010U 36 RW ACB01CR1 76 RW RDIOR01 B6 RW F6 DCB12FN 38 RW 78 RD11R1 B8 RW F8 DCB12DU 3A RW GDRV0_CR <td>DCB03IN</td> <td>2D</td> <td>RW</td> <td>TMP_DR1</td> <td>6D</td> <td>RW</td> <td></td> <td>AD</td> <td></td> <td></td> <td>ED</td> <td></td>	DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
2F TMP_DR3 6F RW AMUX_CLK AF RW EF DBB10FN 30 RW ACB00CR3 70 RW RDIORI B0 RW F0 DBB10IN 31 RW ACB00CR0 71 RW RDIOSYN B1 RW F1 DBB10DU 32 RW ACB00CR1 72 RW RDI0SYN B1 RW F2 33 ACB00CR2 73 RW RDI0LT0 B3 RW F3 DBB11FN 34 RW ACB01CR3 74 RW RDIOLT0 B3 RW F4 DBB01N 35 RW ACB01CR0 75 RW RDIOR00 B5 RW F6 0B8010U 36 RW ACB01CR1 76 RW RDIOR01 B6 RW F6 0CB12FN 38 RW 78 RD11R1 B8 RW F8 0CB12OU 3A RW	DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
DBB10FN 30 RW ACB00CR3 70 RW RDIORI B0 RW Image: fragment of the system of the		2F		TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBB10IN 31 RW ACB00CR0 71 RW RDI0SYN B1 RW F1 F1 DBB10OU 32 RW ACB00CR1 72 RW RDI0IS B2 RW F1 F1 33 ACB00CR2 73 RW RDI0IT0 B3 RW F3 DBB11FN 34 RW ACB01CR3 74 RW RDI0IT1 B4 RW F4 DBB01IN 35 RW ACB01CR0 75 RW RDI0R00 B5 RW F6 DBB01OU 36 RW ACB01CR1 76 RW RDI0R01 B6 RW F6 0BB01OU 36 RW ACB01CR2 77 RW B7 CPU_F F7 RL DBB01OU 36 RW ACB01CR2 77 RW RD1RI B8 RW F8 DCB12FN 38 RW GDRV0_CR 79 RW RD1S	DBB10FN	30	RW	ACB00CR3	70	RW	RDIORI	B0	RW		F0	
DBB100U32RWACB00CR172RWRDI0ISB2RWFWF233ACB00CR273RWRDI0LT0B3RWF3DBB11FN34RWACB01CR374RWRDI0LT1B4RWF4DBB01IN35RWACB01CR075RWRDI0R00B5RWF5DBB01OU36RWACB01CR176RWRDI0R01B6RWF60BB01OU36RWACB01CR277RWRDI0R01B6RWF7RL0DB12FN38RWACB01CR277RWRDI1RIB8RWF80CB12IN39RWGDRV0_CR79RWRDI1SYNB9RWF60DB13FN30RWGDRV1_CR77RWRDI1LT0B8RWF60CB13IN30RWGDRV2_CR70RWRDI1R00BDRWDAC_CRFDRW0CB13OU34RWGDRV2_CR77RWRDI1R00BBRWDAC_CRFDRW0CB13IN30RWGDRV2_CR70RWRDI1R01BERWDAC_CRFDRW0CB13OU34RWGDRV3_CR74RWRDI1R01BERWDAC_CRFDRW0CB13OU35RWGDRV3_CR77RWRDI1R01BERWCPU_SCR01FE#<	DBB10IN	31	RW	ACB00CR0	71	RW	RDIOSYN	B1	RW		F1	
33ACB00CR273RWRDI0LT0B3RWF3DBB11FN34RWACB01CR374RWRDI0LT1B4RWF4DBB011N35RWACB01CR075RWRDI0RO0B5RWF4DBB010U36RWACB01CR176RWRDI0RO1B6RWF6DBB010U36RWACB01CR277RWRDI0RO1B6RWF7RLDCB12FN38RWACB01CR277RWRD11RIB8RWF8DCB12IN39RWGDRV0_CR79RWRD11SNB9RWF6DCB12OU3ARWGDRV1_CR78RWRD11SNB8RWF6DCB13IN3DRWGDRV2_CR70RWRD11R1BCRWF6DCB13OU34RWGDRV1_CR78RWRD11SNB9RWF6DCB13IN3DRWGDRV2_CR70RWRD11R00BDRWDAC_CRFDRWDCB13OU3ERWGDRV2_CR77RWRD11R01BERWDAC_CRFD#DCB13OU3FGDRV3_CR7FRWRD11R01BERWDAC_CRFD#DCB13OU3FRWGDRV3_CR7FRWRD11R01BERWCPU_SCR01FE#DCB13OU3F	DBB10OU	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBB11FN 34 RW ACB01CR3 74 RW RDI0LT1 B4 RW RCM F4 DBB011N 35 RW ACB01CR0 75 RW RDI0RO0 B5 RW F6 DBB010U 36 RW ACB01CR1 76 RW RDI0RO1 B6 RW F6 0BB010U 36 RW ACB01CR1 76 RW RDI0RO1 B6 RW CPU_F F6 0CB12FN 38 RW ACB01CR2 77 RW B87 CPU_F F7 RL DCB12FN 38 RW GDRV0_CR 79 RW RDI1SYN B9 RW F6 DCB12IN 39 RW GDRV1_CR 78 RDI1SYN B9 RW F6 DCB130U 3A RW GDRV1_CR 78 RW RDI1LT0 B8 RW F6 DCB131N		33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB011N 35 RW ACB01CR0 75 RW RDI0R00 B5 RW CPU F5 DBB010U 36 RW ACB01CR1 76 RW RDI0R01 B6 RW F6 37 ACB01CR2 77 RW B7 CPU_F F7 RL DCB12FN 38 RW ACB01CR2 77 RW B8 RW CPU_F F7 RL DCB12FN 38 RW GDRV0_CR 79 RW RDI1RI B8 RW F9 DCB12IN 39 RW GDRV0_CR 79 RW RDI1SN B9 RW F6 DCB12OU 3A RW GDRV1_CR 78 RW RDI1SN B4 RW F6 DCB13OU 3A RW GDRV1_CR 78 RW RDI1LT0 B8 RW F6 DCB13FN 3C RW <td< td=""><td>DBB11FN</td><td>34</td><td>RW</td><td>ACB01CR3</td><td>74</td><td>RW</td><td>RDI0LT1</td><td>B4</td><td>RW</td><td></td><td>F4</td><td></td></td<>	DBB11FN	34	RW	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBD1100 30 RW ACB01CR1 70 RW RD10R01 B6 RW CPU_F F6 37 ACB01CR2 77 RW B7 CPU_F F7 RL DCB12FN 38 RW 78 RU RD11RI B8 RW F8 DCB12IN 39 RW GDRV0_CR 79 RW RD11RI B8 RW F8 DCB12IN 39 RW GDRV0_CR 79 RW RD11SI B4 RW F9 DCB12OU 3A RW GDRV1_CR 78 RW RD11SI B4 RW F6 DCB13OU 3A RW GDRV1_CR 78 RW RD11LT0 B8 RW F6 DCB13FN 3C RW GDRV2_CR 70 RW RD11R00 BD RW DAC_CR FD RW DCB130U 3E RW <t< td=""><td>DBB010U</td><td>35</td><td>RW</td><td>ACB01CR0</td><td>/5</td><td>RW</td><td>RDI0RO0</td><td>B5</td><td>RW</td><td></td><td>+5</td><td></td></t<>	DBB010U	35	RW	ACB01CR0	/5	RW	RDI0RO0	B5	RW		+5	
S7 RCB010R2 77 RW B7 CP0_F F7 RL DCB12FN 38 RW 78 RDI1RI B8 RW F8 DCB12IN 39 RW GDRV0_CR 79 RW RDI1SN B9 RW F8 DCB12IN 39 RW GDRV0_CR 79 RW RDI1SN B9 RW F9 DCB12OU 3A RW GDRV1_CR 78 RU RDI1SN B4 RW F8 DCB12OU 3A RW GDRV1_CR 78 RW RDI1LT0 B8 RW F6 DCB13FN 3C RW GDRV2_CR 70 RW RDI1LT1 BC RW DAC_CR FD RW DCB13IN 3D RW GDRV2_CR 70 RW RDI1R00 BD RW DAC_CR FD RW DCB13OU 3E RW <	0660100	30 27	KW		/b 77	RW DW/	KUIUKU'I	80 07	KW		F0 E7	DI
DCB12IN 39 RW GDRV0_CR 79 RW RDI1SYN B9 RW F6 DCB120N 3A RW 79 RW RDI1SYN B9 RW F9 DCB120V 3A RW 7A RDI1SYN B9 RW F6 3B GDRV1_CR 7B RW RDI1LT0 BB RW F6 DCB13FN 3C RW 7C RDI1LT1 BC RW F6 DCB13IN 3D RW GDRV2_CR 7D RW RDI1R00 BD RW DAC_CR FD RW DCB13OU 3E RW GDRV3_CR 7F RW BF CPU_SCR0 FF #	DCB12EN	30	R\//	ACOULCRZ	79	L M M	RDI1PI	B8	B/\/		F1 F2	κL
DCB120U 3A RW 7A RDI1IS BA RW FA 3B GDRV1_CR 7B RW RDI1IS BA RW FA DCB13FN 3C RW 7C RDI1LT1 BC RW FC DCB13IN 3D RW GDRV2_CR 7D RW RDI1R00 BD RW DAC_CR FD RW DCB13OU 3E RW GDRV3_CR 7F RW BF CPU_SCR0 FF #	DCB12FN DCB12IN	30	RW	GDRV/0 CR	70	RW	RDI1SVN	R9	RW		FQ	
3B GDRV1_CR 7B RW RDI1LT0 BB RW FB DCB13FN 3C RW GDRV2_CR 7C RDI1LT1 BC RW FC DCB13IN 3D RW GDRV2_CR 7D RW RDI1R00 BD RW DAC_CR FD RW DCB13OU 3E RW GDRV2_CR 7F RW RD1R01 BE RW CPU_SCR1 FE # 3F GDRV3_CR 7F RW BF CPU_SCR0 FF #	DCB120U	34	RW/		74	1.17	RDI1IS	BA	RW/		FA	
DCB13FN 3C RW GDRV2_CR 7C RD11L11 BC RW FC DCB13IN 3D RW GDRV2_CR 7D RW RD11R00 BD RW DAC_CR FD RW DCB13OU 3E RW 7E RD11R01 BE RW CPU_SCR1 FE # 3F GDRV3_CR 7F RW BF CPU_SCR0 FF #	2001200	3B		GDRV1 CR	7B	RW	RDI1LT0	BB	RW		FB	
DCB13IN 3D RW GDRV2_CR 7D RW RDI1R00 BD RW DAC_CR FD RW DCB13OU 3E RW TC 7E RDI1R01 BE RW CPU_SCR1 FE # 3F GDRV3_CR 7F RW BF CPU_SCR0 FF #	DCB13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCB13OU 3E RW 7E RDI1RO1 BE RW CPU_SCR1 FE # 3F GDRV3_CR 7F RW BF CPU_SCR0 FF #	DCB13IN	3D	RW	GDRV2 CR	7D	RW	RDI1RO0	BD	RW	DAC CR	FD	RW
3F GDRV3_CR 7F RW BF CPU_SCR0 FF #	DCB13OU	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
		3F		GDRV3_CR	7F	RW		BF		CPU_SCR0	FF	#



14. Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CLED04D0X, CY8CLED04G01, CY8CLED03D0X, CY8CLED03G01, CY8CLED02D01, and CY8CLED01D01 of the PowerPSoC device family. For the most up to date electrical specifications, confirm that you have the most recent datasheet by going to the web at http://www.cypress.com/powerpsoc. Specifications for Industrial rated devices are valid for -40 °C $\leq T_A \leq 85$ °C, $T_J \leq 115$ °C and for Extended Temperature rated devices for -40 °C $\leq T_A \leq 105$ °C, $T_J \leq 125$ °C, except where noted.

14.1 Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. Not all user guidelines are production tested.

Table 14-1. Absolute Maximum Ratings

Symbol	Description	Min	Тур	Max	Units	Notes
T _{STG}	Storage temperature	-55	-	+115	°C	Higher storage temperatures reduces data retention time. Recommended storage temperature is 0 °C to 50 °C.
T _A	Ambient temperature with power applied	-40 -40	-	+85 +105	çç	$T_J \le 115$ °C (industrial rated) $T_J \le 125$ °C (extended temperature rated)
V _{DD} , AV _{DD} , GDV _{DD}	Supply voltage on $V_{DD},AV_{DD},andGDV_{DD}$	-0.5	-	+6.0	V	Relative to V_{SS} , AV_{SS} , and GDV_{SS} respectively
V _{IO}	DC input voltage	V _{SS} – 0.5	-	V _{DD} + 0.5	V	Applies only to GPIO and FN0 pins
V _{IO2}	DC voltage applied to tristate	$V_{SS} - 0.5$	_	V _{DD} + 0.5	V	
V _{FET}	Maximum voltage from power Switch (SWx) to Power FET Ground (PGNDx)	-	_	36 ^[13]	V	PGNDx is connected to GDV _{SS}
V _{REGIN}	Maximum voltage on SREGHVIN Pin relative to V _{SS}	-	-	36 ^[13]	V	
V _{CSP,} V _{CSN}	Maximum voltage applied to CSA pins relative to V_{SS}	-0.5	-	36 ^[13]	V	
V _{SENSE}	Maximum input differential voltage across CSA input	-1.0	-	1.0	V	
I _{MAIO}	Maximum current into any port pin configured as analog driver	-50	-	+50	mA	
I _{MIO}	Maximum current into any port and function pin	-25	-	+50	mA	
LU	Latch up current	200	_	-	mA	JESD78A Conformal
ESD	Electrostatic discharge voltage	2000	_	_	V	Human Body Model ESD.
SR _{REGIN}	Ramp rate for the SREGHVIN pin	-	-	32	V/µs	
SR _{CSP}	Ramp rate for the CSPx pins	-	-	3.2	V/µs	
SR _H V _{DD-FLB}	High voltage supply ramp rate for floating load buck configuration	_	_	15	V/ms	For other topologies, to enable operation with faster ramp rates, or if the LED string voltage is < 6.5 V, see the <i>PowerPSoC</i> <i>Technical Reference Manual</i> .
SRV _{DD-EXT}	External V_{DD} supply ramp rate (V_{DD} , AV_{DD} , and GDV_{DD} pins)	-	_	0.2	V/µs	Applies only when powered by a source other than the Built-in Switching Regulator

Note

^{13.} Stresses beyond the "Absolute Maximum Ratings" on page 30 may cause permanent damage to the device. You must ensure that the absolute maximum ratings are NEVER exceeded. Functional operation is not implied under any conditions beyond the "Electrical Characteristics" on page 31 onwards. Extended exposure to "Absolute Maximum Ratings" on page 30 may affect reliability of the device.



15.9 Power Peripheral Reference DAC Specification

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-16.	Reference	DAC DC	Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
I _{SDAC}	Supply current - reference DAC	-	-	600	μA	Mode 0 and Mode1
INL	Integral non linearity	-1 -1.5	_ _	1 1.5	LSB LSB	Mode 0 Mode 1
DNL	Differential non linearity	-0.5	-	0.5	LSB	Mode 0 and Mode1
A _{ERROR}	Gain error	-5 -7	_	5 7	LSB LSB	Mode 0 Mode 1
OS _{ERROR}	Offset error	-	_	1	LSB	Mode 0 and Mode1
V _{DACFS}	Fullscale voltage - reference DAC	-	_	2.6 1.3	LSB LSB	Mode 0 Mode 1
V _{DACMM}	Fullscale voltage mismatch (pair of reference DACs - even and odd)	 	 	9 14 10.5 15.5	LSB LSB LSB LSB	Mode 0 (DAC0 through DAC7) Mode 1 (DAC0 through DAC7) Mode 0 (DAC8 through DAC13) Mode 1 (DAC8 through DAC13)

Table 15-17. Reference DAC AC Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
t _{SETTLE}	Output settling time to 0.5 LSB of final value	-	-	10	μS	Mode 0 and Mode1
t _{STARTUP}	Startup time to within 0.5 LSB of final value	-	-	10.5	μS	Mode 0 and Mode1

15.10 Power Peripheral Built-in Switching Regulator

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-18.	Built-in	Switching	Regulator	DC	Specifications
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Symbol	Description	Min	Тур	Max	Units	Notes
V _{REGIN}	Input supply voltage range	7 8		32 32	V V	Industrial rated Extended temperature rated See Absolute Maximum Ratings on page 30
V _{REGOUT}	Output voltage range	4.8	5.0	5.2	V	Does not include V _{RIPPLE}
V _{RIPPLE}	Output ripple	-	-	100	mV	
V _{UVLO}	Under voltage lockout voltage	5.5	-	6.5	V	V _{REGIN} < V _{UVLO} : Power down mode V _{REGIN} > V _{UVLO} : Active mode
I _{LOAD}	DC output current -active mode	0.01	-	250	mA	_
I _{S,BSR}	Supply current - built-in switching regulator	-	-	4	mA	_
I _{SB,HV}	Standby current (high voltage)	-	-	250	μΑ	_
I _{INRUSH}	Inrush current	-	-	1.2	A	V _{REGIN} = 32 V, SR _{REGIN} = 32 V/ms (Industrial rated)
		-	-	1.5	A	V _{REGIN} = 32 V, SR _{REGIN} = 32 V/ms (Extended Temperature rated)
R _{DS(ON),PFET}	PFET drain to source ON resistance	_	2.5	_	Ω	
Line _{REG}	Line regulation	-	1	-	mV	I_{LOAD} = 250 mA, V_{REGIN} = 7 V to 32 V



Table 15-18. Built-in Switching Regulator DC Specifications (continued)

Symbol	Description	Min	Тур	Max	Units	Notes
Load _{REG}	Load regulation	_	1	-	mV	V_{REGIN} = 24 V, I _{LOAD} = 2.5 mA to 250 mA
PSRR	Power supply rejection ratio	_	-60	-	dB	V _{RIPPLE} = 0.2 * V _{REGIN,} f _{RIPPLE} = 1 kHz to 10 kHz
E _{BSR}	Built-in switching regulator efficiency	80	-	-	%	$V_{REGIN} = 24 \text{ V}, I_{LOAD} = 250 \text{ mA}$

Table 15-19. Built-in Switching Regulator AC Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
f _{SW}	Switching frequency	0.956	1	1.04	MHz	-
t _{RESP}	Response time to within 0.5% of final value	-	10	-	μS	-
t _{SU}	Startup time	-	-	1	ms	-
t _{PD}	Power down time	-	-	100	μS	-
t _{PD_ACT}	Time from power down to active mode	-	-	1	ms	-
t _{ACT_PD}	Time from active mode to power down mode	-	-	50	μS	-
SR _{REGIN}	Ramp rate for the SREGHVIN pin	_	_	32	V/µs	See Absolute Maximum Ratings on page 30

Table 15-20. Built-in Switching Regulator Recommended Components

Component Name	Value	Unit	Notes			
R _{fb1}	2	kΩ	Tolerance 1% and 0.05-W rated or better			
R _{fb2}	0.698	kΩ	Tolerance 1% and 0.05-W rated or better			
C _{comp}	2200	pF	Tolerance 20% and 6.3-V rated or better			
R _{comp}	20	kΩ	Tolerance 5% and 0.05-W rated or better			
L	47	μH	Tolerance 20% or better, Saturation current rating of 1.5 A or higher			
R _{sense}	0.5	Ω	Tolerance 1% and 0.05 W (I_{LOAD} = 0.250 A) rated or better			
C ₁	10	μF	Ceramic, X7R grade, Minimum ESR of 0.1 Ω , 6.3-V rated			
C _{in}	1	μF	Ceramic, X7R grade, 50-V rated (V _{REGIN} = 32 V)			
D1	40/0.5	V/A	Schottky diode - Reverse voltage 40 V, average rectified forward current 0.5 A ($V_{REGIN} = 32 V$)			

Note If the built-in switching regulator is not being used in a design, it must be configured as per the following instructions to ensure it is disabled in a safe state.

SREGFB: 5 V

SREGCSN: 5 V

SREGCSP: 5 V

SREGCOMP: Floating

SREGHVIN: \geq VDD rail

SREGSW: Floating/Tie to SREGHVIN

If the switching regulator is disabled through wiring its input pins (as previously explained) then it must be disabled through software as well (bit SREG_TST[0] = 1), which is set in the Global Resources in the Interconnect View of PSoC Designer.



15.12 PSoC Core Operational Amplifier Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Capacitor PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block.

Table 13-23. Operational Ampliner Do operincation	Table 15-23.	Operational	Amplifier DC	Specifications
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Symbol	Description	Min	Тур	Max	Units	Notes
V _{OSOA}	Input offset voltage (absolute value) Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	- - - -	1.6 1.6 1.3 1.3 1.2 1.2	10 15 8 13 7.5 12	mV mV mV mV mV	Industrial rated Extended temperature rated Industrial rated Extended temperature rated Industrial rated Extended temperature rated
TCVoson	Average input offset voltage drift	_	7.0	35.0	uV / °C	
	Input leakage current (Port 0 analog pins)	_	20	-	pA	Gross tested to 1 µA.
CINOA	Input capacitance (Port 0 analog pins)	_	4.5	9.5	pF	T _{.1} = 25 °C.
V _{CMOA}	Common mode voltage range Common mode voltage range (high power or high opamp bias)	0.0 0.5	-	V _{DD} V _{DD} – 0.5	V V	The common-mode input voltage range is measured through an analog output buffer. The specifi- cation includes the limitations imposed by the characteristics of the analog output buffer.
G _{OLOA}	Open loop gain Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	60 60 80			dB dB dB	_
V _{ohighoa}	High output voltage swing (internal signals) Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	V _{DD} – 0.2 V _{DD} – 0.2 V _{DD} – 0.5		- - -	> > >	_
V _{OLOWOA}	Low output voltage swing (internal signals) Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	- - -		0.2 0.2 0.5	V V V	-
I _{SOA}	Supply current (including associated analog output buffer) Power = low, opamp bias = low Power = low, opamp bias = high Power = medium, opamp bias = low Power = medium, opamp bias = high Power = high, opamp bias = low Power = high, opamp bias = high	- - - - - -	400 500 800 1200 2400 4600	800 900 1000 1600 3200 6400	μΑ μΑ μΑ μΑ μΑ μΑ	-
FSKKOA	Supply voltage rejection ratio	52	80	_	aв	$V_{SS} \le V_{IN} \le (V_{DD} - 2.25) \text{ of } (V_{DD} - 1.25 \text{ V}) \le V_{IN} \le V_{DD}.$



Table 15-28. Analog Output Buffer AC Specifications (continued)

Symbol	Description	Min	Тур	Max	Units	Notes
SR _{ROB}	Rising slew rate (20% to 80%), 1 V step, 100 pF load					_
	Power = low	0.65	_	_	V/μs	
	Power = high	0.65	-	—	V/µs	
SR _{FOB}	Falling slew rate (80% to 20%), 1 V step, 100 pF load					-
	Power = low	0.65	—	—	V/µs	
	Power = high	0.65	-	_	V/µs	
BW _{OBSS}	Small signal bandwidth, 20 mV _{pp} , 3 dB BW, 100 pF load					_
	Power = low	0.8	_	_	MHz	
	Power = high	0.8	-	_	MHz	
BW _{OBLS}	Large signal bandwidth, 1 V _{pp} , 3 dB BW, 100 pF load					_
	Power = low	300	-	-	kHz	
	Power = high	300	-	—	kHz	



15.15 PSoC Core Analog Reference

Table 15.20 Analog Peteronee DC Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for extended temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the analog continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Table 15-29. Analog Reference DC Specifications					
Symbol	Description	Min	Тур		

Symbol	Description	Min	Тур	Max	Units	Notes
BG	Bandgap voltage reference	1.28 1.27	1.30 1.30	1.32 1.33	V V	Industrial rated Extended Temperature rated
_	$AGND = V_{DD}/2^{[16]}$	V _{DD} /2 - 0.04 V _{DD} /2 - 0.02	V _{DD} /2 – 0.01 V _{DD} /2	V _{DD} /2 + 0.007 V _{DD} /2 + 0.02	V V	Industrial rated Extended Temperature rated
-	AGND = 2 x BandGap ^[16]	2 x BG – 0.048	2 x BG - 0.030	2 x BG + 0.024	V	
-	AGND = BandGap ^[16]	BG – 0.009	BG + 0.008	BG + 0.016	V	
-	AGND = 1.6 x BandGap ^[16]	1.6 x BG - 0.022	1.6 x BG - 0.010	1.6 x BG + 0.018	V	
_	AGND Block to Block Variation (AGND = $V_{DD}/2$) ^[16]	-0.034	0.000	0.034	V	
_	RefHi = V _{DD} /2 + BandGap	V _{DD} /2 + BG - 0.10	V _{DD} /2 + BG	V _{DD} /2 + BG + 0.10	V	
-	RefHi = 3 x BandGap	3 x BG – 0.06	3 x BG	3 x BG + 0.06	V	
-	RefHi = 3.2 x BandGap	3.2 x BG - 0.112	3.2 x BG	3.2 x BG + 0.076	V	
-	RefLo = V _{DD} /2 – BandGap	V _{DD} /2 – BG – 0.04 V _{DD} /2 – BG – 0.06	V _{DD} /2 – BG + 0.024 V _{DD} /2 – BG	V _{DD} /2 – BG + 0.04 V _{DD} /2 – BG + 0.06	V V	Industrial rated Extended Temperature rated
-	RefLo = BandGap	BG – 0.06	BG	BG + 0.06	V	

15.16 PSoC Core Analog Block

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-30. Analog Block DC Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
R _{CT}	Resistor unit value (continuous time)	_	12.2		kΩ	
C _{SC}	Capacitor unit value (switched capacitor)	_	80	_	fF	

Notes 16. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is $1.3 \text{ V} \pm 0.02 \text{ V}$.



15.17 PSoC Core POR and LVD

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the *PowerPSoC Technical Reference Manual* for more information on the VLT_CR register.

Table 15-31. POR and LVD DC Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
V _{PPOR2}	V _{DD} Value for PPOR Trip PORLEV[1:0] = 10b	_	4.55	4.70	V	_
V _{LVD6} V _{LVD7}	V _{DD} Value for LVD Trip VM[2:0] = 110b VM[2:0] = 111b	4.62 4.71	4.73 4.81	4.83 4.95	V V	_

15.18 PSoC Core Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Symbol	Description	Min	Тур	Max	Units	Notes
I _{DDP}	Supply current during programming or verify	-	15	30	mA	-
V _{ILP}	Input low voltage during programming or verify	-	-	0.8	V	-
V _{IHP}	Input high voltage during programming or verify	2.1	-	-	V	-
I _{ILP}	Input current when applying V _{ILP} to P1[0] or P1[1] during programming or verify	-	-	0.2	mA	Driving internal pull down resistor.
I _{IHP}	Input current when applying V _{IHP} to P1[0] or P1[1] during programming or verify	-	-	1.5	mA	Driving internal pull down resistor.
V _{OLV}	Output low voltage during programming or verify	-	-	V _{SS} + 0.75	V	-
V _{OHV}	Output high voltage during programming or verify	V _{DD} – 1.0	-	V _{DD}	V	-
Flash _{ENPB}	Flash endurance (per block)	50,000	-	-	-	Erase/write cycles per block.
Flash _{ENT}	Flash endurance (total) ^[17]	1,800,000	-	-	-	Erase/write cycles.
Flash _{DR}	Flash data retention ^[18]	10	_	-	Years	_

Table 15-32. Programming DC Specifications

Notes

^{17.} A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36 x 1 blocks of 50,000 maximum cycles each, 36 x 2 blocks of 25,000 maximum cycles each, or 36 x 4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36 x 50,000 and that no single block ever sees more than 50,000 cycles)

^{18.} Guaranteed for -40 °C \leq T_A \leq 85 °C for Industrial rated devices and -40 °C \leq T_A \leq 105 °C for Extended Temperature rated devices.



15.20 PSoC Core I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-35. AC Chara	cteristics of the I ² C	SDA and SCL Pins
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Symbol	Description	Standa	d Mode	e Fast Mo	Fast Mode		Unito	Notos
Symbol	Description	Min	Max	Min	Max	Units	NOLES	
f _{SCLI2C}	SCL clock frequency	0	100	0	400	kHz	-	
t _{HDSTAI2C}	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	Ι	0.6	Ι	μs	_	
t _{LOWI2C}	LOW period of the SCL clock	4.7	Ι	1.3	-	μS	-	
t _{HIGHI2C}	HIGH period of the SCL clock	4.0	Ι	0.6	Ι	μS	-	
t _{SUSTAI2C}	Setup time for a repeated START condition	4.7	Ι	0.6	Ι	μS	-	
t _{HDDATI2C}	Data hold time	0	Ι	0	Ι	μS	_	
t _{SUDATI2C}	Data setup time	250	Ι	100 ^[21]	Ι	ns	-	
t _{SUSTOI2C}	Setup time for STOP condition	4.0	-	0.6	-	μS	-	
t _{BUFI2C}	Bus free time between a STOP and START condition	4.7	-	1.3	-	μs	_	
t _{SPI2C}	Pulse width of spikes are suppressed by the input filter.	_	-	0	50	ns	_	

Figure 15-8. Definition of Timing for Fast/Standard Mode on the I²C Bus



Note

^{21.} A fast mode I²C bus device can be used in a standard mode I²C bus system, but the requirement t_{SUDATI2} ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line trmax + t_{SUDATI2} = 1000 + 250 = 1250 ns (according to the standard mode I²C bus specification) before the SCL line is released.



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