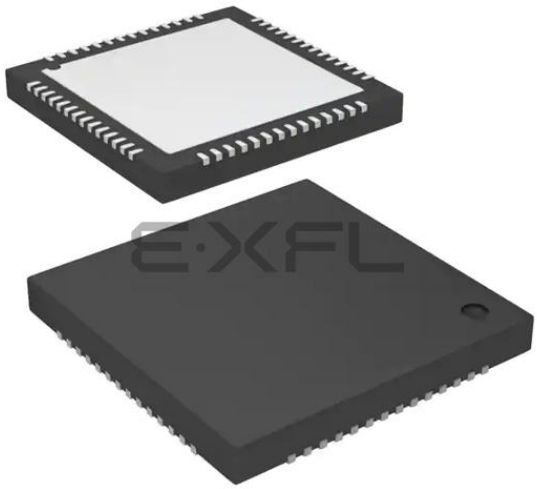
Infineon Technologies - CY8CLED01D01-56LTXQT Datasheet



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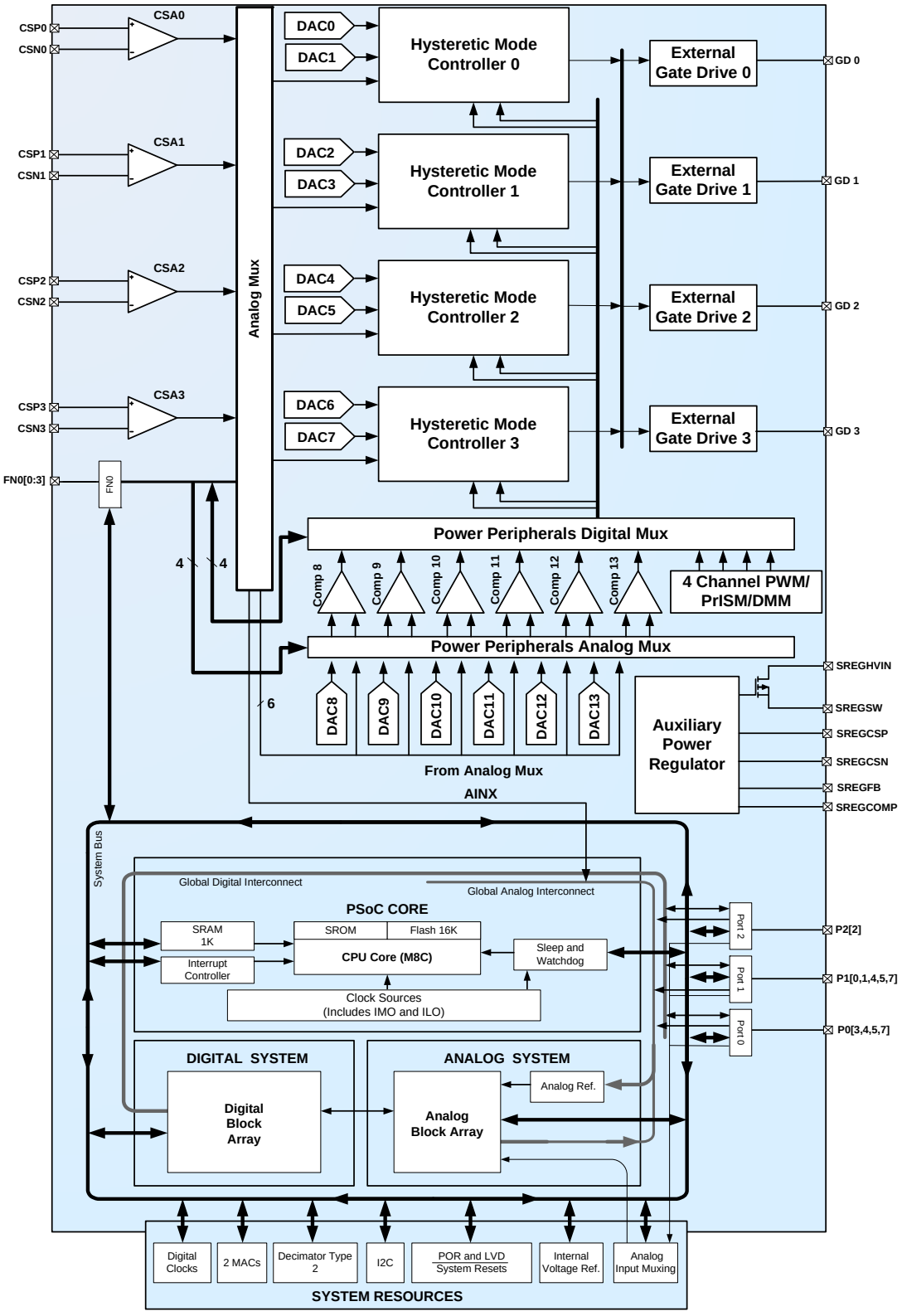
What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Discontinued at Digi-Key
Applications	Intelligent LED Driver
Core Processor	M8C
Program Memory Type	FLASH (16KB)
Controller Series	CY8CLED
RAM Size	1K x 8
Interface	DALI, DMX512, I²C, IrDA, SPI, UART/USART
Number of I/O	-
Voltage - Supply	4.75V ~ 5.25V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad
Supplier Device Package	56-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8cled01d01-56ltxqt

2. Contents

Figure 3-2. CY8CLED04G01 Logic Block Diagram



4. PowerPSoC® Functional Overview

The PowerPSoC family incorporates programmable system-on-chip technology with the best in class power electronics controllers and switching devices to create easy to use power-system-on-chip solutions for lighting applications.

All PowerPSoC family devices are designed to replace traditional MCUs, system ICs, and the numerous discrete components that surround them. PowerPSoC devices feature high performance power electronics including 1 ampere 2 MHz power FETs, hysteretic controllers, current sense amplifiers, and PrISM/PWM modulators to create a complete power electronics solution for LED power management. Configurable power, analog, digital, and interconnect circuitry enables a high level of integration in a host of industrial, commercial, and consumer LED lighting applications.

This architecture integrates programmable analog and digital blocks to enable you to create customized peripheral configurations that match the requirements of each individual application. Additionally, the device includes a 24 MHz CPU, Flash program memory, SRAM data memory, and configurable I/O in a range of convenient pinouts and packages.

The PowerPSoC architecture, as illustrated in the block diagrams, consists of five main areas: PSoC core, digital system, analog system, system resources, and power peripherals, which include power FETs, hysteretic controllers, current sense amplifiers, and PrISM/PWM modulators. Configurable global busing combines all of the device resources into a complete custom system. The PowerPSoC family of devices have 10-port I/Os that connect to the global digital and analog interconnects, providing access to eight digital blocks and six analog blocks.

5. Power Peripherals

PowerPSoC is designed to operate at voltages from 7 V to 32 V, drive up to 1 ampere of current using internal MOSFET switches, and over 1 ampere with external MOSFETs.

This family of devices (CY8CLED0xD/G0y) combines up to four independent channels of constant current drivers. These drivers feature hysteretic controllers with the Programmable System-on-Chip (PSoC) that contains an 8-bit microcontroller, configurable digital and analog peripherals, and embedded flash memory.

The CY8CLED0xD/G0y is the first product in the PowerPSoC family to integrate power peripherals to add further integration for your power electronics applications.The PowerPSoC family of intelligent power controller ICs are used in lighting applications that need traditional MCUs and discrete power electronics support. The power peripherals of the CY8CLED0xD/G0y include up to four 32 volt power MOSFETs with current ratings up to 1 ampere each. It also integrates gate drivers that enable applications to drive external MOSFETs for higher current and voltage capabilities. The controller is a programmable threshold hysteretic controller, with user-selectable feedback paths that uses the IC in current mode floating load buck, floating load buck-boost, and boost configurations.

5.1 Hysteretic Controllers

The PowerPSoC contains four hysteretic controllers. There is one hysteretic controller for each channel of the device.

The hysteretic controllers provide cycle by cycle switch control with fast transient response, which simplifies system design by requiring no external compensation. The hysteretic controllers include the following key features:

- Four independent channels
- DAC configurable thresholds
- Wide switching frequency range from 20 kHz to 2 MHz
- Programmable minimum on and off time
- Floating load buck, floating load buck-boost and boost topology controller

The reference inputs (REF_A and REF_B in Figure 5-1.) of the hysteretic controller are provided by the reference DACs as illustrated in the top level block diagram (see Figure 3-1. on page 3).

The hysteretic control function output is generated by comparing the feedback value to two thresholds. Going below the lower threshold turns the switch ON and exceeding the upper threshold turns the switch OFF as shown in Figure 5-1. The output current waveforms are shown in Figure 5-2.

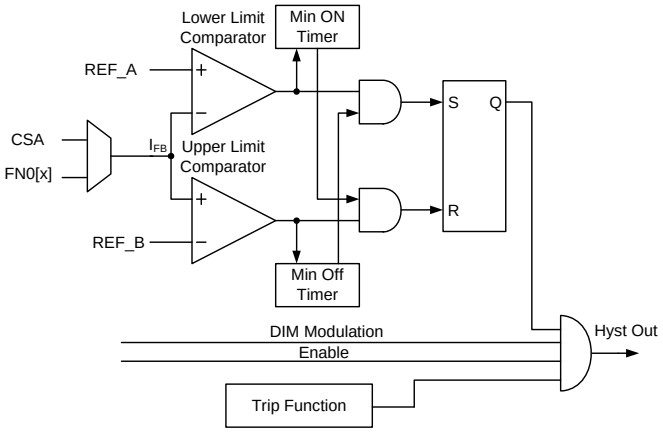
The hysteretic controller also controls the minimum on-time and off-time. This circuit prevents oscillation at very high frequencies; which can be very destructive to output switches.

The output to the gate drivers is gated by the Trip, DIM and Enable signals. The Enable signal is a direct result of the enable bit in the control register for the hysteretic controller.

The Trip signal can be any digital signal that follows TTL logic (logic high and logic low). It is an active high input.

The DIM Modulation signal is the output of the dedicated modulators that are present in the power peripherals, or any other digital modulation signal.

Figure 5-1. Generating Hysteretic Control Function Output



6. PSoC Core

The PSoC core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable general purpose I/O(GPIO).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with up to 20 vectors to simplify programming of real time embedded events. The program execution is timed and protected using the included sleep and watchdog timers (WDT) time and protect program execution.

Memory encompasses 16 K of flash for program storage, 1 K of SRAM for data storage, and up to 2 K of EEPROM emulated using the flash. Program flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

The PSoC device incorporates flexible internal clock generators, including a 24 MHz internal main oscillator (IMO) accurate to 4 percent over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz internal low-speed oscillator (ILO) is provided for the sleep timer and WDT. The clocks, together with programmable clock dividers (as a system resource), provide the flexibility to integrate almost any timing requirement into the PowerPSoC device.

PowerPSoC GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

6.1 Digital System

The digital system contains eight digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

Digital peripheral configurations include:

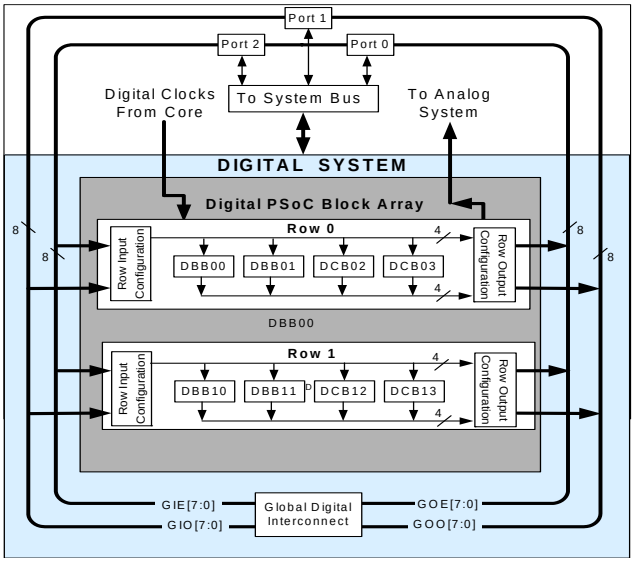
- DMX512
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8-bit with selectable parity
- SPI master and slave
- I^2C master, slave, and multi-master
- Cyclical redundancy checker/generator (8 to 32 bit)
- IrDA
- Pseudo random sequence generators (8 to 32 bit)

Note The DALI interface is supported through the use of a combination of the above mentioned user modules. For more details on the exact configuration and an example project, refer to the application note, PowerPSoC Firmware Design Guidelines, Lighting Control Interfaces - AN51012.

The digital blocks can be connected to any GPIO through a series of global buses that route any signal to any pin. The buses also allow signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

There are four digital blocks in each row. This allows optimum choice of system resources for your application.

Figure 6-1. Digital System Block Diagram



6.2 Analog System

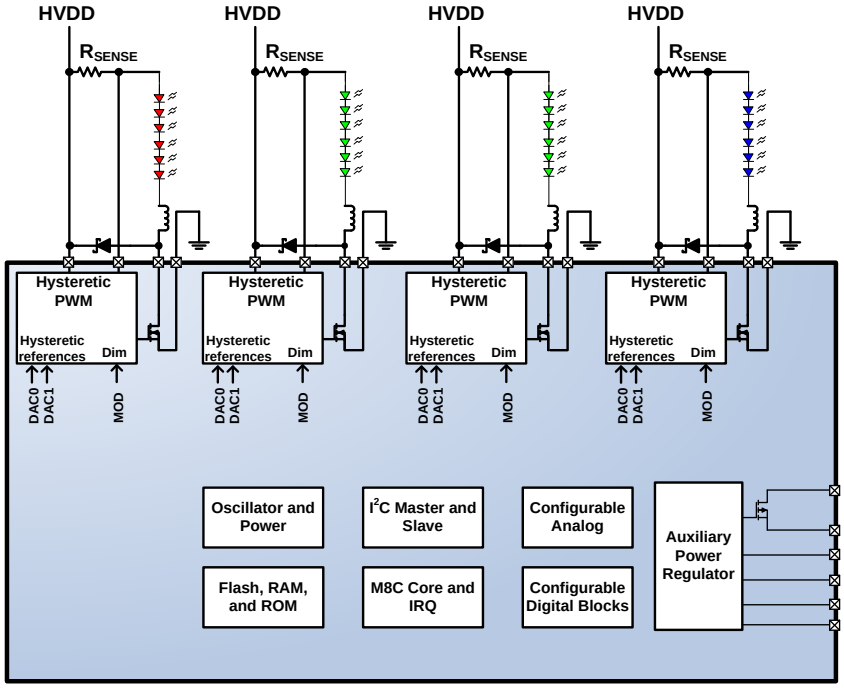
The analog system contains six configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PowerPSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (up to 2, with 6 to 12-bit resolution, selectable as incremental, Delta Sigma, and SAR)
- Filters (2 and 4 pole band-pass, low-pass, and notch)
- Amplifiers (up to 2, with selectable gain to 48x)
- Instrumentation amplifiers (1 with selectable gain to 93x)
- Comparators (up to 2, with 16 selectable thresholds)
- DACs (up to 2, with 6 to 9-bit resolution)
- Multiplying DACs (up to 2, with 6 to 9-bit resolution)
- High current output drivers (two with 30 mA drive as a PSoC core resource)
- 1.3 V reference (as a system resource)
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

7. Applications

The PowerPSoC family of devices can be used to add hysteretic current control capability to power applications. The devices can be used to control current in devices such as LEDs, heating elements, and solenoids. For LED applications, all high-brightness LEDs (HBLEDs) can be controlled using the PowerPSoC. The following figures show examples of applications in which the PowerPSoC family of devices adds intelligent power control for power applications.

Figure 7-1. LED Lighting with RGGB Color Mixing Configured as Floating Load Buck Converter



12. Pin Information

12.1 CY8CLED04D0x 56-Pin Part Pinout (without OCD)

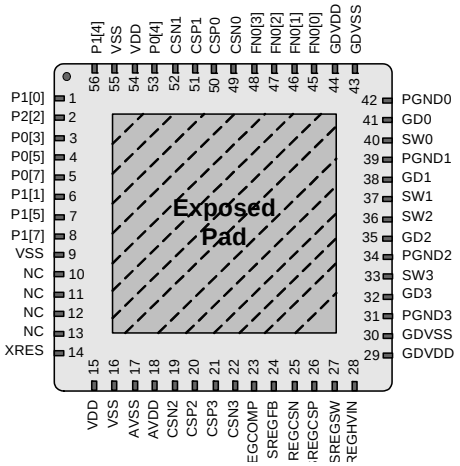
The CY8CLED04D01 and CY8CLED04D02 PowerPSoC devices are available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-1. CY8CLED04D0x 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I^{2}C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I^{2}C SCL (Secondary)/ISSP SCLK
7	I/O	I		P1[5]	GPIO/I^{2}C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I^{2}C SCL (Primary)
9				V_{SS}	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19			I	CSN2	Current Sense Negative Input - CSA2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				CSP3	Current Sense Positive Input and Power Supply - CSA3
22			I	CSN3	Current Sense Negative Input 3
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[1]	Power FET Ground 3
32			O	GD3	External Low Side Gate Driver 3
33				SW3	Power Switch 3
34				PGND2[1]	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				SW2	Power Switch 2
37				SW1	Power Switch 1
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[1]	Power FET Ground 1
40				SW0	Power Switch 0
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[1]	Power FETGround 0
43				GDV_{SS}	Gate Driver Ground

Figure 12-1. CY8CLED04D0x 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Note
1. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

12.2 CY8CLED04G01 56-Pin Part Pinout (without OCD)

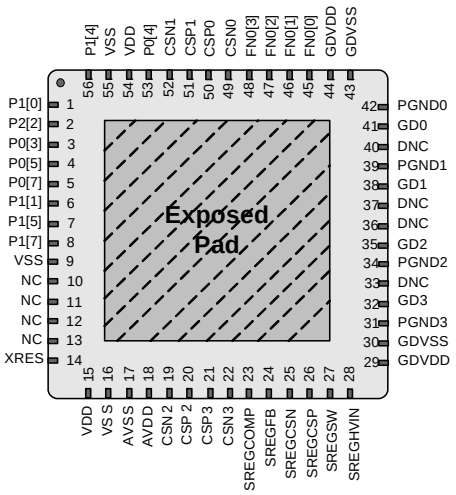
The CY8CLED04G01 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-2. CY8CLED04G01 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I^{2}C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I^{2}C SCL (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I^{2}C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I^{2}C SCL (Primary)
9				V_{SS}	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19			I	CSN2	Current Sense Negative Input 2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				CSP3	Current Sense Positive Input and Power Supply - CSA3
22			I	CSN3	Current Sense Negative Input 3
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[3]	Power FET Ground 3
32			O	GD3	External Low Side Gate Driver 3
33				DNC[2]	Do Not Connect
34				PGND2[3]	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				DNC[2]	Do Not Connect
37				DNC[2]	Do Not Connect
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[3]	Power FET Ground 1
40				DNC[2]	Do Not Connect
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[3]	Power FET Ground 0
43				GDV_{SS}	Gate Driver Ground
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Figure 12-2. CY8CLED04G01 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Notes
2. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
3. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

12.4 CY8CLED03D0x 56-Pin Part Pinout (without OCD)

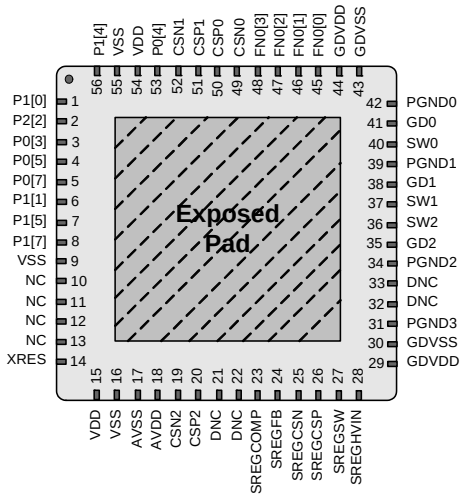
The CY8CLED03D01 and CY8CLED03D02 PowerPSoC devices are available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-4. CY8CLED03D0x 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I2C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCL (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I2C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I2C SCL (Primary)
9				V_{SS}	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19			I	CSN2	Current Sense Negative Input - CSA2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				DNC[5]	Do Not Connect
22				DNC[5]	Do Not Connect
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[6]	Power FET Ground 3
32				DNC[5]	Do Not Connect
33				DNC[5]	Do Not Connect
34				PGND2[6]	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				SW2	Power Switch 2
37				SW1	Power Switch 1
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[6]	Power FET Ground 1
40				SW0	Power Switch 0
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[6]	Power FETGround 0
43				GDV_{SS}	Gate Driver Ground

Figure 12-4. CY8CLED03D0x 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Notes
5. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
6. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

12.6 CY8CLED02D01 56-Pin Part Pinout (without OCD)

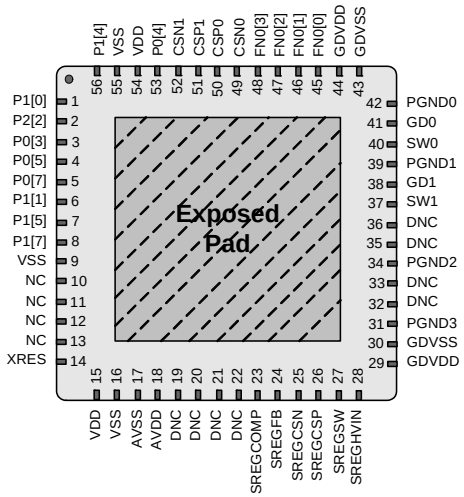
The CY8CLED02D01 PowerPSoC devices are available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-6. CY8CLED02D01 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I2C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCLK (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I2C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I2C SCL (Primary)
9				V_{SS}	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19				DNC[9]	Do Not Connect
20				DNC[9]	Do Not Connect
21				DNC[9]	Do Not Connect
22				DNC[9]	Do Not Connect
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[10]	Power FET Ground 3
32				DNC[9]	Do Not Connect
33				DNC[9]	Do Not Connect
34				PGND2[10]	Power FET Ground 2
35				DNC[9]	Do Not Connect
36				DNC[9]	Do Not Connect
37				SW1	Power Switch 1
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[10]	Power FET Ground 1
40				SW0	Power Switch 0
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[10]	Power FETGround 0
43				GDV_{SS}	Gate Driver Ground

Figure 12-6. CY8CLED02D01 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Notes
9. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
10. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

12.7 CY8CLED01D01 56-Pin Part Pinout (without OCD)

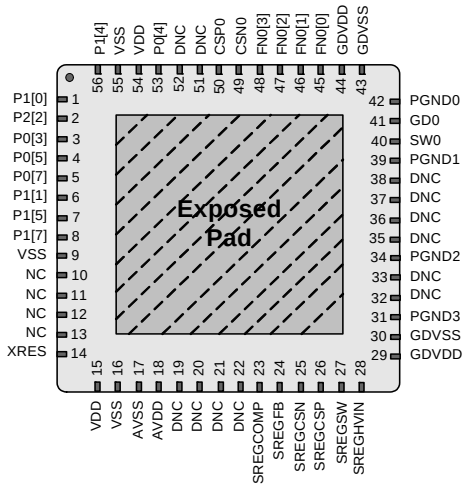
The CY8CLED01D01 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-7. CY8CLED01D01 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I2C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCLK (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I2C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I2C SCL (Primary)
9				V_{SS}	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19				DNC[11]	Do Not Connect
20				DNC[11]	Do Not Connect
21				DNC[11]	Do Not Connect
22				DNC[11]	Do Not Connect
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[12]	Power FET Ground 3
32				DNC[11]	Do Not Connect
33				DNC[11]	Do Not Connect
34				PGND2[12]	Power FET Ground 2
35				DNC[11]	Do Not Connect
36				DNC[11]	Do Not Connect
37				DNC[11]	Do Not Connect
38				DNC[11]	Do Not Connect
39				PGND1[12]	Power FET Ground 1
40				SW0	Power Switch 0
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[12]	Power FET Ground 0
43				GDV_{SS}	Gate Driver Ground

Figure 12-7. CY8CLED01D01 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				DNC[11]	Do Not Connect
52				DNC[11]	Do Not Connect
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Notes
11. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
12. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

13.5 Register Map Bank 1 Table: User Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	CSA0_CR	40	RW	ASC10CR0	80	RW	CMPCH0_CR	C0	RW
PRT0DM1	01	RW		41		ASC10CR1	81	RW	CMPCH2_CR	C1	RW
PRT0IC0	02	RW		42		ASC10CR2	82	RW	CMPCH4_CR	C2	RW
PRT0IC1	03	RW		43		ASC10CR3	83	RW	CMPCH6_CR	C3	RW
PRT1DM0	04	RW	CSA1_CR	44	RW	ASD11CR0	84	RW	CMPBNK8_CR	C4	RW
PRT1DM1	05	RW		45		ASD11CR1	85	RW	CMPBNK9_CR	C5	RW
PRT1IC0	06	RW		46		ASD11CR2	86	RW	CMPBNK10_CR	C6	RW
PRT1IC1	07	RW		47		ASD11CR3	87	RW	CMPBNK11_CR	C7	RW
PRT2DM0	08	RW	CSA2_CR	48	RW		88		CMPBNK12_CR	C8	RW
PRT2DM1	09	RW		49			89		CMPBNK13_CR	C9	RW
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
FN0DM0	0C	RW	CSA3_CR	4C	RW		8C			CC	
FN0DM1	0D	RW		4D			8D			CD	
FN0IC0	0E	RW		4E			8E			CE	
FN0IC1	0F	RW		4F			8F			CF	
	10			50		ASD20CR0	90	RW	GDI_O_IN	D0	RW
	11			51		ASD20CR1	91	RW	GDI_E_IN	D1	RW
	12			52		ASD20CR2	92	RW	GDI_O_OU	D2	RW
	13			53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
	14			54		ASC21CR0	94	RW	HYSCTLR0CR	D4	RW
	15			55		ASC21CR1	95	RW	HYSCTLR1CR	D5	RW
	16			56		ASC21CR2	96	RW	HYSCTLR2CR	D6	RW
	17			57		ASC21CR3	97	RW	HYSCTLR3CR	D7	RW
	18			58			98		MUX_CR0	D8	RW
	19			59			99		MUX_CR1	D9	RW
	1A			5A			9A		MUX_CR2	DA	RW
	1B			5B			9B			DB	
	1C			5C			9C		SREG_TST	DC	RW
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW	CMP_GO_EN	64	RW		A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7		DEC_CR2	E7	RW
DCB02FN	28	RW	ALT_CR1	68	RW		A8		IMO_TR	E8	RW
DCB02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	RW
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB			EB	
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBB10FN	30	RW	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10IN	31	RW	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10OU	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11FN	34	RW	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB01IN	35	RW	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB01OU	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCB12IN	39	RW	GDRV0_CR	79	RW	RDI1SYN	B9	RW		F9	
DCB12OU	3A	RW		7A		RDI1IS	BA	RW		FA	
	3B		GDRV1_CR	7B	RW	RDI1LT0	BB	RW		FB	
DCB13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCB13IN	3D	RW	GDRV2_CR	7D	RW	RDI1RO0	BD	RW	DAC_CR	FD	RW
DCB13OU	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
	3F		GDRV3_CR	7F	RW		BF		CPU_SCR0	FF	#

14. Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CLED04D0X, CY8CLED04G01, CY8CLED03D0X, CY8CLED03G01, CY8CLED02D01, and CY8CLED01D01 of the PowerPSoC device family. For the most up to date electrical specifications, confirm that you have the most recent datasheet by going to the web at http://www.cypress.com/powerpsoc. Specifications for Industrial rated devices are valid for –40 °C ≤ T_A ≤ 85 °C, T_J ≤ 115 °C and for Extended Temperature rated devices for –40 °C ≤ T_A ≤ 105 °C, T_J ≤ 125 °C, except where noted.

14.1 Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. Not all user guidelines are production tested.

Table 14-1. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	–	+115	°C	Higher storage temperatures reduces data retention time. Recommended storage temperature is 0 °C to 50 °C.
T_A	Ambient temperature with power applied	–40 –40	– –	+85 +105	°C °C	T_J ≤ 115 °C (industrial rated) T_J ≤ 125 °C (extended temperature rated)
V_{DD}, AV_{DD}, GDV_{DD}	Supply voltage on V_{DD}, AV_{DD}, and GDV_{DD}	–0.5	–	+6.0	V	Relative to V_{SS}, AV_{SS}, and GDV_{SS} respectively
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	Applies only to GPIO and FN0 pins
V_{IO2}	DC voltage applied to tristate	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{FET}	Maximum voltage from power Switch (SWx) to Power FET Ground (PGNDx)	–	–	36[13]	V	PGNDx is connected to GDV_{SS}
V_{REGIN}	Maximum voltage on SREGHVIN Pin relative to V_{SS}	–	–	36[13]	V	
V_{CSP},V_{CSN}	Maximum voltage applied to CSA pins relative to V_{SS}	–0.5	–	36[13]	V	
V_{SENSE}	Maximum input differential voltage across CSA input	–1.0	–	1.0	V	
I_{MAIO}	Maximum current into any port pin configured as analog driver	–50	–	+50	mA	
I_{MIO}	Maximum current into any port and function pin	–25	–	+50	mA	
LU	Latch up current	200	–	–	mA	JESD78A Conformal
ESD	Electrostatic discharge voltage	2000	–	–	V	Human Body Model ESD.
SR_{REGIN}	Ramp rate for the SREGHVIN pin	–	–	32	V/µs	
SR_{CSP}	Ramp rate for the CSPx pins	–	–	3.2	V/µs	
$SR_H V_{DD-FLB}$	High voltage supply ramp rate for floating load buck configuration	–	–	15	V/ms	For other topologies, to enable operation with faster ramp rates, or if the LED string voltage is < 6.5 V, see the *PowerPSoC Technical Reference Manual*.
SRV_{DD-EXT}	External V_{DD} supply ramp rate (V_{DD}, AV_{DD}, and GDV_{DD} pins)	–	–	0.2	V/µs	Applies only when powered by a source other than the Built-in Switching Regulator

Note
13. Stresses beyond the "Absolute Maximum Ratings" on page 30 may cause permanent damage to the device. You must ensure that the absolute maximum ratings are NEVER exceeded. Functional operation is not implied under any conditions beyond the "Electrical Characteristics" on page 31 onwards. Extended exposure to "Absolute Maximum Ratings" on page 30 may affect reliability of the device.

15.9 Power Peripheral Reference DAC Specification

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-16. Reference DAC DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{SDAC}	Supply current - reference DAC	–	–	600	µA	Mode 0 and Mode1
INL	Integral non linearity	–1 –1.5	– –	1 1.5	LSB LSB	Mode 0 Mode 1
DNL	Differential non linearity	–0.5	–	0.5	LSB	Mode 0 and Mode1
A_{ERROR}	Gain error	–5 –7	– –	5 7	LSB LSB	Mode 0 Mode 1
OS_{ERROR}	Offset error	–	–	1	LSB	Mode 0 and Mode1
V_{DACFS}	Fullscale voltage - reference DAC	– –	– –	2.6 1.3	LSB LSB	Mode 0 Mode 1
V_{DACMM}	Fullscale voltage mismatch (pair of reference DACs - even and odd)	– – – –	– – – –	9 14 10.5 15.5	LSB LSB LSB LSB	Mode 0 (DAC0 through DAC7) Mode 1 (DAC0 through DAC7) Mode 0 (DAC8 through DAC13) Mode 1 (DAC8 through DAC13)

Table 15-17. Reference DAC AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{SETTLE}	Output settling time to 0.5 LSB of final value	–	–	10	µs	Mode 0 and Mode1
$t_{STARTUP}$	Startup time to within 0.5 LSB of final value	–	–	10.5	µs	Mode 0 and Mode1

15.10 Power Peripheral Built-in Switching Regulator

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-18. Built-in Switching Regulator DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REGIN}	Input supply voltage range	7 8	– –	32 32	V V	Industrial rated Extended temperature rated See Absolute Maximum Ratings on page 30
V_{REGOUT}	Output voltage range	4.8	5.0	5.2	V	Does not include V_{RIPPLE}
V_{RIPPLE}	Output ripple	–	–	100	mV	
V_{UVLO}	Under voltage lockout voltage	5.5	–	6.5	V	$V_{REGIN} < V_{UVLO}$: Power down mode $V_{REGIN} > V_{UVLO}$: Active mode
I_{LOAD}	DC output current -active mode	0.01	–	250	mA	–
$I_{S,BSR}$	Supply current - built-in switching regulator	–	–	4	mA	–
$I_{SB,HV}$	Standby current (high voltage)	–	–	250	µA	–
I_{INRUSH}	Inrush current	– –	– –	1.2 1.5	A A	V_{REGIN} = 32 V, SR_{REGIN} = 32 V/ms (Industrial rated) V_{REGIN} = 32 V, SR_{REGIN} = 32 V/ms (Extended Temperature rated)
$R_{DS(ON),PFET}$	PFET drain to source ON resistance	–	2.5	–	Ω	
$Line_{REG}$	Line regulation	–	1	–	mV	I_{LOAD} = 250 mA, V_{REGIN} = 7 V to 32 V

Table 15-18. Built-in Switching Regulator DC Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
$Load_{REG}$	Load regulation	–	1	–	mV	V_{REGIN} = 24 V, I_{LOAD} = 2.5 mA to 250 mA
PSRR	Power supply rejection ratio	–	–60	–	dB	V_{RIPPLE} = 0.2 * V_{REGIN}, f_{RIPPLE} = 1 kHz to 10 kHz
E_{BSR}	Built-in switching regulator efficiency	80	–	–	%	V_{REGIN} = 24 V, I_{LOAD} = 250 mA

Table 15-19. Built-in Switching Regulator AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
f_{SW}	Switching frequency	0.956	1	1.04	MHz	–
t_{RESP}	Response time to within 0.5% of final value	–	10	–	µs	–
t_{SU}	Startup time	–	–	1	ms	–
t_{PD}	Power down time	–	–	100	µs	–
t_{PD_ACT}	Time from power down to active mode	–	–	1	ms	–
t_{ACT_PD}	Time from active mode to power down mode	–	–	50	µs	–
SR_{REGIN}	Ramp rate for the SREGHVIN pin	–	–	32	V/µs	See Absolute Maximum Ratings on page 30

Table 15-20. Built-in Switching Regulator Recommended Components

Component Name	Value	Unit	Notes
R_{fb1}	2	kΩ	Tolerance 1% and 0.05-W rated or better
R_{fb2}	0.698	kΩ	Tolerance 1% and 0.05-W rated or better
C_{comp}	2200	pF	Tolerance 20% and 6.3-V rated or better
R_{comp}	20	kΩ	Tolerance 5% and 0.05-W rated or better
L	47	µH	Tolerance 20% or better, Saturation current rating of 1.5 A or higher
R_{sense}	0.5	Ω	Tolerance 1% and 0.05 W (I_{LOAD} = 0.250 A) rated or better
C_1	10	µF	Ceramic, X7R grade, Minimum ESR of 0.1 Ω, 6.3-V rated
C_{in}	1	µF	Ceramic, X7R grade, 50-V rated (V_{REGIN} = 32 V)
D1	40/0.5	V/A	Schottky diode - Reverse voltage 40 V, average rectified forward current 0.5 A (V_{REGIN} = 32 V)

Note If the built-in switching regulator is not being used in a design, it must be configured as per the following instructions to ensure it is disabled in a safe state.

SREGFB: 5 V

SREGCSN: 5 V

SREGCSP: 5 V

SREGCOMP: Floating

SREGHVIN: ≥ VDD rail

SREGSW: Floating/Tie to SREGHVIN

If the switching regulator is disabled through wiring its input pins (as previously explained) then it must be disabled through software as well (bit SREG_TST[0] = 1), which is set in the Global Resources in the Interconnect View of PSoC Designer.

15.12 PSoC Core Operational Amplifier Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Capacitor PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block.

Table 15-23. Operational Amplifier DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 – – – – – –	 1.6 1.6 1.3 1.3 1.2 1.2	 10 15 8 13 7.5 12	 mV mV mV mV mV mV	 Industrial rated Extended temperature rated Industrial rated Extended temperature rated Industrial rated Extended temperature rated
TCV_{OSOA}	Average input offset voltage drift	–	7.0	35.0	µV / °C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	T_J = 25 °C.
V_{CMOA}	Common mode voltage range Common mode voltage range (high power or high opamp bias)	0.0 0.5	– –	V_{DD} V_{DD} – 0.5	V V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 60 60 80	 – – –	 – – –	 dB dB dB	–
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.5	 – – –	 – – –	 V V V	–
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 – – –	 – – –	 0.2 0.2 0.5	 V V V	–
I_{SOA}	Supply current (including associated analog output buffer) Power = low, opamp bias = low Power = low, opamp bias = high Power = medium, opamp bias = low Power = medium, opamp bias = high Power = high, opamp bias = low Power = high, opamp bias = high	 – – – – – –	 400 500 800 1200 2400 4600	 800 900 1000 1600 3200 6400	 µA µA µA µA µA µA	–
$PSRR_{OA}$	Supply voltage rejection ratio	52	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$.

Table 15-28. Analog Output Buffer AC Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
SR_{ROB}	Rising slew rate (20% to 80%), 1 V step, 100 pF load					–
	Power = low	0.65	–	–	V/µs	
	Power = high	0.65	–	–	V/µs	
SR_{FOB}	Falling slew rate (80% to 20%), 1 V step, 100 pF load					–
	Power = low	0.65	–	–	V/µs	
	Power = high	0.65	–	–	V/µs	
BW_{OBSS}	Small signal bandwidth, 20 mV_{pp}, 3 dB BW, 100 pF load					–
	Power = low	0.8	–	–	MHz	
	Power = high	0.8	–	–	MHz	
BW_{OBLS}	Large signal bandwidth, 1 V_{pp}, 3 dB BW, 100 pF load					–
	Power = low	300	–	–	kHz	
	Power = high	300	–	–	kHz	

15.15 PSoC Core Analog Reference

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for extended temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the analog continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Table 15-29. Analog Reference DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
BG	Bandgap voltage reference	1.28 1.27	1.30 1.30	1.32 1.33	V V	Industrial rated Extended Temperature rated
–	AGND = $V_{DD}/2$[16]	$V_{DD}/2 - 0.04$ $V_{DD}/2 - 0.02$	$V_{DD}/2 - 0.01$ $V_{DD}/2$	$V_{DD}/2 + 0.007$ $V_{DD}/2 + 0.02$	V V	Industrial rated Extended Temperature rated
–	AGND = 2 x BandGap[16]	2 x BG – 0.048	2 x BG – 0.030	2 x BG + 0.024	V	
–	AGND = BandGap[16]	BG – 0.009	BG + 0.008	BG + 0.016	V	
–	AGND = 1.6 x BandGap[16]	1.6 x BG – 0.022	1.6 x BG – 0.010	1.6 x BG + 0.018	V	
–	AGND Block to Block Variation (AGND = $V_{DD}/2$)[16]	–0.034	0.000	0.034	V	
–	RefHi = $V_{DD}/2$ + BandGap	$V_{DD}/2$ + BG – 0.10	$V_{DD}/2$ + BG	$V_{DD}/2$ + BG + 0.10	V	
–	RefHi = 3 x BandGap	3 x BG – 0.06	3 x BG	3 x BG + 0.06	V	
–	RefHi = 3.2 x BandGap	3.2 x BG – 0.112	3.2 x BG	3.2 x BG + 0.076	V	
–	RefLo = $V_{DD}/2$ – BandGap	$V_{DD}/2$ – BG – 0.04 $V_{DD}/2$ – BG – 0.06	$V_{DD}/2$ – BG + 0.024 $V_{DD}/2$ – BG	$V_{DD}/2$ – BG + 0.04 $V_{DD}/2$ – BG + 0.06	V V	Industrial rated Extended Temperature rated
–	RefLo = BandGap	BG – 0.06	BG	BG + 0.06	V	

15.16 PSoC Core Analog Block

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-30. Analog Block DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor unit value (continuous time)	–	12.2	–	kΩ	
C_{SC}	Capacitor unit value (switched capacitor)	–	80	–	fF	

Notes
16. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3 V ± 0.02 V.

15.17 PSoC Core POR and LVD

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the *PowerPSoC Technical Reference Manual* for more information on the VLT_CR register.

Table 15-31. POR and LVD DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PPOR2}	V_{DD} Value for PPOR Trip PORLEV[1:0] = 10b	–	4.55	4.70	V	–
	V_{DD} Value for LVD Trip					–
V_{LVD6}	VM[2:0] = 110b	4.62	4.73	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.81	4.95	V	

15.18 PSoC Core Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-32. Programming DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDP}	Supply current during programming or verify	–	15	30	mA	–
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	–
V_{IHP}	Input high voltage during programming or verify	2.1	–	–	V	–
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull down resistor.
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	–
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	–
$Flash_{ENPB}$	Flash endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[17]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention[18]	10	–	–	Years	–

Notes
17. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36 x 1 blocks of 50,000 maximum cycles each, 36 x 2 blocks of 25,000 maximum cycles each, or 36 x 4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36 x 50,000 and that no single block ever sees more than 50,000 cycles)
18. Guaranteed for –40 °C ≤ T_A ≤ 85 °C for Industrial rated devices and –40 °C ≤ T_A ≤ 105 °C for Extended Temperature rated devices.

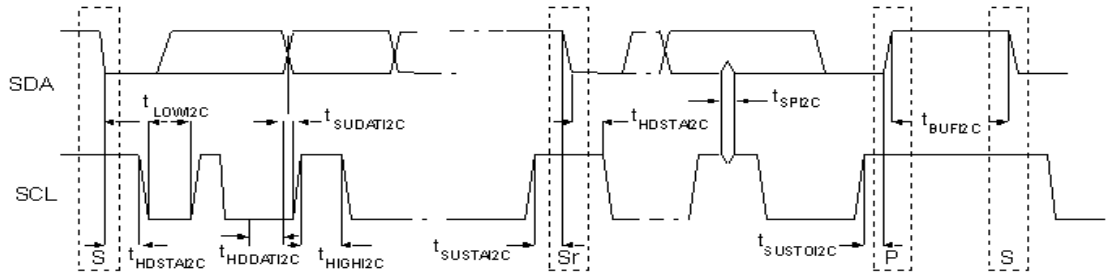
15.20 PSoC Core I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-35. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
f_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz	–
$t_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	–
t_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs	–
$t_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs	–
$t_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs	–
$t_{HDDATI2C}$	Data hold time	0	–	0	–	µs	–
$t_{SUDATI2C}$	Data setup time	250	–	100[21]	–	ns	–
$t_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs	–
t_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs	–
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	0	50	ns	–

Figure 15-8. Definition of Timing for Fast/Standard Mode on the I²C Bus



Note

21. A fast mode I²C bus device can be used in a standard mode I²C bus system, but the requirement $t_{SUDATI2} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line trmax + $t_{SUDATI2}$ = 1000 + 250 = 1250 ns (according to the standard mode I²C bus specification) before the SCL line is released.

21. Sales, Solutions, and Legal Information

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