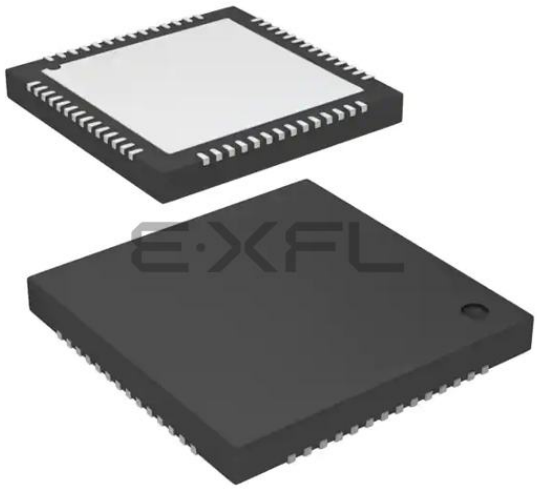


Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Intelligent LED Driver
Core Processor	M8C
Program Memory Type	FLASH (16KB)
Controller Series	CY8CLED
RAM Size	1K x 8
Interface	DALI, DMX512, I²C, IrDA, SPI, UART/USART
Number of I/O	14
Voltage - Supply	4.75V ~ 5.25V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad
Supplier Device Package	56-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8cled02d01-56ltxi

2. Contents

Figure 3-2. CY8CLED04G01 Logic Block Diagram

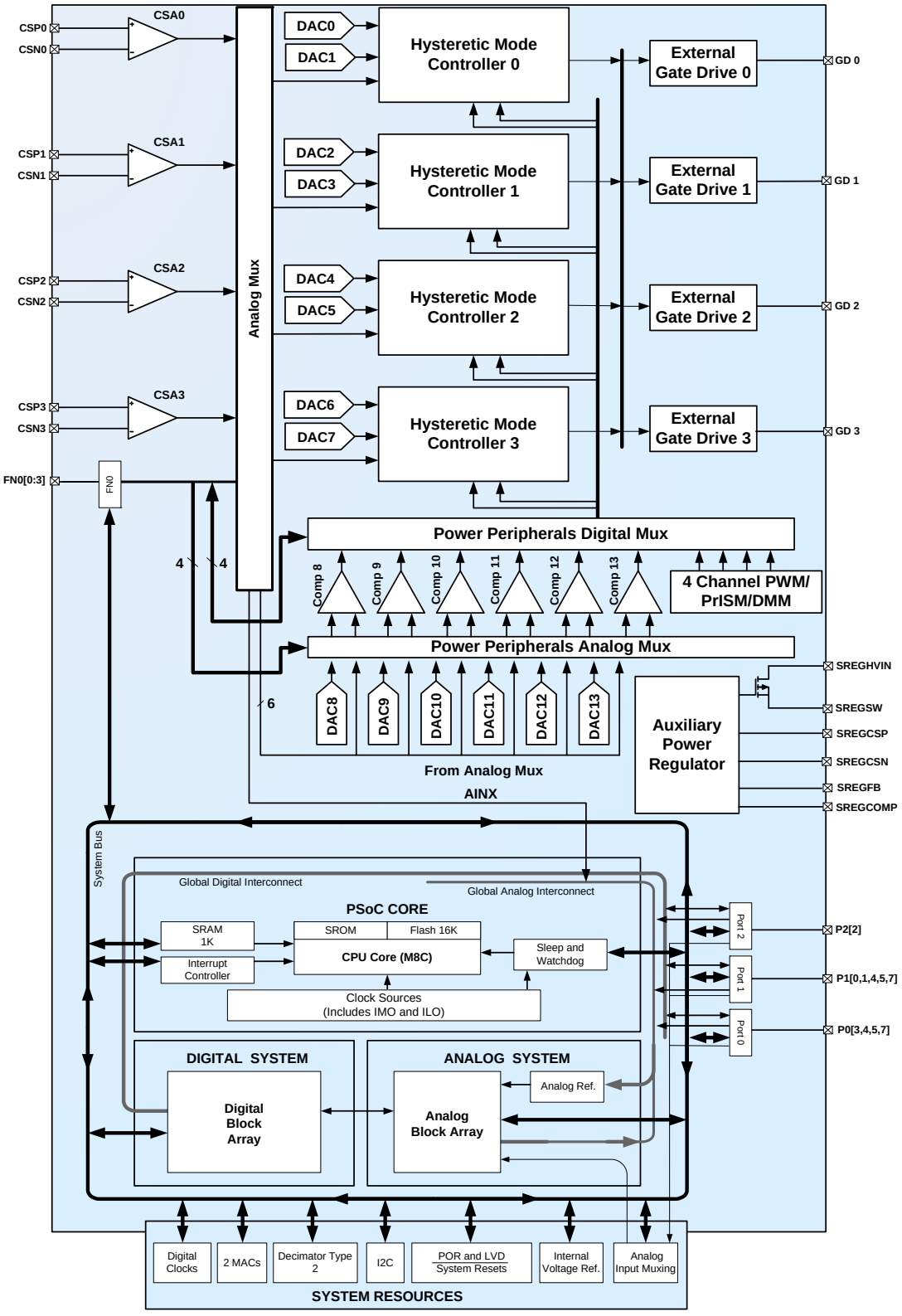


Figure 3-3. CY8CLED03D0x Logic Block Diagram

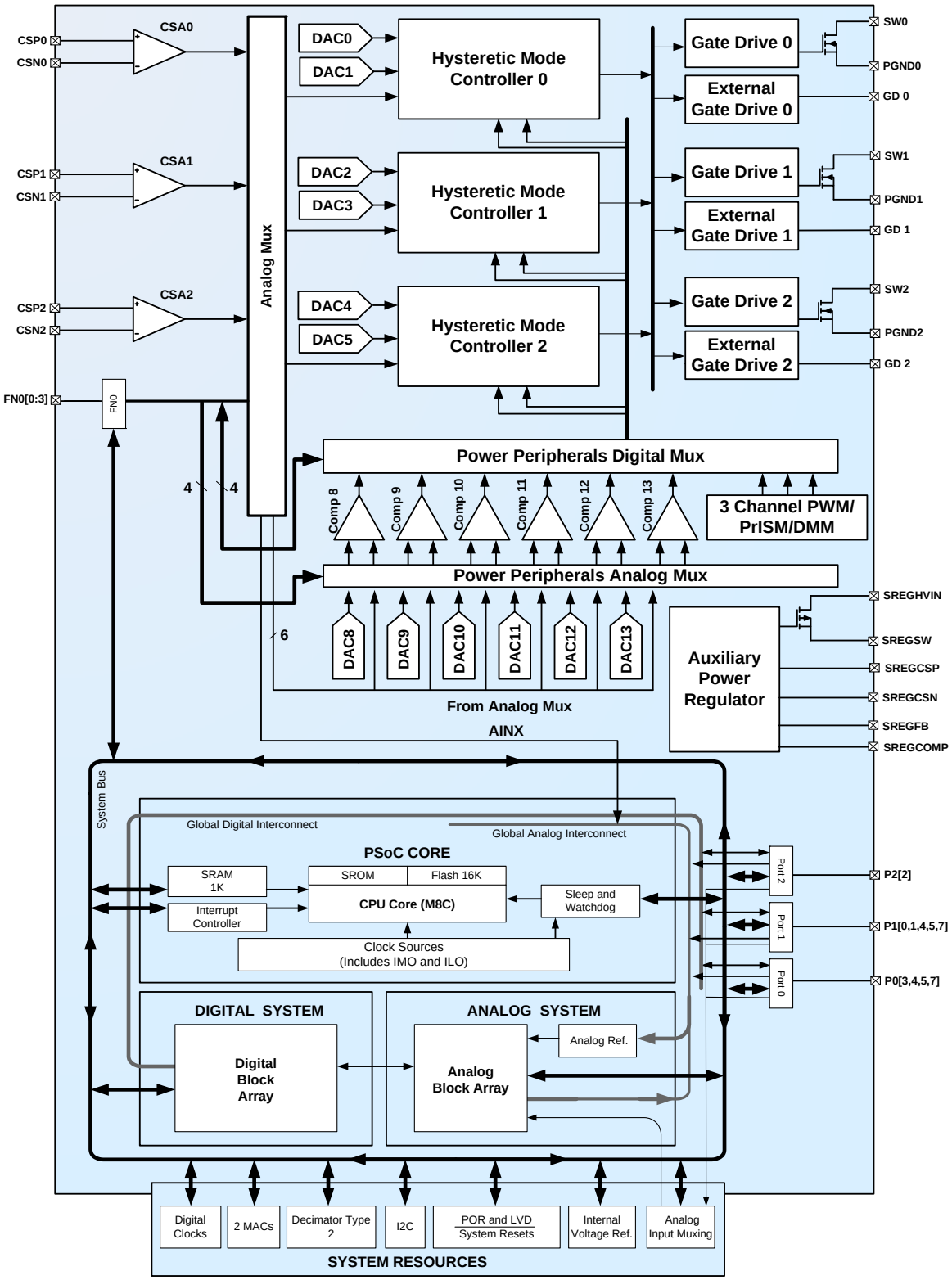


Figure 3-5. CY8CLED02D01 Logic Block Diagram

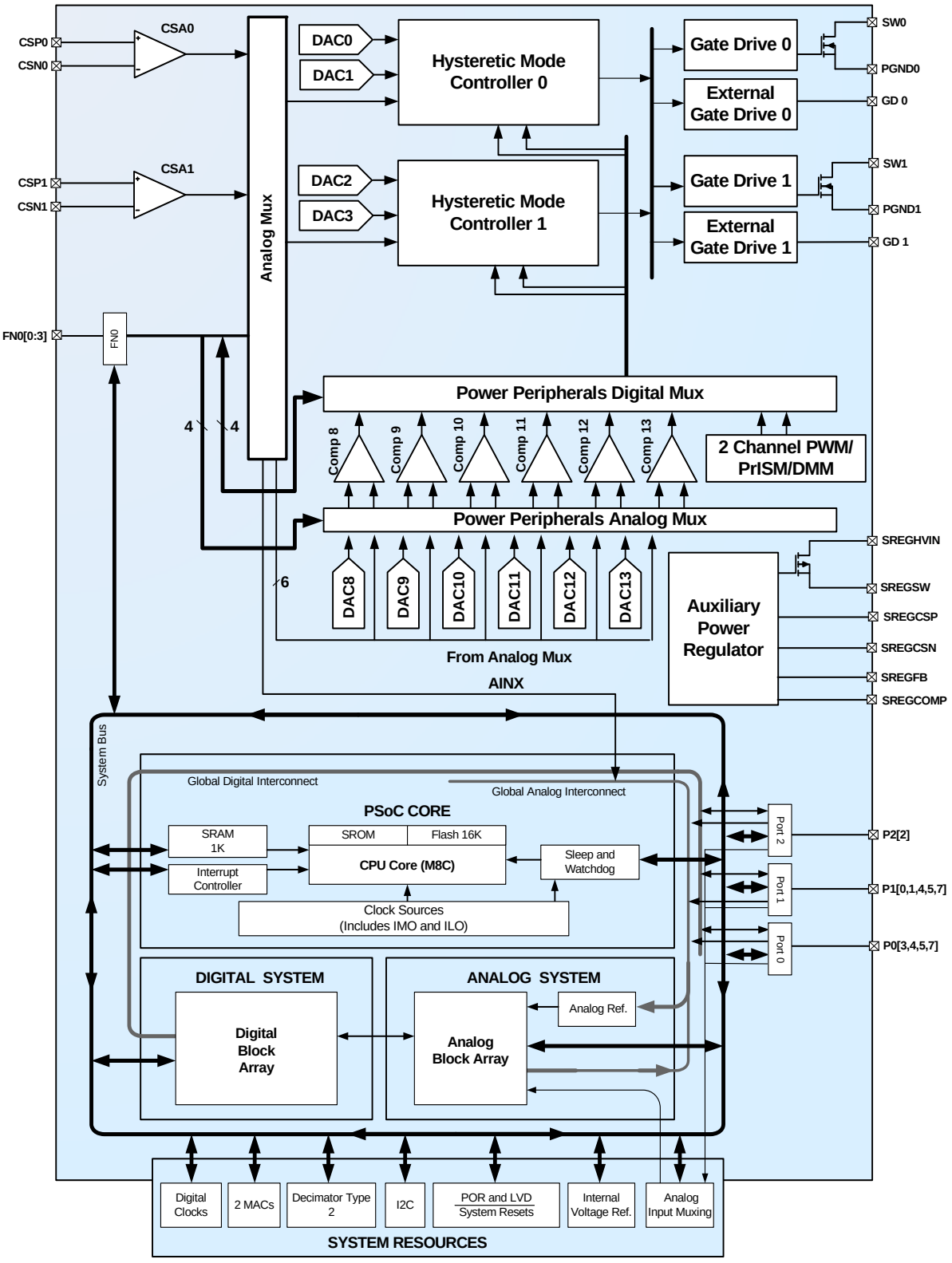
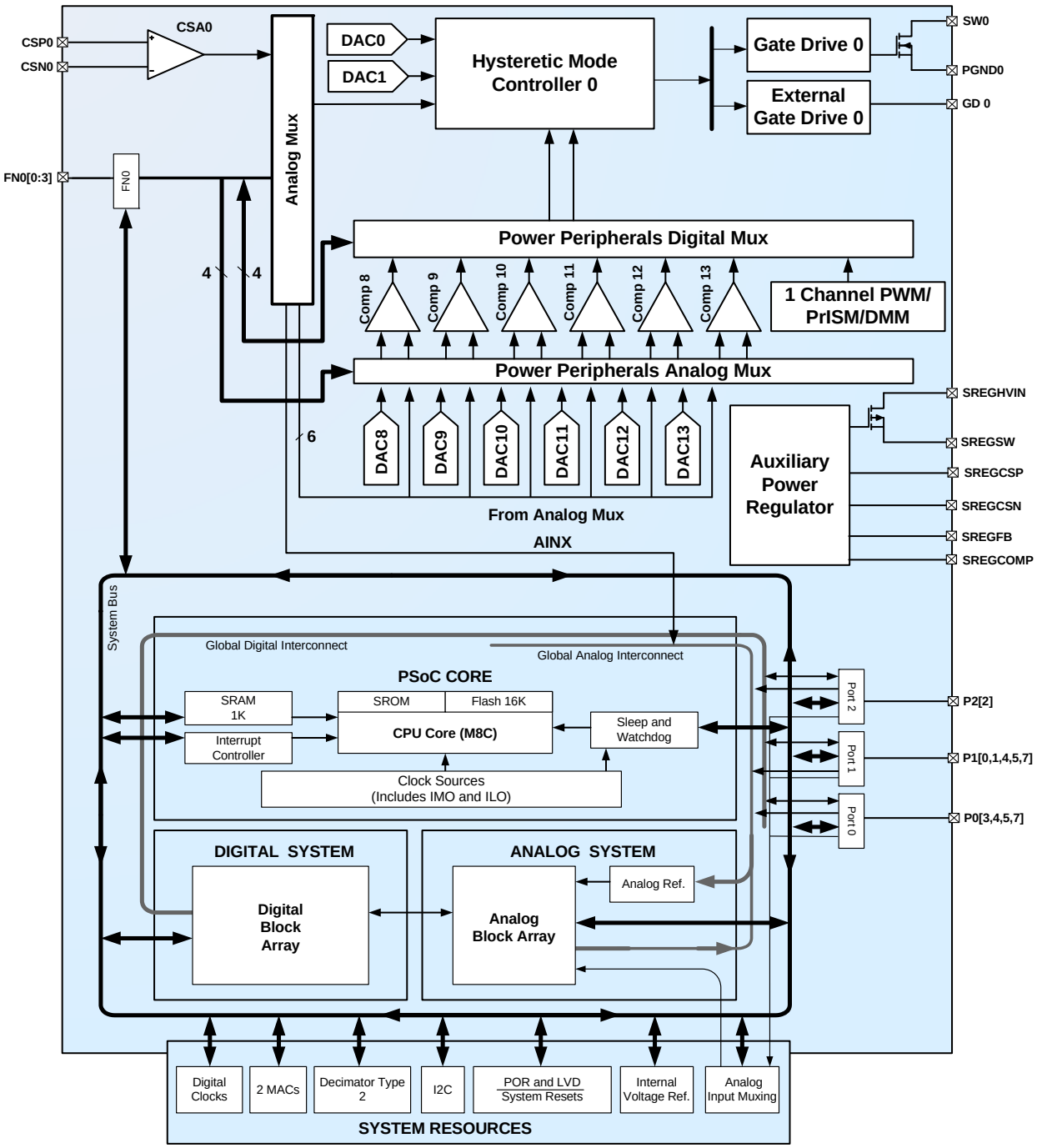


Figure 3-6. CY8CLED01D01 Logic Block Diagram



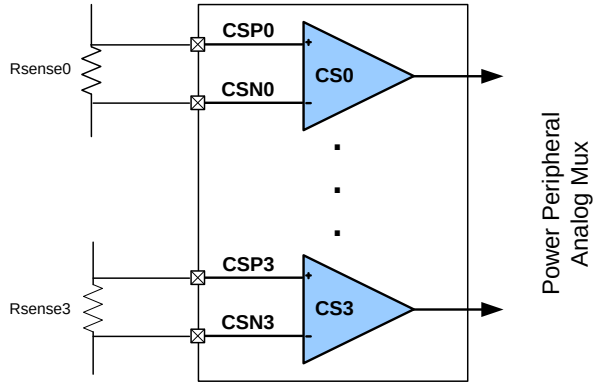
the routing is done. Table 5-1 illustrates example values of R_{sense} for different currents.

The method to calculate the R_{sense} value for a desired average current is explained in the application note CY8CLED0xx0x: Topology and Design Guide for Circuits using PowerPSoC - AN52699

Table 5-1. R_{sense} Values for Different Currents

Max Load Current (mA)	Typical R_{sense} (mΩ)
1000	100
750	130
500	200
350	300

Figure 5-3. High Side Current Measurement



5.6 Voltage Comparators

There are six comparators that provide high speed comparator operation for over voltage, over current, and various other system event detections. For example, the comparators may be used for zero crossing detection for an AC input line or monitoring total DC bus current. Programmable internal analog routing enables these comparators to monitor various analog signals. These comparators include the following key features:

- High speed comparator operation: 100 ns response time
- Programmable interrupt generation
- Low input offset voltage and input bias currents

Six precision voltage comparators are available. The differential positive and negative inputs of the comparators are routed from the analog multiplexer and the output goes to the digital multiplexer. A programmable inverter is used to select the output polarity. User-selectable hysteresis can be enabled or disabled to trade-off noise immunity versus comparator sensitivity.

5.7 Reference DACs

The reference DACs are used to generate set points for various analog modules such as Hysteretic controllers and comparators. The reference DACs include the following key features:

- 8-bit resolution
- Guaranteed monotonic operation
- Low gain errors
- 10 us settling time

These DACs are available to provide programmable references for the various analog and comparator functions and are controlled by memory mapped registers.

DAC[0:7] are embedded in the hysteretic controllers and are required to set the upper and lower thresholds for channel 0 to 3.

DAC [8:13] are connected to the Power Peripherals Analog Multiplexer and provide programmable references to the comparator bank. These are used to set trip points which enable over voltage, over current, and other system event detection.

5.8 Built-in Switching Regulator

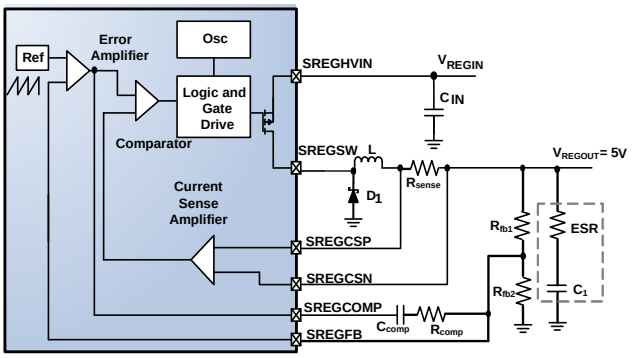
The switching regulator is used to power the low voltage (5 V portion of the PowerPSoC) from the input line. This regulator is based upon a peak current control loop which can support up to 250 mA of output current. The current not being consumed by PowerPSoC is used to power additional system peripherals. The key features of the built-in switching regulator include:

- Ability to self power device from input line
- Small filter component sizes
- Fast response to transients

Refer to Table 15-20 for component values.

The 'Ref' signal that forms the reference to the Error Amplifier is internally generated and there is no user control over it.

Figure 5-4. Built-in Switching Regulator



5.9 Analog Multiplexer

The PowerPSoC family's analog MUX is designed to route signals from the CSA output, function I/O pins and the DACs to comparator inputs and the current sense inputs of the hysteretic controllers. Additionally, CSA outputs can be routed to the AINX block using this MUX.

For a full matrix representation of all possible routing using this MUX, refer to the PowerPSoC Technical Reference Manual.

The CPU configures the Power Peripherals Analog Multiplexer connections using memory mapped registers. The analog multiplexer includes the following key features:

- Signal integrity for minimum signal corruption

5.10 Digital Multiplexer

The PowerPSoC family's digital MUX is a configurable switching matrix that connects the power peripheral digital resources.

For a full matrix representation of all possible routing using this MUX, refer to the PowerPSoC Technical Reference Manual.

This power peripheral digital multiplexer is independent of the main PSoC digital buses or global interconnect of the PSoC core. The digital multiplexer includes the following key features:

- Connect signals to ensure needed flexibility

5.11 Function Pins (FN0[0:3])

The function I/O pins are a set of dedicated control pins used to perform system level functions with the power peripheral blocks of the PowerPSoC. These pins are dynamically configurable, enabling them to perform a multitude of input and output functions. These I/Os have direct access to the input and output of the voltage comparators, input of the hysteretic controller, and output of the digital PWM blocks for the device. The function I/O pins are register mapped. The microcontroller can control and read the state of these pins and the interrupt function.

Some of the key system benefits of the function I/O are:

- Enabling an external higher voltage current-sense amplifier as shown in Figure 5-5.
- Synchronizing dimming of multiple PowerPSoC controllers as shown in Figure 5-6.
- Programmable fail-safe monitor and dedicated shutdown of hysteretic controller as shown in Figure 5-7.

Along with the these functions, these I/Os also provide interrupt functionality, enabling intelligent system responses to power control lighting system status.

Figure 5-5. External CSA and FET Application

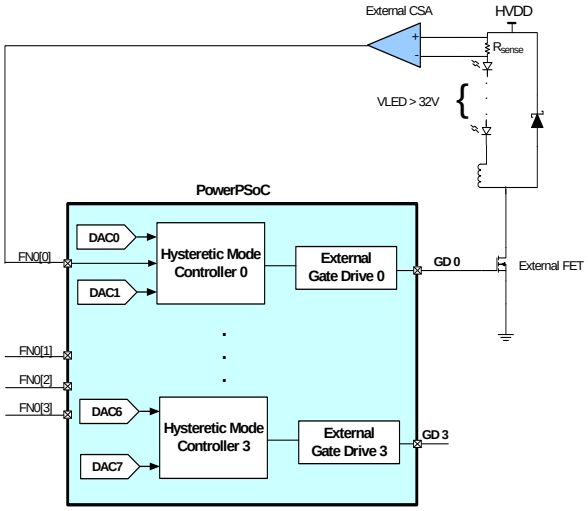


Figure 5-6. PowerPSoC in Master/Slave Configuration

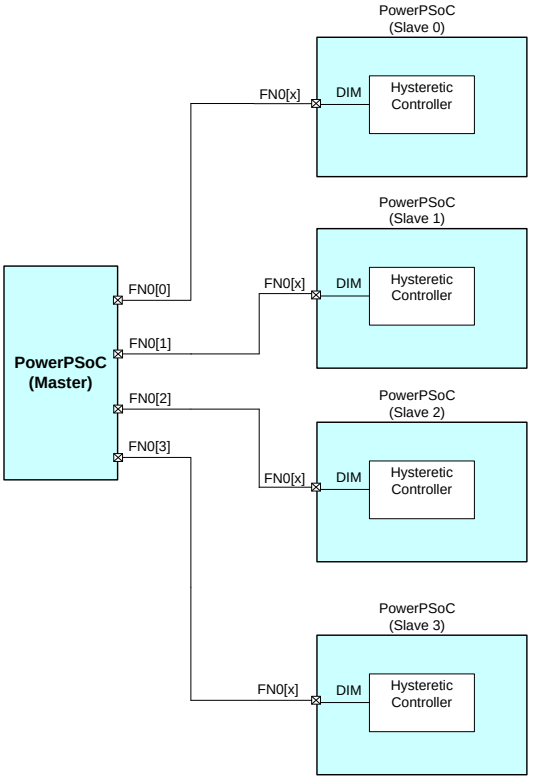
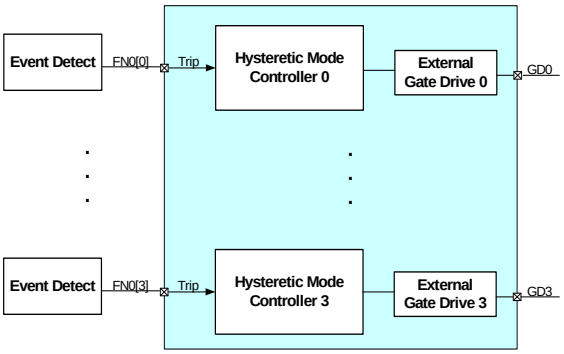


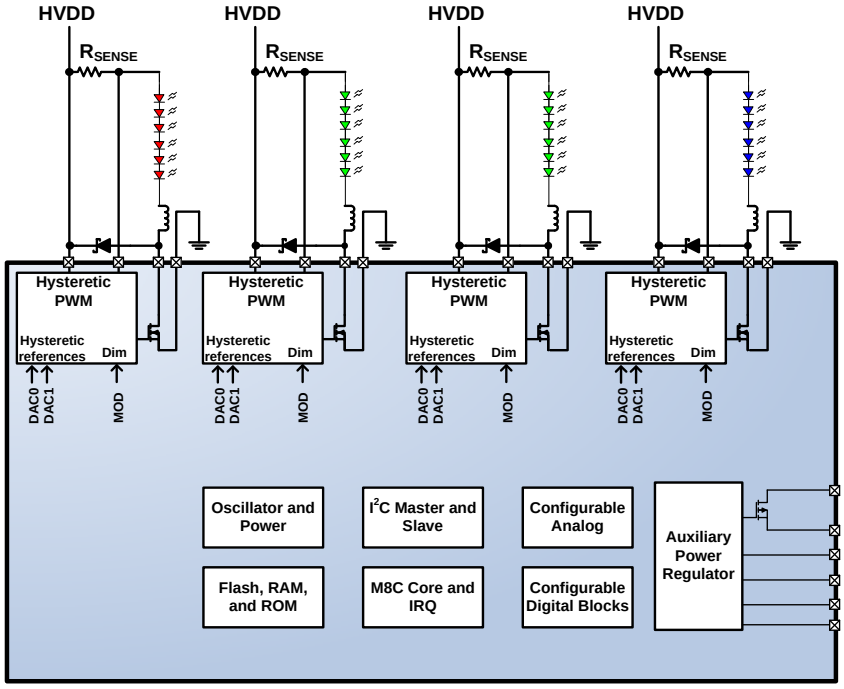
Figure 5-7. Event Detection



7. Applications

The PowerPSoC family of devices can be used to add hysteretic current control capability to power applications. The devices can be used to control current in devices such as LEDs, heating elements, and solenoids. For LED applications, all high-brightness LEDs (HBLEDs) can be controlled using the PowerPSoC. The following figures show examples of applications in which the PowerPSoC family of devices adds intelligent power control for power applications.

Figure 7-1. LED Lighting with RGGB Color Mixing Configured as Floating Load Buck Converter



8. PowerPSoC Device Characteristics

There are two major groups of devices in the PowerPSoC family. One group is a 4-channel 56-pin QFN and the other is a 3-channel 56-pin QFN. These are summarized in the following table.

Table 8-1. PowerPSoC Device Characteristics

Device Group	Internal Power FETs	External Gate Drivers	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8CLED04D01-56LTXI	4X1.0 A	4	14	2	8	14	2	2	6	1 K	16 K
CY8CLED04D02-56LTXI	4X0.5 A	4	14	2	8	14	2	2	6	1 K	16 K
CY8CLED04G01-56LTXI	0	4	14	2	8	14	2	2	6	1 K	16 K
CY8CLED03D01-56LTXI	3X1.0 A	3	14	2	8	14	2	2	6	1 K	16 K
CY8CLED03D02-56LTXI	3X0.5 A	3	14	2	8	14	2	2	6	1 K	16 K
CY8CLED03G01-56LTXI	0	3	14	2	8	14	2	2	6	1 K	16 K
CY8CLED02D01-56LTXI	2X1.0 A	2	14	2	8	14	2	2	6	1 K	16 K
CY8CLED01D01-56LTXI	1X1.0 A	1	14	2	8	14	2	2	6	1 K	16 K
CY8CLED01D01-56LTXQ	1X1.0 A	1	14	2	8	14	2	2	6	1 K	16 K

9. Getting Started

The quickest way to understand the PowerPSoC device is to read this datasheet and then use the PSoC Designer integrated development environment (IDE). This datasheet is an overview of the PowerPSoC integrated circuit and presents specific pin, register, and electrical specifications. For in depth information, along with detailed programming information, refer to the *PowerPSoC Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PowerPSoC device datasheets on the web at www.cypress.com.

9.1 Application Notes

Application notes are an excellent introduction to a wide variety of possible PowerPSoC designs. Layout guidelines, thermal management and firmware design guidelines are some of the topics covered. To view the PowerPSoC application notes, go to htttp://www.cypress.com/powerpsoc and click on the Application Notes link.

9.2 Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store contains development kits, C compilers, and all accessories for PowerPSoC development. For more information on the kits or to purchase a kit from the Cypress web site, go to htttp://www.cypress.com/powerpsoc and click on the Development Kits link.

9.3 Training

Free PowerPSoC technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

9.4 CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PowerPSoC designs. To contact or become a PSoC Consultant go to www.cypress.com/cypros.

9.5 Technical Support

PowerPSoC application engineers take pride in fast and accurate response. They can be reached with a 24-hour guaranteed response at http://www.cypress.com/support/. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

10. Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE runs on Windows XP, Windows Vista, or Windows 7.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built-in support for third-party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PowerPSoC family.

10.1 PSoC Designer Software Subsystems

10.1.1 Chip-Level View

The chip-level view is a more traditional integrated development environment (IDE) based on PSoC Designer. Choose a base device to work with and then select different onboard analog and digital components called user modules that use the PowerPSoC blocks. Examples of user modules are current sense amplifiers, PrISM, PWM, DMM, Floating Load Buck, and Boost. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

10.1.2 Code Generation Tools

PSoC Designer supports multiple third party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to merge seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PowerPSoC family of devices. The products allow you to create complete C programs for the PowerPSoC family of devices.

The optimizing C compilers provide all the features of C tailored to the PowerPSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

10.1.3 Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PowerPSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

10.1.4 Online Help System

The online help system displays online, context-sensitive help for you. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to faqs and an Online Support Forum to aid the designer in getting started.

12.2 CY8CLED04G01 56-Pin Part Pinout (without OCD)

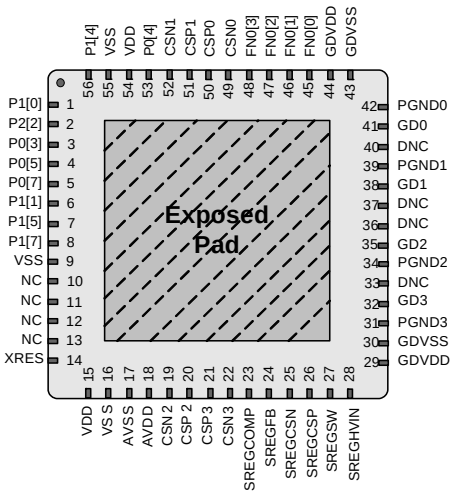
The CY8CLED04G01 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-2. CY8CLED04G01 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I^{2}C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I^{2}C SCL (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I^{2}C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I^{2}C SCL (Primary)
9				V_{SS}	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19			I	CSN2	Current Sense Negative Input 2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				CSP3	Current Sense Positive Input and Power Supply - CSA3
22			I	CSN3	Current Sense Negative Input 3
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[3]	Power FET Ground 3
32			O	GD3	External Low Side Gate Driver 3
33				DNC[2]	Do Not Connect
34				PGND2[3]	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				DNC[2]	Do Not Connect
37				DNC[2]	Do Not Connect
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[3]	Power FET Ground 1
40				DNC[2]	Do Not Connect
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[3]	Power FET Ground 0
43				GDV_{SS}	Gate Driver Ground
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Figure 12-2. CY8CLED04G01 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Notes
2. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
3. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

12.5 CY8CLED03G01 56-Pin Part Pinout (without OCD)

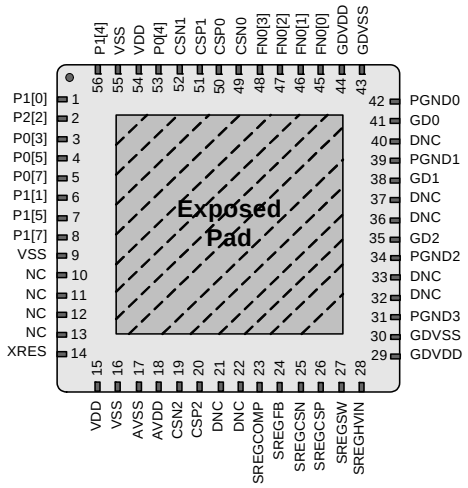
The CY8CLED03G01 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-5. CY8CLED03G01 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I2C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCL (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I2C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I2C SCL (Primary)
9				V_{SS}	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19			I	CSN2	Current Sense Negative Input 2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				DNC[7]	Do Not Connect
22				DNC[7]	Do Not Connect
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[8]	Power FET Ground 3
32				DNC[7]	Do Not Connect
33				DNC[7]	Do Not Connect
34				PGND2[8]	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				DNC[7]	Do Not Connect
37				DNC[7]	Do Not Connect
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[8]	Power FET Ground 1
40				DNC[7]	Do Not Connect
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[8]	Power FET Ground 0
43				GDV_{SS}	Gate Driver Ground

Figure 12-5. CY8CLED03G01 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Notes
7. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
8. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

14. Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CLED04D0X, CY8CLED04G01, CY8CLED03D0X, CY8CLED03G01, CY8CLED02D01, and CY8CLED01D01 of the PowerPSoC device family. For the most up to date electrical specifications, confirm that you have the most recent datasheet by going to the web at http://www.cypress.com/powerpsoc. Specifications for Industrial rated devices are valid for –40 °C ≤ T_A ≤ 85 °C, T_J ≤ 115 °C and for Extended Temperature rated devices for –40 °C ≤ T_A ≤ 105 °C, T_J ≤ 125 °C, except where noted.

14.1 Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. Not all user guidelines are production tested.

Table 14-1. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	–	+115	°C	Higher storage temperatures reduces data retention time. Recommended storage temperature is 0 °C to 50 °C.
T_A	Ambient temperature with power applied	–40 –40	– –	+85 +105	°C °C	T_J ≤ 115 °C (industrial rated) T_J ≤ 125 °C (extended temperature rated)
V_{DD}, AV_{DD}, GDV_{DD}	Supply voltage on V_{DD}, AV_{DD}, and GDV_{DD}	–0.5	–	+6.0	V	Relative to V_{SS}, AV_{SS}, and GDV_{SS} respectively
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	Applies only to GPIO and FN0 pins
V_{IO2}	DC voltage applied to tristate	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{FET}	Maximum voltage from power Switch (SWx) to Power FET Ground (PGNDx)	–	–	36[13]	V	PGNDx is connected to GDV_{SS}
V_{REGIN}	Maximum voltage on SREGHVIN Pin relative to V_{SS}	–	–	36[13]	V	
V_{CSP},V_{CSN}	Maximum voltage applied to CSA pins relative to V_{SS}	–0.5	–	36[13]	V	
V_{SENSE}	Maximum input differential voltage across CSA input	–1.0	–	1.0	V	
I_{MAIO}	Maximum current into any port pin configured as analog driver	–50	–	+50	mA	
I_{MIO}	Maximum current into any port and function pin	–25	–	+50	mA	
LU	Latch up current	200	–	–	mA	JESD78A Conformal
ESD	Electrostatic discharge voltage	2000	–	–	V	Human Body Model ESD.
SR_{REGIN}	Ramp rate for the SREGHVIN pin	–	–	32	V/µs	
SR_{CSP}	Ramp rate for the CSPx pins	–	–	3.2	V/µs	
$SR_H V_{DD-FLB}$	High voltage supply ramp rate for floating load buck configuration	–	–	15	V/ms	For other topologies, to enable operation with faster ramp rates, or if the LED string voltage is < 6.5 V, see the *PowerPSoC Technical Reference Manual*.
SRV_{DD-EXT}	External V_{DD} supply ramp rate (V_{DD}, AV_{DD}, and GDV_{DD} pins)	–	–	0.2	V/µs	Applies only when powered by a source other than the Built-in Switching Regulator

Note
13. Stresses beyond the "Absolute Maximum Ratings" on page 30 may cause permanent damage to the device. You must ensure that the absolute maximum ratings are NEVER exceeded. Functional operation is not implied under any conditions beyond the "Electrical Characteristics" on page 31 onwards. Extended exposure to "Absolute Maximum Ratings" on page 30 may affect reliability of the device.

15.7 Power Peripheral Current Sense Amplifier

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to V_{DD} of 5 V and HV_{DD} of 32 V at 25 °C. These are for design guidance only.

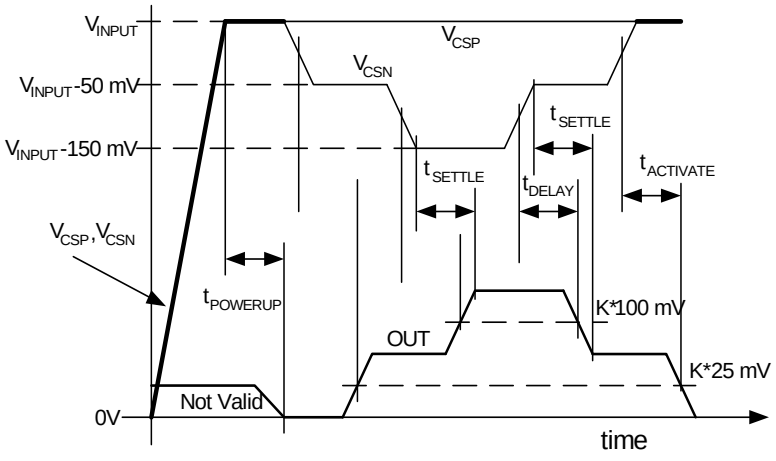
Table 15-12. Current Sense Amplifier DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ICM}	Input common mode voltage operating range	7	–	32	V	Either terminal of the amplifier must not exceed this range for functionality
$V_{ICM(Tolerant)}$	Non functional operating range	0	–	32		Absolute maximum rating for V_{SENSE} should never be exceeded. See Absolute Maximum Ratings on page 30
V_{SENSE}	Input differential voltage range	0	–	150	mV	
$I_{S,CSA}$	Supply current - CSA	–	–	1	mA	Enabling CSA causes an incremental draw of 1 mA on the AV_{DD} rail.
I_{BIASP}	Input bias current (+)	–	–	600	µA	
I_{BIASN}	Input bias current (-)	–	–	1	µA	
PSR_{HV}	Power supply rejection (CSP pin)	–	–	–25	dB	$f_{SW} < 2$ MHz
K	Gain	19.7 19.4	20 20	20.3 20.6	V/V V/V	V_{SENSE} = 50 mV to 130 mV (Industrial rated) V_{SENSE} = 50 mV to 130 mV (Extended Temperature rated)
V_{IOS}	Input offset	–	2	4	mV	V_{SENSE} = 50 mV to 130 mV
C_{IN_CSP}	CSP input capacitance	–	–	5	pF	
C_{IN_CSN}	CSN input capacitance	–	–	2	pF	

Table 15-13. Current Sense Amplifier AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{SETTLE}	Output settling time to 1% of final value	–	–	5	µs	
$t_{POWERUP}$	Power up time to 1% of final value	–	–	5	µs	

Figure 15-4. Current Sense Amplifier Timing Diagram



15.12 PSoC Core Operational Amplifier Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Capacitor PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block.

Table 15-23. Operational Amplifier DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 – – – – – –	 1.6 1.6 1.3 1.3 1.2 1.2	 10 15 8 13 7.5 12	 mV mV mV mV mV mV	 Industrial rated Extended temperature rated Industrial rated Extended temperature rated Industrial rated Extended temperature rated
TCV_{OSOA}	Average input offset voltage drift	–	7.0	35.0	µV / °C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	T_J = 25 °C.
V_{CMOA}	Common mode voltage range Common mode voltage range (high power or high opamp bias)	0.0 0.5	– –	V_{DD} V_{DD} – 0.5	V V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 60 60 80	 – – –	 – – –	 dB dB dB	–
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.5	 – – –	 – – –	 V V V	–
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 – – –	 – – –	 0.2 0.2 0.5	 V V V	–
I_{SOA}	Supply current (including associated analog output buffer) Power = low, opamp bias = low Power = low, opamp bias = high Power = medium, opamp bias = low Power = medium, opamp bias = high Power = high, opamp bias = low Power = high, opamp bias = high	 – – – – – –	 400 500 800 1200 2400 4600	 800 900 1000 1600 3200 6400	 µA µA µA µA µA µA	–
$PSRR_{OA}$	Supply voltage rejection ratio	52	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$.

Table 15-28. Analog Output Buffer AC Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
SR_{ROB}	Rising slew rate (20% to 80%), 1 V step, 100 pF load					–
	Power = low	0.65	–	–	V/µs	
	Power = high	0.65	–	–	V/µs	
SR_{FOB}	Falling slew rate (80% to 20%), 1 V step, 100 pF load					–
	Power = low	0.65	–	–	V/µs	
	Power = high	0.65	–	–	V/µs	
BW_{OBSS}	Small signal bandwidth, 20 mV_{pp}, 3 dB BW, 100 pF load					–
	Power = low	0.8	–	–	MHz	
	Power = high	0.8	–	–	MHz	
BW_{OBLS}	Large signal bandwidth, 1 V_{pp}, 3 dB BW, 100 pF load					–
	Power = low	300	–	–	kHz	
	Power = high	300	–	–	kHz	

15.17 PSoC Core POR and LVD

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the *PowerPSoC Technical Reference Manual* for more information on the VLT_CR register.

Table 15-31. POR and LVD DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PPOR2}	V_{DD} Value for PPOR Trip PORLEV[1:0] = 10b	–	4.55	4.70	V	–
	V_{DD} Value for LVD Trip					–
V_{LVD6}	VM[2:0] = 110b	4.62	4.73	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.81	4.95	V	

15.18 PSoC Core Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-32. Programming DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDP}	Supply current during programming or verify	–	15	30	mA	–
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	–
V_{IHP}	Input high voltage during programming or verify	2.1	–	–	V	–
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull down resistor.
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	–
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	–
$Flash_{ENPB}$	Flash endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[17]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention[18]	10	–	–	Years	–

Notes
17. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36 x 1 blocks of 50,000 maximum cycles each, 36 x 2 blocks of 25,000 maximum cycles each, or 36 x 4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36 x 50,000 and that no single block ever sees more than 50,000 cycles)
18. Guaranteed for –40 °C ≤ T_A ≤ 85 °C for Industrial rated devices and –40 °C ≤ T_A ≤ 105 °C for Extended Temperature rated devices.

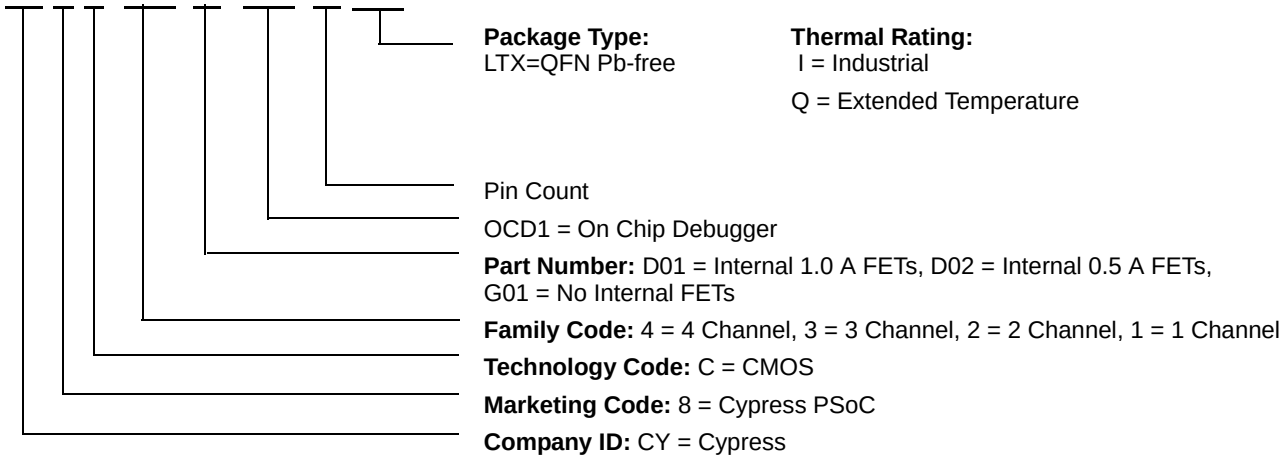
16. Ordering Information

Table 16-1. Device Key Features and Ordering Information

PowerPSoC Part Number	No. of Pins	Package	Channels	Voltage	Internal FETs	Gate Drivers for External Low Side N-FETs
CY8CLED04D01-56LTXI	56 QFN	8 mm × 8 mm	4	32 V	4 × 1.0 A	4
CY8CLED04D02-56LTXI	56 QFN	8 mm × 8 mm	4	32 V	4 × 0.5 A	4
CY8CLED04G01-56LTXI	56 QFN	8 mm × 8 mm	4	32 V	0	4
CY8CLED04DOCD1-56LTXI	56 QFN	8 mm × 8 mm	4	32 V	4 × 1.0 A	4
CY8CLED03D01-56LTXI	56 QFN	8 mm × 8 mm	3	32 V	3 × 1.0 A	3
CY8CLED03D02-56LTXI	56 QFN	8 mm × 8 mm	3	32 V	3 × 0.5 A	3
CY8CLED03G01-56LTXI	56 QFN	8 mm × 8 mm	3	32 V	0	3
CY8CLED02D01-56LTXI	56 QFN	8 mm × 8 mm	2	32 V	2 × 1.0 A	2
CY8CLED01D01-56LTXI	56 QFN	8 mm × 8 mm	1	32 V	1 × 1.0 A	1
CY8CLED01D01-56LTXQ	56 QFN	8 mm × 8 mm	1	32 V	1 × 1.0 A	1

16.1 Ordering Code Definitions

CY 8 C LED0x xxx (xxxx) - xx xxxx



20. Document History Page

Document Title: CY8CLED04D01/CY8CLED04D02/CY8CLED04G01/CY8CLED03D01/CY8CLED03D02/CY8CLED03G01/ CY8CLED02D01/CY8CLED01D01, PowerPSoC® Intelligent LED Driver Document Number: 001-46319				
Revision	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2506500	ANWA/ DSG	05/20/08	New datasheet.
*A	2575708	ANWA/ AESA	10/01/08	1) Updated Logic Block Diagram with AINX label and SREGFB pin. 2) Updated Current Sense Amplifier Specification Table. 3) Updated External Gate Driver Specification Table. 4) Updated Register Table.
*B	2662774	KJV	02/19/09	Extensive changes made to content and electrical specifications.
*C	2665155	KJV/PYRS	02/25/09	Updated Notes in electrical specifications.
*D	2671254	KJV/PYRS	03/10/09	Updated sections 8, 9, and 10 on pages 14, 15, and 16.
*E	2683506	VED	04/03/09	Release to the external web site.
*F	2698529	KJV/PYRS	04/27/09	Updated Figure 15-2., and Figure 15-4..
*G	2735072	KJV	07/10/09	Added 1 and 2 channel part information.
*H	2765369	KJV	09/17/09	Updated electrical specifications.
*I	2870389	FRE/PYRS	02/01/10	Updated Absolute Maximum Ratings, DC GPIO, AC Chip-Level, and AC Programming Specifications as follows: Added $V_{REGINMAX}$ absolute maximum specification. Modified t_{WRITE} specification. Added I_{OH}, I_{OL}, DC_{ILO}, f_{32K_U}, $t_{POWERUP}$, $t_{ERASEALL}$, $t_{PROGRAM\_HOT}$, and $t_{PROGRAM\_COLD}$ specifications Updated package diagram
*J	2952677	FRE/UKK	06/15/10	Datasheet reviewed and updated with a view to improve clarity, readability and customer-friendliness. This includes language, consistency in terminology to match software and other PowerPSoC documentation, changes to reflect major changes in software such as removal of system level design addition of links to relevant collateral such as kits, technical reference manuals and application notes.
*K	3031567	FRE/UKK	09/16/10	Removed DALI in Page 1 and Page 13, and added the DALI note in Page 13. Added a note to Section 15.10 after Table 15-20 on page 38. Updated as per the new Cypress Style and datasheet template.
*L	3073506	KJV	11/08/2010	Updated datasheet to add Extended Temperature rated device CY8CLED01D01-56LTXQ
*M	3178540	KJV	02/28/2011	Updated certain specifications for Extended Temperature rated device
*N	3244595	KJV	05/04/2011	Updated description for Symbol V_{REGIN} and V_{CSP},V_{CSN} in Table 14-1. Updated Figure 15-6.
*O	3355306	KJV	08/29/2011	Replaced Table 16-20 with Table 15-20 in Built-in Switching Regulator
*P	3597060	GULA	04/24/2012	Updated Packaging Information (51-85187 from Rev *E to *F). Completing Sunset Review.
*Q	4374000	SNVN	05/08/2014	Added D1 and updated notes for the other components in Table 15-20. Updated links to reference documents in Current Sense Amplifier, Digital System, and Analog Multiplexer System sections. Added note for F_{IMO24} parameter in Table 15-3. Updated links in Worldwide Sales and Design Support based on the template.
*R	4727870	SNVN	04/16/2015	Updated Electrical Characteristics: Updated Table 15-34 (Updated details in Description column). Updated Packaging Information: spec 51-85187 – Changed revision from *F to *G. Updated Note 23. Completing Sunset Review.

21. Sales, Solutions, and Legal Information

21.1 Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC® Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Community | Forums | Blogs | Video | Training

Technical Support

cypress.com/go/support