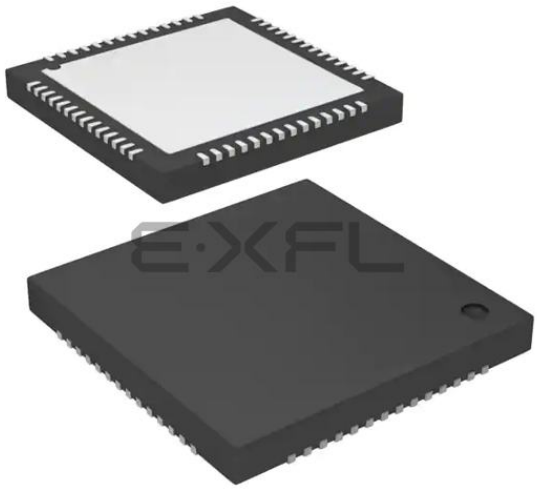

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Intelligent LED Driver
Core Processor	M8C
Program Memory Type	FLASH (16KB)
Controller Series	CY8CLED
RAM Size	1K x 8
Interface	DALI, DMX512, I²C, IrDA, SPI, UART/USART
Number of I/O	14
Voltage - Supply	4.75V ~ 5.25V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad
Supplier Device Package	56-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8cled03d02-56ltxi

3. Logic Block Diagrams

Figure 3-1. CY8CLED04D0x Logic Block Diagram

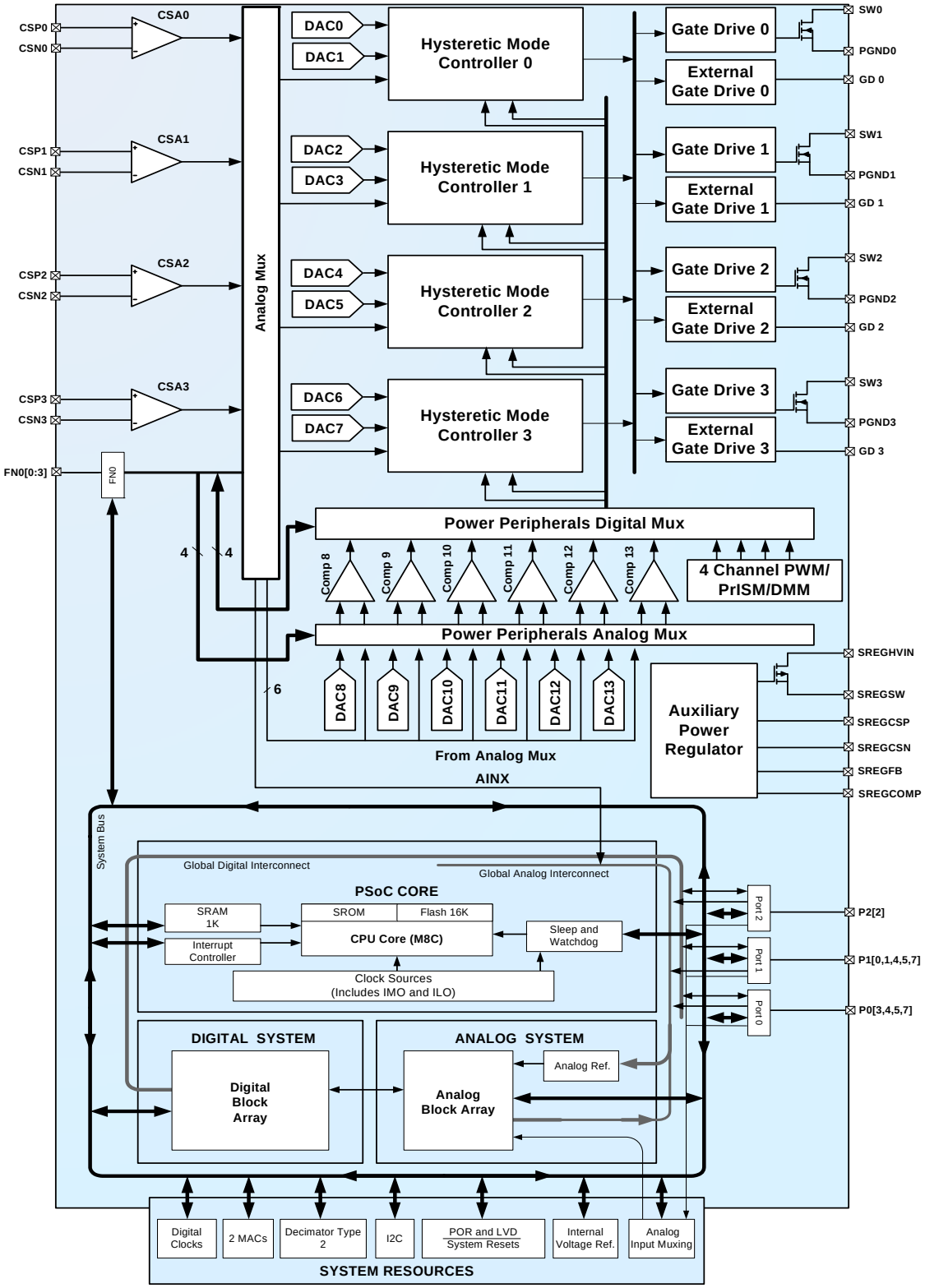
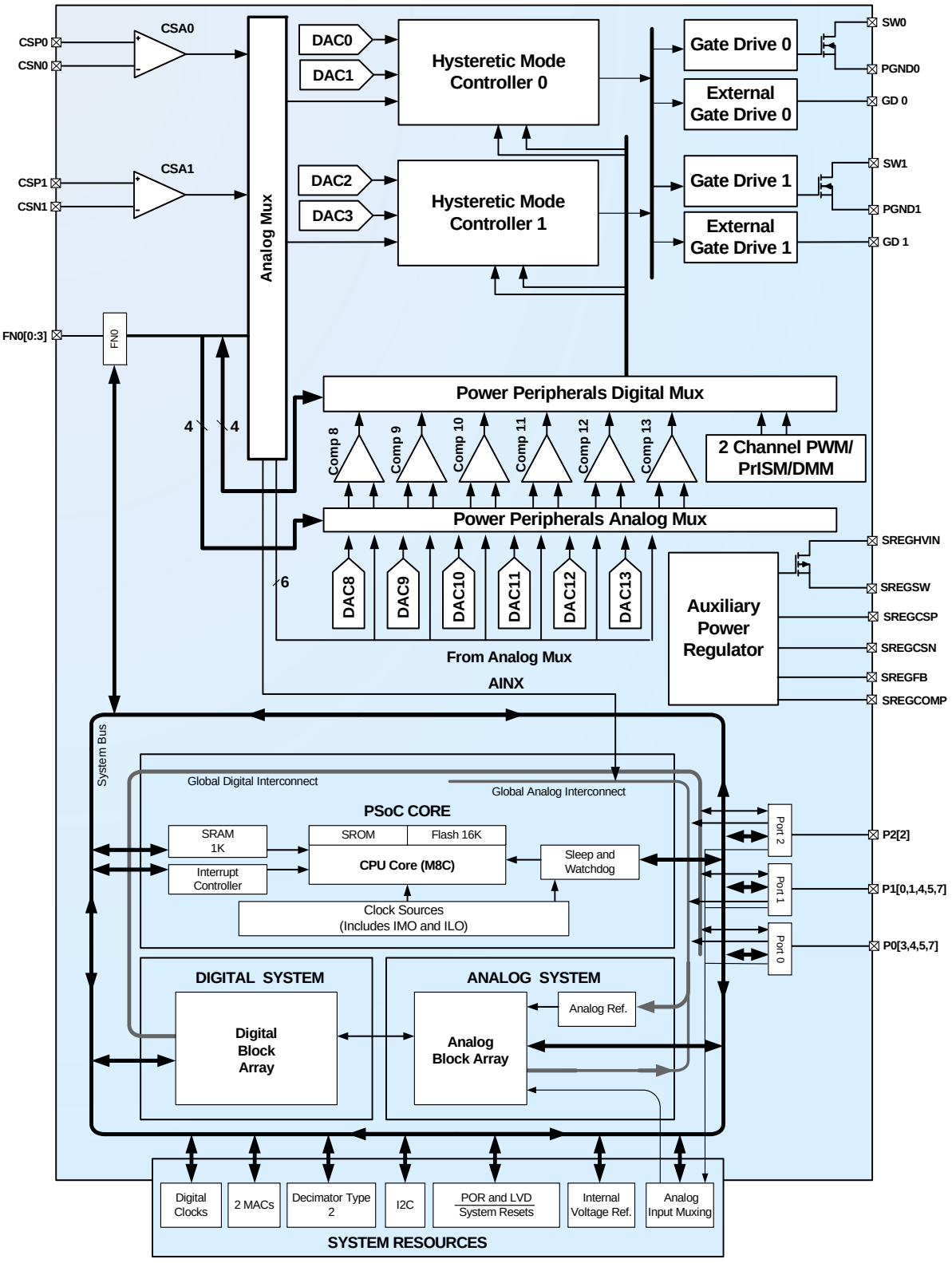


Figure 3-5. CY8CLED02D01 Logic Block Diagram



4. PowerPSoC® Functional Overview

The PowerPSoC family incorporates programmable system-on-chip technology with the best in class power electronics controllers and switching devices to create easy to use power-system-on-chip solutions for lighting applications.

All PowerPSoC family devices are designed to replace traditional MCUs, system ICs, and the numerous discrete components that surround them. PowerPSoC devices feature high performance power electronics including 1 ampere 2 MHz power FETs, hysteretic controllers, current sense amplifiers, and PrISM/PWM modulators to create a complete power electronics solution for LED power management. Configurable power, analog, digital, and interconnect circuitry enables a high level of integration in a host of industrial, commercial, and consumer LED lighting applications.

This architecture integrates programmable analog and digital blocks to enable you to create customized peripheral configurations that match the requirements of each individual application. Additionally, the device includes a 24 MHz CPU, Flash program memory, SRAM data memory, and configurable I/O in a range of convenient pinouts and packages.

The PowerPSoC architecture, as illustrated in the block diagrams, consists of five main areas: PSoC core, digital system, analog system, system resources, and power peripherals, which include power FETs, hysteretic controllers, current sense amplifiers, and PrISM/PWM modulators. Configurable global busing combines all of the device resources into a complete custom system. The PowerPSoC family of devices have 10-port I/Os that connect to the global digital and analog interconnects, providing access to eight digital blocks and six analog blocks.

5. Power Peripherals

PowerPSoC is designed to operate at voltages from 7 V to 32 V, drive up to 1 ampere of current using internal MOSFET switches, and over 1 ampere with external MOSFETs.

This family of devices (CY8CLED0xD/G0y) combines up to four independent channels of constant current drivers. These drivers feature hysteretic controllers with the Programmable System-on-Chip (PSoC) that contains an 8-bit microcontroller, configurable digital and analog peripherals, and embedded flash memory.

The CY8CLED0xD/G0y is the first product in the PowerPSoC family to integrate power peripherals to add further integration for your power electronics applications.The PowerPSoC family of intelligent power controller ICs are used in lighting applications that need traditional MCUs and discrete power electronics support. The power peripherals of the CY8CLED0xD/G0y include up to four 32 volt power MOSFETs with current ratings up to 1 ampere each. It also integrates gate drivers that enable applications to drive external MOSFETs for higher current and voltage capabilities. The controller is a programmable threshold hysteretic controller, with user-selectable feedback paths that uses the IC in current mode floating load buck, floating load buck-boost, and boost configurations.

5.1 Hysteretic Controllers

The PowerPSoC contains four hysteretic controllers. There is one hysteretic controller for each channel of the device.

The hysteretic controllers provide cycle by cycle switch control with fast transient response, which simplifies system design by requiring no external compensation. The hysteretic controllers include the following key features:

- Four independent channels
- DAC configurable thresholds
- Wide switching frequency range from 20 kHz to 2 MHz
- Programmable minimum on and off time
- Floating load buck, floating load buck-boost and boost topology controller

The reference inputs (REF_A and REF_B in Figure 5-1.) of the hysteretic controller are provided by the reference DACs as illustrated in the top level block diagram (see Figure 3-1. on page 3).

The hysteretic control function output is generated by comparing the feedback value to two thresholds. Going below the lower threshold turns the switch ON and exceeding the upper threshold turns the switch OFF as shown in Figure 5-1. The output current waveforms are shown in Figure 5-2.

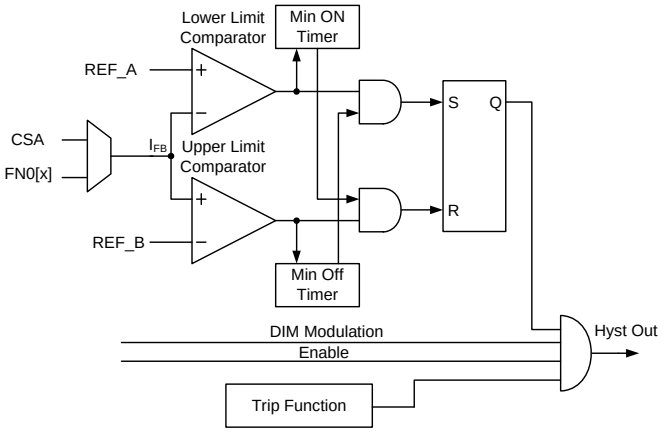
The hysteretic controller also controls the minimum on-time and off-time. This circuit prevents oscillation at very high frequencies; which can be very destructive to output switches.

The output to the gate drivers is gated by the Trip, DIM and Enable signals. The Enable signal is a direct result of the enable bit in the control register for the hysteretic controller.

The Trip signal can be any digital signal that follows TTL logic (logic high and logic low). It is an active high input.

The DIM Modulation signal is the output of the dedicated modulators that are present in the power peripherals, or any other digital modulation signal.

Figure 5-1. Generating Hysteretic Control Function Output



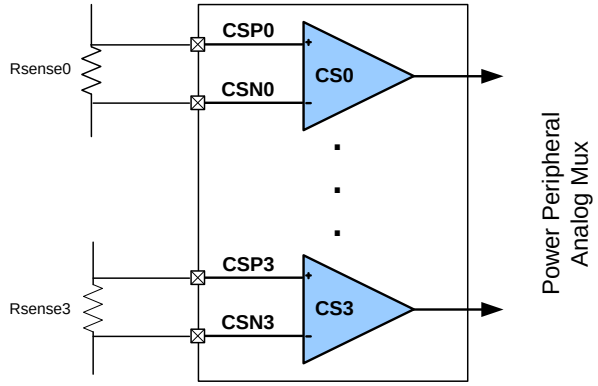
the routing is done. Table 5-1 illustrates example values of R_{sense} for different currents.

The method to calculate the R_{sense} value for a desired average current is explained in the application note CY8CLED0xx0x: Topology and Design Guide for Circuits using PowerPSoC - AN52699

Table 5-1. R_{sense} Values for Different Currents

Max Load Current (mA)	Typical R_{sense} (mΩ)
1000	100
750	130
500	200
350	300

Figure 5-3. High Side Current Measurement



5.6 Voltage Comparators

There are six comparators that provide high speed comparator operation for over voltage, over current, and various other system event detections. For example, the comparators may be used for zero crossing detection for an AC input line or monitoring total DC bus current. Programmable internal analog routing enables these comparators to monitor various analog signals. These comparators include the following key features:

- High speed comparator operation: 100 ns response time
- Programmable interrupt generation
- Low input offset voltage and input bias currents

Six precision voltage comparators are available. The differential positive and negative inputs of the comparators are routed from the analog multiplexer and the output goes to the digital multiplexer. A programmable inverter is used to select the output polarity. User-selectable hysteresis can be enabled or disabled to trade-off noise immunity versus comparator sensitivity.

5.7 Reference DACs

The reference DACs are used to generate set points for various analog modules such as Hysteretic controllers and comparators. The reference DACs include the following key features:

- 8-bit resolution
- Guaranteed monotonic operation
- Low gain errors
- 10 us settling time

These DACs are available to provide programmable references for the various analog and comparator functions and are controlled by memory mapped registers.

DAC[0:7] are embedded in the hysteretic controllers and are required to set the upper and lower thresholds for channel 0 to 3.

DAC [8:13] are connected to the Power Peripherals Analog Multiplexer and provide programmable references to the comparator bank. These are used to set trip points which enable over voltage, over current, and other system event detection.

5.8 Built-in Switching Regulator

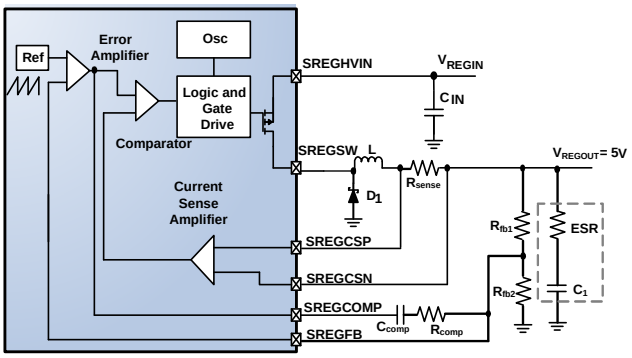
The switching regulator is used to power the low voltage (5 V portion of the PowerPSoC) from the input line. This regulator is based upon a peak current control loop which can support up to 250 mA of output current. The current not being consumed by PowerPSoC is used to power additional system peripherals. The key features of the built-in switching regulator include:

- Ability to self power device from input line
- Small filter component sizes
- Fast response to transients

Refer to Table 15-20 for component values.

The 'Ref' signal that forms the reference to the Error Amplifier is internally generated and there is no user control over it.

Figure 5-4. Built-in Switching Regulator



5.9 Analog Multiplexer

The PowerPSoC family's analog MUX is designed to route signals from the CSA output, function I/O pins and the DACs to comparator inputs and the current sense inputs of the hysteretic controllers. Additionally, CSA outputs can be routed to the AINX block using this MUX.

For a full matrix representation of all possible routing using this MUX, refer to the PowerPSoC Technical Reference Manual.

The CPU configures the Power Peripherals Analog Multiplexer connections using memory mapped registers. The analog multiplexer includes the following key features:

- Signal integrity for minimum signal corruption

5.10 Digital Multiplexer

The PowerPSoC family's digital MUX is a configurable switching matrix that connects the power peripheral digital resources.

For a full matrix representation of all possible routing using this MUX, refer to the PowerPSoC Technical Reference Manual.

This power peripheral digital multiplexer is independent of the main PSoC digital buses or global interconnect of the PSoC core. The digital multiplexer includes the following key features:

- Connect signals to ensure needed flexibility

5.11 Function Pins (FN0[0:3])

The function I/O pins are a set of dedicated control pins used to perform system level functions with the power peripheral blocks of the PowerPSoC. These pins are dynamically configurable, enabling them to perform a multitude of input and output functions. These I/Os have direct access to the input and output of the voltage comparators, input of the hysteretic controller, and output of the digital PWM blocks for the device. The function I/O pins are register mapped. The microcontroller can control and read the state of these pins and the interrupt function.

Some of the key system benefits of the function I/O are:

- Enabling an external higher voltage current-sense amplifier as shown in Figure 5-5.
- Synchronizing dimming of multiple PowerPSoC controllers as shown in Figure 5-6.
- Programmable fail-safe monitor and dedicated shutdown of hysteretic controller as shown in Figure 5-7.

Along with the these functions, these I/Os also provide interrupt functionality, enabling intelligent system responses to power control lighting system status.

Figure 5-5. External CSA and FET Application

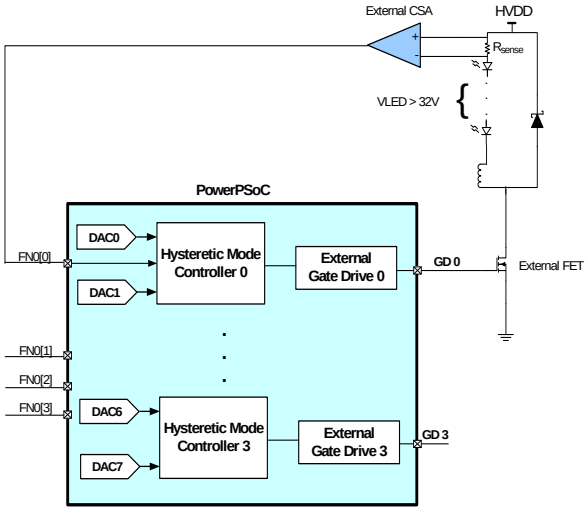


Figure 5-6. PowerPSoC in Master/Slave Configuration

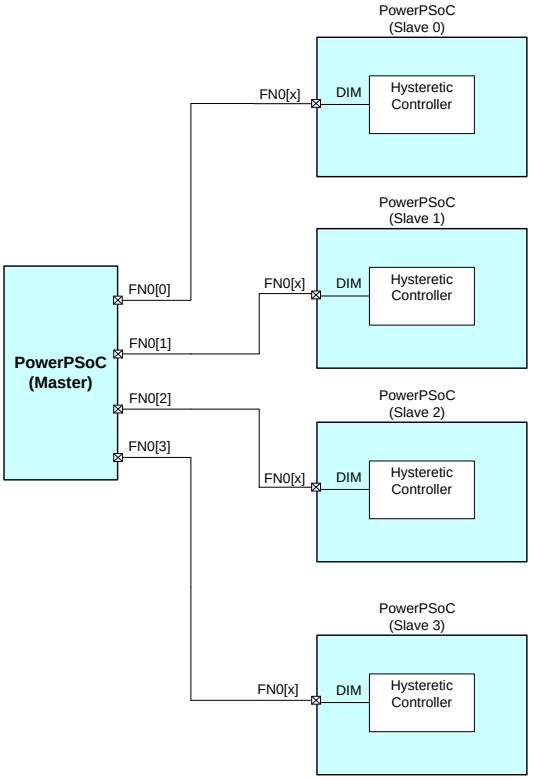
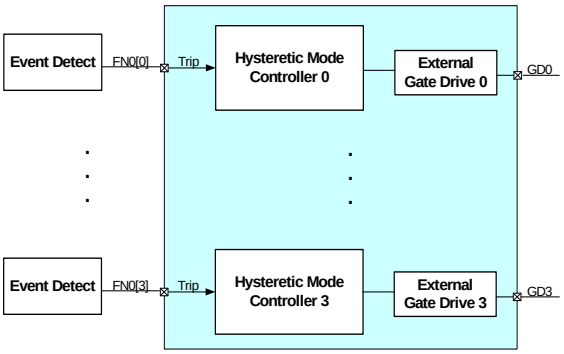


Figure 5-7. Event Detection



6. PSoC Core

The PSoC core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable general purpose I/O(GPIO).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with up to 20 vectors to simplify programming of real time embedded events. The program execution is timed and protected using the included sleep and watchdog timers (WDT) time and protect program execution.

Memory encompasses 16 K of flash for program storage, 1 K of SRAM for data storage, and up to 2 K of EEPROM emulated using the flash. Program flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

The PSoC device incorporates flexible internal clock generators, including a 24 MHz internal main oscillator (IMO) accurate to 4 percent over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz internal low-speed oscillator (ILO) is provided for the sleep timer and WDT. The clocks, together with programmable clock dividers (as a system resource), provide the flexibility to integrate almost any timing requirement into the PowerPSoC device.

PowerPSoC GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

6.1 Digital System

The digital system contains eight digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

Digital peripheral configurations include:

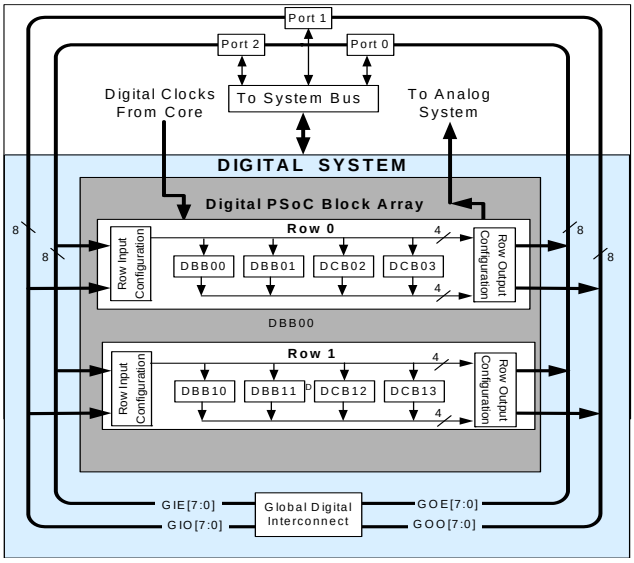
- DMX512
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8-bit with selectable parity
- SPI master and slave
- I^2C master, slave, and multi-master
- Cyclical redundancy checker/generator (8 to 32 bit)
- IrDA
- Pseudo random sequence generators (8 to 32 bit)

Note The DALI interface is supported through the use of a combination of the above mentioned user modules. For more details on the exact configuration and an example project, refer to the application note, PowerPSoC Firmware Design Guidelines, Lighting Control Interfaces - AN51012.

The digital blocks can be connected to any GPIO through a series of global buses that route any signal to any pin. The buses also allow signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

There are four digital blocks in each row. This allows optimum choice of system resources for your application.

Figure 6-1. Digital System Block Diagram



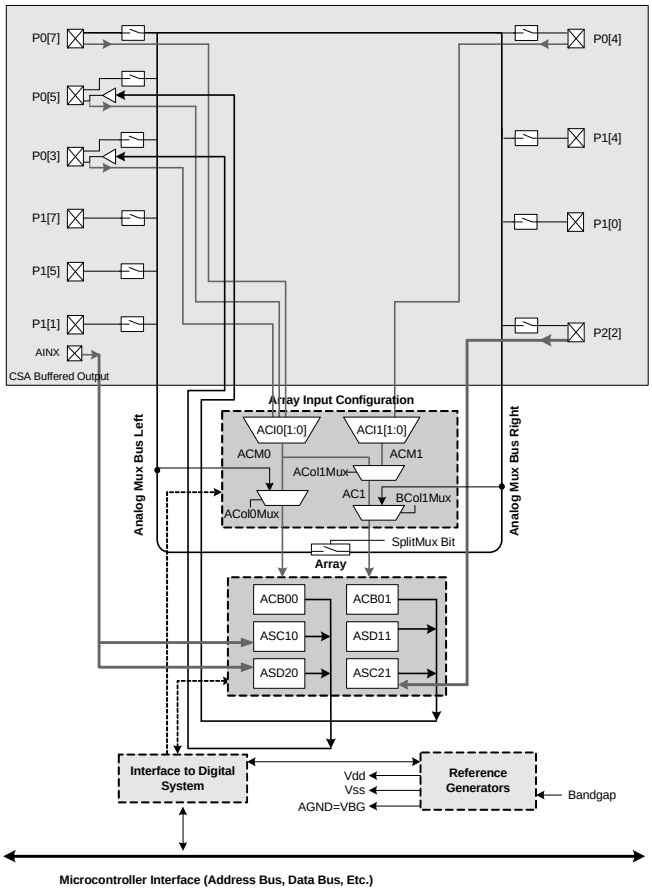
6.2 Analog System

The analog system contains six configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PowerPSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (up to 2, with 6 to 12-bit resolution, selectable as incremental, Delta Sigma, and SAR)
- Filters (2 and 4 pole band-pass, low-pass, and notch)
- Amplifiers (up to 2, with selectable gain to 48x)
- Instrumentation amplifiers (1 with selectable gain to 93x)
- Comparators (up to 2, with 16 selectable thresholds)
- DACs (up to 2, with 6 to 9-bit resolution)
- Multiplying DACs (up to 2, with 6 to 9-bit resolution)
- High current output drivers (two with 30 mA drive as a PSoC core resource)
- 1.3 V reference (as a system resource)
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are arranged in two columns of three blocks each, which includes one continuous time (CT) and two switched capacitor (SC) blocks, as shown in Figure 6-2. on page 14.

Figure 6-2. Analog System Block Diagram



6.3 Analog Multiplexer System

The Analog Mux Bus connects to every GPIO pin in ports 0 to 2. Pins can be connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters. It can be split into two sections for simultaneous dual-channel processing. An additional analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Track pad, finger sensing
- Crosspoint connection between any I/O pin combinations

Like other PSoC devices, PowerPSoC has specific pins allocated to the reference capacitor (Ref Cap) and modulation resistor (Mod resistor). These are indicated in the device pinouts (Section 13). For more details on capacitive sensing, see the design guide, Getting Started With CapSense. Apart from these, there are a number of application notes on Capacitive Sensing on the Cypress webbiest. The PowerPSoC Technical Reference Manual provides details on the analog system configuration that enables all I/Os in the device to be CapSense inputs.

6.4 Additional System Resources

System resources provide additional capability useful in complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power on reset. Brief statements describing the merits of each resource follow.

- Two multiply accumulates (MACs) provide fast 8-bit multipliers with 32-bit accumulate, to assist in both general math and digital filters.
- A decimator provides a custom hardware filter for digital signal processing applications including creation of delta sigma ADCs.
- Low-voltage detection (LVD) interrupts signal the application of falling voltage levels, while the advanced POR (power on reset) circuit eliminates the need for a system supervisor.
- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. The designer can generate additional clocks using digital PSoC blocks as clock dividers.
- The I^2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master applications are supported.
- An internal 1.3 V reference provides an absolute reference for the analog system, including ADCs and DACs.
- Versatile analog multiplexer system.

8. PowerPSoC Device Characteristics

There are two major groups of devices in the PowerPSoC family. One group is a 4-channel 56-pin QFN and the other is a 3-channel 56-pin QFN. These are summarized in the following table.

Table 8-1. PowerPSoC Device Characteristics

Device Group	Internal Power FETs	External Gate Drivers	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8CLED04D01-56LTXI	4X1.0 A	4	14	2	8	14	2	2	6	1 K	16 K
CY8CLED04D02-56LTXI	4X0.5 A	4	14	2	8	14	2	2	6	1 K	16 K
CY8CLED04G01-56LTXI	0	4	14	2	8	14	2	2	6	1 K	16 K
CY8CLED03D01-56LTXI	3X1.0 A	3	14	2	8	14	2	2	6	1 K	16 K
CY8CLED03D02-56LTXI	3X0.5 A	3	14	2	8	14	2	2	6	1 K	16 K
CY8CLED03G01-56LTXI	0	3	14	2	8	14	2	2	6	1 K	16 K
CY8CLED02D01-56LTXI	2X1.0 A	2	14	2	8	14	2	2	6	1 K	16 K
CY8CLED01D01-56LTXI	1X1.0 A	1	14	2	8	14	2	2	6	1 K	16 K
CY8CLED01D01-56LTXQ	1X1.0 A	1	14	2	8	14	2	2	6	1 K	16 K

9. Getting Started

The quickest way to understand the PowerPSoC device is to read this datasheet and then use the PSoC Designer integrated development environment (IDE). This datasheet is an overview of the PowerPSoC integrated circuit and presents specific pin, register, and electrical specifications. For in depth information, along with detailed programming information, refer to the *PowerPSoC Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PowerPSoC device datasheets on the web at www.cypress.com.

9.1 Application Notes

Application notes are an excellent introduction to a wide variety of possible PowerPSoC designs. Layout guidelines, thermal management and firmware design guidelines are some of the topics covered. To view the PowerPSoC application notes, go to htttp://www.cypress.com/powerpsoc and click on the Application Notes link.

9.2 Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store contains development kits, C compilers, and all accessories for PowerPSoC development. For more information on the kits or to purchase a kit from the Cypress web site, go to htttp://www.cypress.com/powerpsoc and click on the Development Kits link.

9.3 Training

Free PowerPSoC technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

9.4 CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PowerPSoC designs. To contact or become a PSoC Consultant go to www.cypress.com/cypros.

9.5 Technical Support

PowerPSoC application engineers take pride in fast and accurate response. They can be reached with a 24-hour guaranteed response at http://www.cypress.com/support/. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

10. Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE runs on Windows XP, Windows Vista, or Windows 7.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built-in support for third-party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PowerPSoC family.

10.1 PSoC Designer Software Subsystems

10.1.1 Chip-Level View

The chip-level view is a more traditional integrated development environment (IDE) based on PSoC Designer. Choose a base device to work with and then select different onboard analog and digital components called user modules that use the PowerPSoC blocks. Examples of user modules are current sense amplifiers, PrISM, PWM, DMM, Floating Load Buck, and Boost. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

10.1.2 Code Generation Tools

PSoC Designer supports multiple third party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to merge seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PowerPSoC family of devices. The products allow you to create complete C programs for the PowerPSoC family of devices.

The optimizing C compilers provide all the features of C tailored to the PowerPSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

10.1.3 Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PowerPSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

10.1.4 Online Help System

The online help system displays online, context-sensitive help for you. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to faqs and an Online Support Forum to aid the designer in getting started.

12.6 CY8CLED02D01 56-Pin Part Pinout (without OCD)

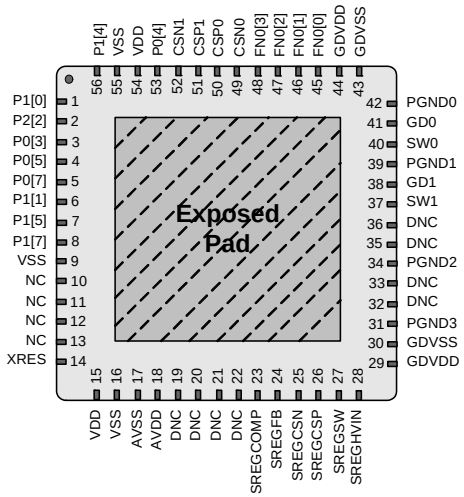
The CY8CLED02D01 PowerPSoC devices are available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-6. CY8CLED02D01 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I2C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCLK (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I2C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I2C SCL (Primary)
9				V_{SS}	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19				DNC[9]	Do Not Connect
20				DNC[9]	Do Not Connect
21				DNC[9]	Do Not Connect
22				DNC[9]	Do Not Connect
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[10]	Power FET Ground 3
32				DNC[9]	Do Not Connect
33				DNC[9]	Do Not Connect
34				PGND2[10]	Power FET Ground 2
35				DNC[9]	Do Not Connect
36				DNC[9]	Do Not Connect
37				SW1	Power Switch 1
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[10]	Power FET Ground 1
40				SW0	Power Switch 0
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[10]	Power FETGround 0
43				GDV_{SS}	Gate Driver Ground

Figure 12-6. CY8CLED02D01 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Notes
9. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
10. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

12.7 CY8CLED01D01 56-Pin Part Pinout (without OCD)

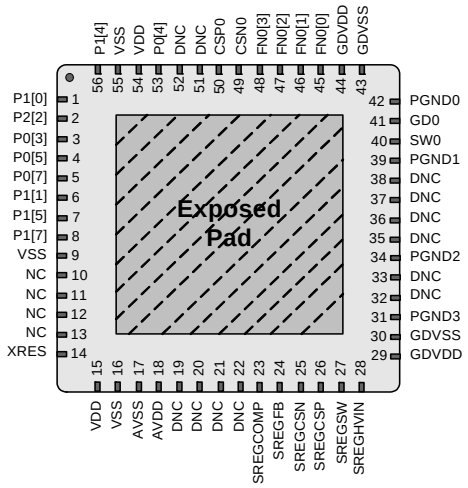
The CY8CLED01D01 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-7. CY8CLED01D01 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I2C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCLK (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I2C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I2C SCL (Primary)
9				V_{SS}	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19				DNC[11]	Do Not Connect
20				DNC[11]	Do Not Connect
21				DNC[11]	Do Not Connect
22				DNC[11]	Do Not Connect
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[12]	Power FET Ground 3
32				DNC[11]	Do Not Connect
33				DNC[11]	Do Not Connect
34				PGND2[12]	Power FET Ground 2
35				DNC[11]	Do Not Connect
36				DNC[11]	Do Not Connect
37				DNC[11]	Do Not Connect
38				DNC[11]	Do Not Connect
39				PGND1[12]	Power FET Ground 1
40				SW0	Power Switch 0
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[12]	Power FET Ground 0
43				GDV_{SS}	Gate Driver Ground

Figure 12-7. CY8CLED01D01 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				DNC[11]	Do Not Connect
52				DNC[11]	Do Not Connect
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Notes
11. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
12. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

14. Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CLED04D0X, CY8CLED04G01, CY8CLED03D0X, CY8CLED03G01, CY8CLED02D01, and CY8CLED01D01 of the PowerPSoC device family. For the most up to date electrical specifications, confirm that you have the most recent datasheet by going to the web at http://www.cypress.com/powerpsoc. Specifications for Industrial rated devices are valid for –40 °C ≤ T_A ≤ 85 °C, T_J ≤ 115 °C and for Extended Temperature rated devices for –40 °C ≤ T_A ≤ 105 °C, T_J ≤ 125 °C, except where noted.

14.1 Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. Not all user guidelines are production tested.

Table 14-1. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	–	+115	°C	Higher storage temperatures reduces data retention time. Recommended storage temperature is 0 °C to 50 °C.
T_A	Ambient temperature with power applied	–40 –40	– –	+85 +105	°C °C	T_J ≤ 115 °C (industrial rated) T_J ≤ 125 °C (extended temperature rated)
V_{DD}, AV_{DD}, GDV_{DD}	Supply voltage on V_{DD}, AV_{DD}, and GDV_{DD}	–0.5	–	+6.0	V	Relative to V_{SS}, AV_{SS}, and GDV_{SS} respectively
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	Applies only to GPIO and FN0 pins
V_{IO2}	DC voltage applied to tristate	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{FET}	Maximum voltage from power Switch (SWx) to Power FET Ground (PGNDx)	–	–	36[13]	V	PGNDx is connected to GDV_{SS}
V_{REGIN}	Maximum voltage on SREGHVIN Pin relative to V_{SS}	–	–	36[13]	V	
V_{CSP},V_{CSN}	Maximum voltage applied to CSA pins relative to V_{SS}	–0.5	–	36[13]	V	
V_{SENSE}	Maximum input differential voltage across CSA input	–1.0	–	1.0	V	
I_{MAIO}	Maximum current into any port pin configured as analog driver	–50	–	+50	mA	
I_{MIO}	Maximum current into any port and function pin	–25	–	+50	mA	
LU	Latch up current	200	–	–	mA	JESD78A Conformal
ESD	Electrostatic discharge voltage	2000	–	–	V	Human Body Model ESD.
SR_{REGIN}	Ramp rate for the SREGHVIN pin	–	–	32	V/µs	
SR_{CSP}	Ramp rate for the CSPx pins	–	–	3.2	V/µs	
$SR_H V_{DD-FLB}$	High voltage supply ramp rate for floating load buck configuration	–	–	15	V/ms	For other topologies, to enable operation with faster ramp rates, or if the LED string voltage is < 6.5 V, see the *PowerPSoC Technical Reference Manual*.
SRV_{DD-EXT}	External V_{DD} supply ramp rate (V_{DD}, AV_{DD}, and GDV_{DD} pins)	–	–	0.2	V/µs	Applies only when powered by a source other than the Built-in Switching Regulator

Note
13. Stresses beyond the "Absolute Maximum Ratings" on page 30 may cause permanent damage to the device. You must ensure that the absolute maximum ratings are NEVER exceeded. Functional operation is not implied under any conditions beyond the "Electrical Characteristics" on page 31 onwards. Extended exposure to "Absolute Maximum Ratings" on page 30 may affect reliability of the device.

14.2 Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	–40 –40	– –	+85 +105	°C °C	$T_J \le 115$ °C (Industrial rated) $T_J \le 125$ °C (extended temperature rated)
T_J	Junction temperature	–40 –40	– –	+115 +125	°C °C	Industrial rated Extended Temperature rated

15. Electrical Characteristics

15.1 System Level

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-1. System Level Operating Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
f_{SW}	Circuit switching frequency range for hysteretic control loop	0.02	–	2	MHz	
$t_{D,MAX}$	Maximum delay time from CSA input to FET state change	– –	– –	100 115	ns ns	HV_{DD} = 24 V, I_D = 1 A, f_{SW} = 2 MHz (Industrial rated) HV_{DD} = 24 V, I_D = 1 A, f_{SW} = 2 MHz (Extended Temperature rated)
D	Output duty cycle for hysteretic controllers	5	–	95	%	f_{SW} < 0.25 MHz
E	Power converter efficiency	90	95	–	%	HV_{DD} = 24 V, I_D = 1 A, f_{SW} = 2 MHz

15.2 Chip Level

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Note See the *PowerPSoC Technical Reference Manual* for more information on the DPWMxPCF register

Table 15-2. Chip Level DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}, AV_{DD}, GDV_{DD}	Digital, analog, and gate driver supply voltage range	4.75	–	5.25	V	All should be powered from the same source.
HV_{DD}	Power converter high voltage supply range	7	–	32	V	
HV_{PINS}	Voltage range for the CSPx and SREGHVIN pins	7	–	32	V	Not all pins need to be at the same voltage level.
IV_{DD}	Supply current (V_{DD} pins), IMO = 24 MHz	–	16	50	mA	Conditions are V_{DD} = 5 V, T_J = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off.
I_AV_{DD}	Supply current (AV_{DD} pin)	–	–	25	mA	Conditions are V_{DD} = 5 V, T_J = 25 °C,

15.3 Power Peripheral Low Side N-Channel FET

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-4. Low Side N-Channel FET DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DS}	Operating drain to source voltage	–	–	32	V	
$V_{DS,INST}$	Instantaneous drain source voltage	–	–	36	V	
I_D	Average drain current	– –	– –	1 0.5	A A	CY8CLED04/3/2/1D01 devices CY8CLED04/3D02 devices
I_{DMAX}	Maximum instantaneous repetitive pulsed current	– –	– –	3 1.5	A A	Less than 33% duty cycle for an average current of 1 A, f_{SW} = 0.1 MHz. CY8CLED04/3/2/1D01 devices Less than 33% duty cycle for an average current of 0.5 A, f_{SW} = 0.1 MHz. CY8CLED04/3D02 devices
$R_{DS(ON)}$	Drain to source ON resistance	– –	– –	0.5 1	Ω Ω	I_D = 1 A, GDV_{DD} = 5 V, T_J = 25 °C CY8CLED04/3/2/1D01 devices I_D = 0.5 A, GDV_{DD} = 5 V, T_J = 25 °C CY8CLED04/3D02 devices
I_{DSS}	Switching node to PGND leakage	– –	– –	10 250	µA µA	T_J = 25 °C T_J = 115 °C (Industrial rated) and T_J = 125 °C (Extended Temperature rated)
I_{SFET}	Supply current per channel - FET (internal gate driver)	–	–	6.25	mA	f_{SW} = 2 MHz

Table 15-5. Low Side N-Channel FET AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_R	Rise time	–	–	20	ns	I_D = 1 A, R_D = 32 Ω
t_F	Fall time	–	–	20	ns	I_D = 1 A, R_D = 32 Ω

Figure 15-2. Low Side N-Channel FET Test Circuit for I_{DSS}, $t_{R, and}$ t_F

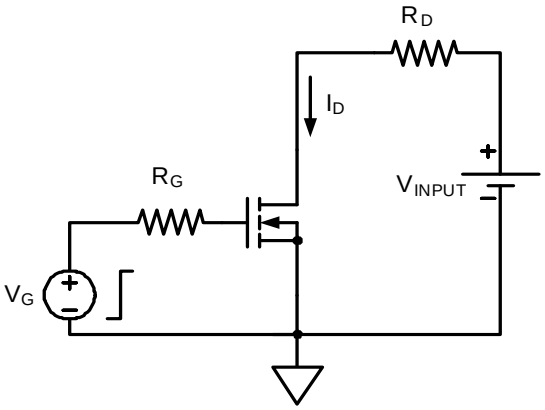


Figure 15-5. Built-in Switching Regulator Timing Diagram

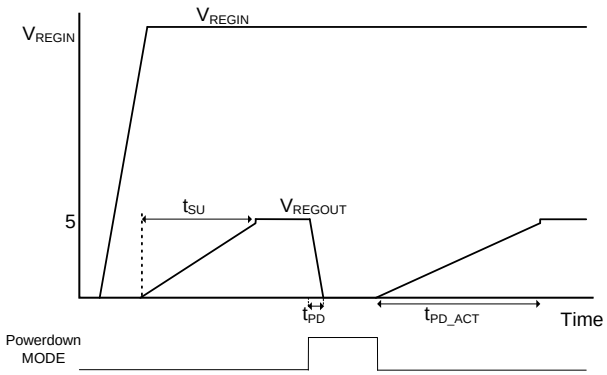
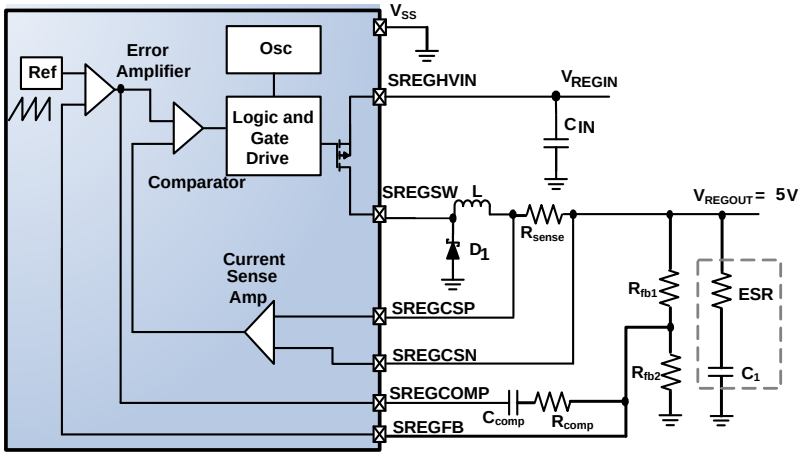


Figure 15-6. Built-in Switching Regulator



15.12 PSoC Core Operational Amplifier Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Capacitor PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block.

Table 15-23. Operational Amplifier DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 – – – – – –	 1.6 1.6 1.3 1.3 1.2 1.2	 10 15 8 13 7.5 12	 mV mV mV mV mV mV	 Industrial rated Extended temperature rated Industrial rated Extended temperature rated Industrial rated Extended temperature rated
TCV_{OSOA}	Average input offset voltage drift	–	7.0	35.0	µV / °C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	T_J = 25 °C.
V_{CMOA}	Common mode voltage range Common mode voltage range (high power or high opamp bias)	0.0 0.5	– –	V_{DD} V_{DD} – 0.5	V V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 60 60 80	 – – –	 – – –	 dB dB dB	–
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.5	 – – –	 – – –	 V V V	–
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	 – – –	 – – –	 0.2 0.2 0.5	 V V V	–
I_{SOA}	Supply current (including associated analog output buffer) Power = low, opamp bias = low Power = low, opamp bias = high Power = medium, opamp bias = low Power = medium, opamp bias = high Power = high, opamp bias = low Power = high, opamp bias = high	 – – – – – –	 400 500 800 1200 2400 4600	 800 900 1000 1600 3200 6400	 µA µA µA µA µA µA	–
$PSRR_{OA}$	Supply voltage rejection ratio	52	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$.

Table 15-28. Analog Output Buffer AC Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
SR_{ROB}	Rising slew rate (20% to 80%), 1 V step, 100 pF load					–
	Power = low	0.65	–	–	V/µs	
	Power = high	0.65	–	–	V/µs	
SR_{FOB}	Falling slew rate (80% to 20%), 1 V step, 100 pF load					–
	Power = low	0.65	–	–	V/µs	
	Power = high	0.65	–	–	V/µs	
BW_{OBSS}	Small signal bandwidth, 20 mV_{pp}, 3 dB BW, 100 pF load					–
	Power = low	0.8	–	–	MHz	
	Power = high	0.8	–	–	MHz	
BW_{OBLS}	Large signal bandwidth, 1 V_{pp}, 3 dB BW, 100 pF load					–
	Power = low	300	–	–	kHz	
	Power = high	300	–	–	kHz	

15.17 PSoC Core POR and LVD

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the *PowerPSoC Technical Reference Manual* for more information on the VLT_CR register.

Table 15-31. POR and LVD DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PPOR2}	V_{DD} Value for PPOR Trip PORLEV[1:0] = 10b	–	4.55	4.70	V	–
	V_{DD} Value for LVD Trip					–
V_{LVD6}	VM[2:0] = 110b	4.62	4.73	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.81	4.95	V	

15.18 PSoC Core Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-32. Programming DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDP}	Supply current during programming or verify	–	15	30	mA	–
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	–
V_{IHP}	Input high voltage during programming or verify	2.1	–	–	V	–
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull down resistor.
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	–
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	–
$Flash_{ENPB}$	Flash endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[17]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention[18]	10	–	–	Years	–

Notes
17. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36 x 1 blocks of 50,000 maximum cycles each, 36 x 2 blocks of 25,000 maximum cycles each, or 36 x 4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36 x 50,000 and that no single block ever sees more than 50,000 cycles)
18. Guaranteed for –40 °C ≤ T_A ≤ 85 °C for Industrial rated devices and –40 °C ≤ T_A ≤ 105 °C for Extended Temperature rated devices.

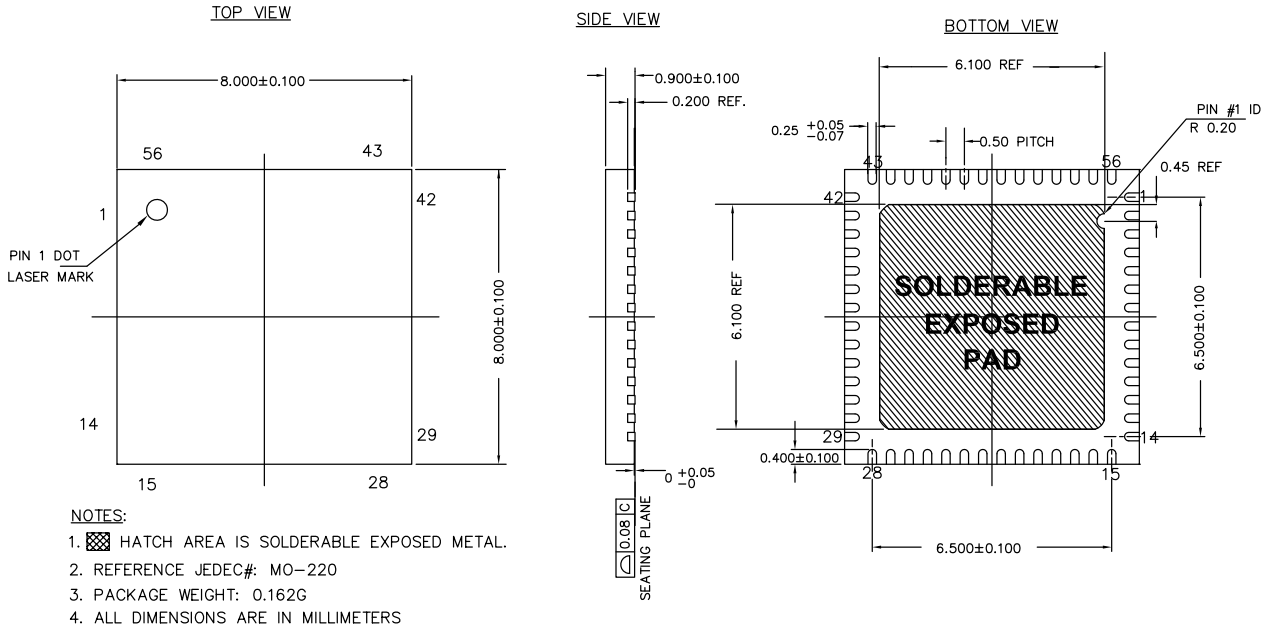
17. Packaging Information

Packaging Dimensions

This section illustrates the package specification for the CY8CLED04D0X, CY8CLED04G01, CY8CLED03D0X, CY8CLED03G01, CY8CLED02D01, and CY8CLED01D01 along with the thermal impedance for the package and solder reflow peak temperatures.

Important Note For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

Figure 17-1. 56-Pin QFN (8 × 8 × 1.0 mm)



51-85187 *G

17.1 Thermal Impedance

Package	Typical θ_{JA} [22]
56 QFN[23]	16.6 °C/W

17.2 Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Package	Minimum Peak Temperature[24]	Maximum Peak Temperature
56 QFN	240 °C	260 °C

Notes

22. $T_J = T_A + POWER \times \theta_{JA}$
23. To achieve the thermal impedance specified for the QFN package, the center thermal pad should be soldered to the PCB ground plane. The thermal model for Cypress's PowerPSoC family was simulated using a JESD51-7 standard FR4 PCB with four metal layers, 2 oz copper weight on outer layers, and 1 oz on inner layers. Thermal via array below the device is laid out according to package manufacturers' recommendations.
24. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

21. Sales, Solutions, and Legal Information

21.1 Worldwide Sales and Design Support

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