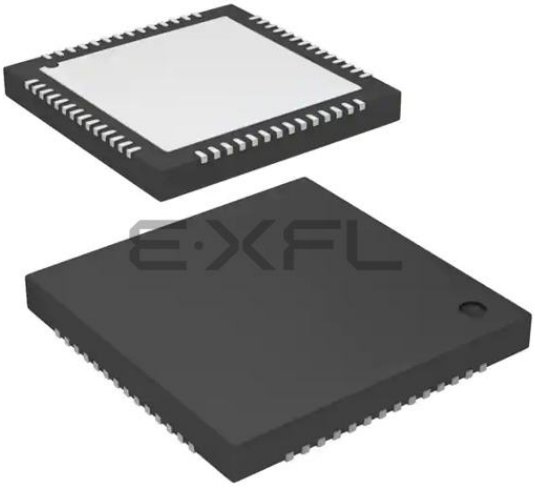

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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Intelligent LED Driver
Core Processor	M8C
Program Memory Type	FLASH (16KB)
Controller Series	CY8CLED
RAM Size	1K x 8
Interface	DALI, DMX512, I²C, IrDA, SPI, UART/USART
Number of I/O	14
Voltage - Supply	4.75V ~ 5.25V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad
Supplier Device Package	56-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8cled03g01-56ltxi

3. Logic Block Diagrams

Figure 3-1. CY8CLED04D0x Logic Block Diagram

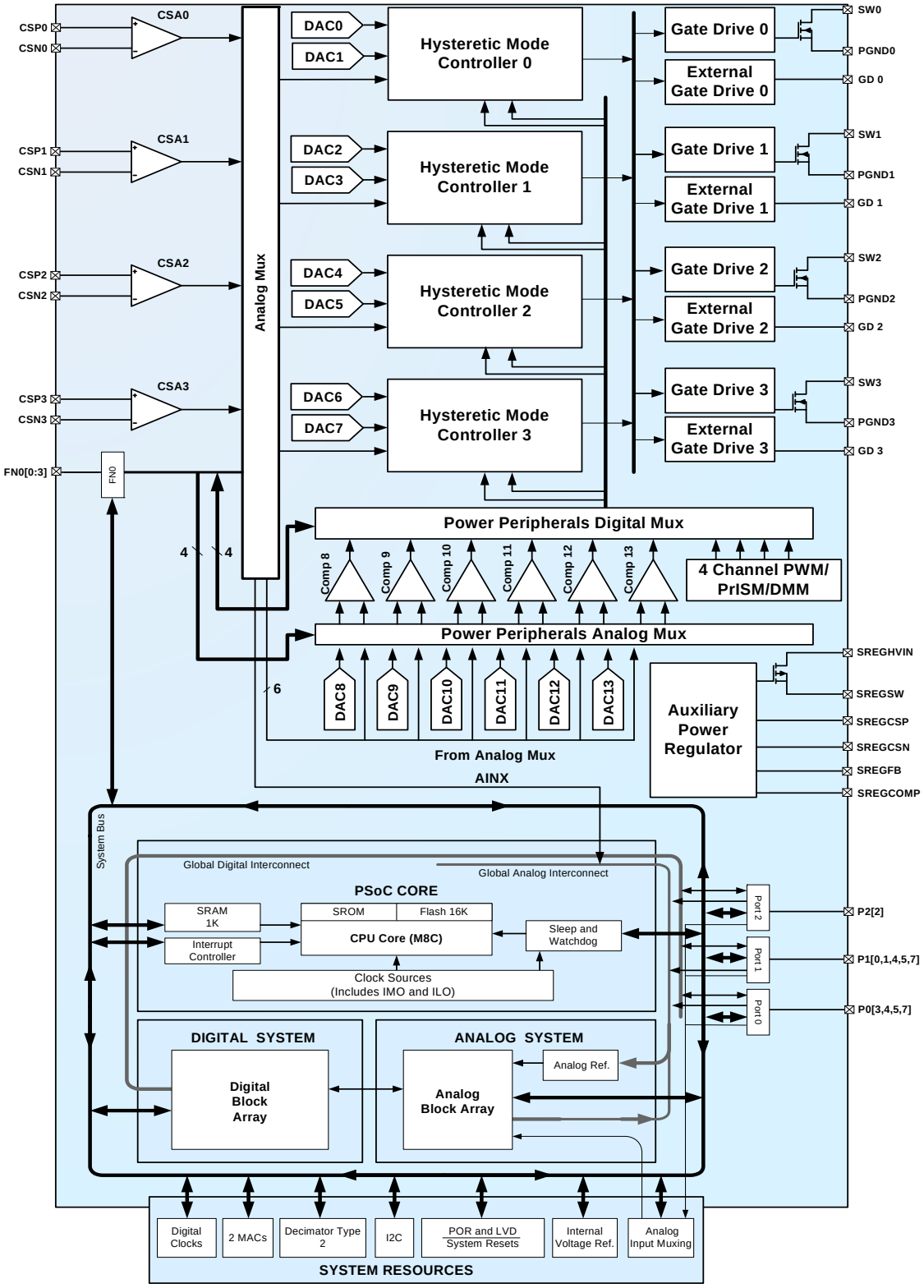


Figure 3-3. CY8CLED03D0x Logic Block Diagram

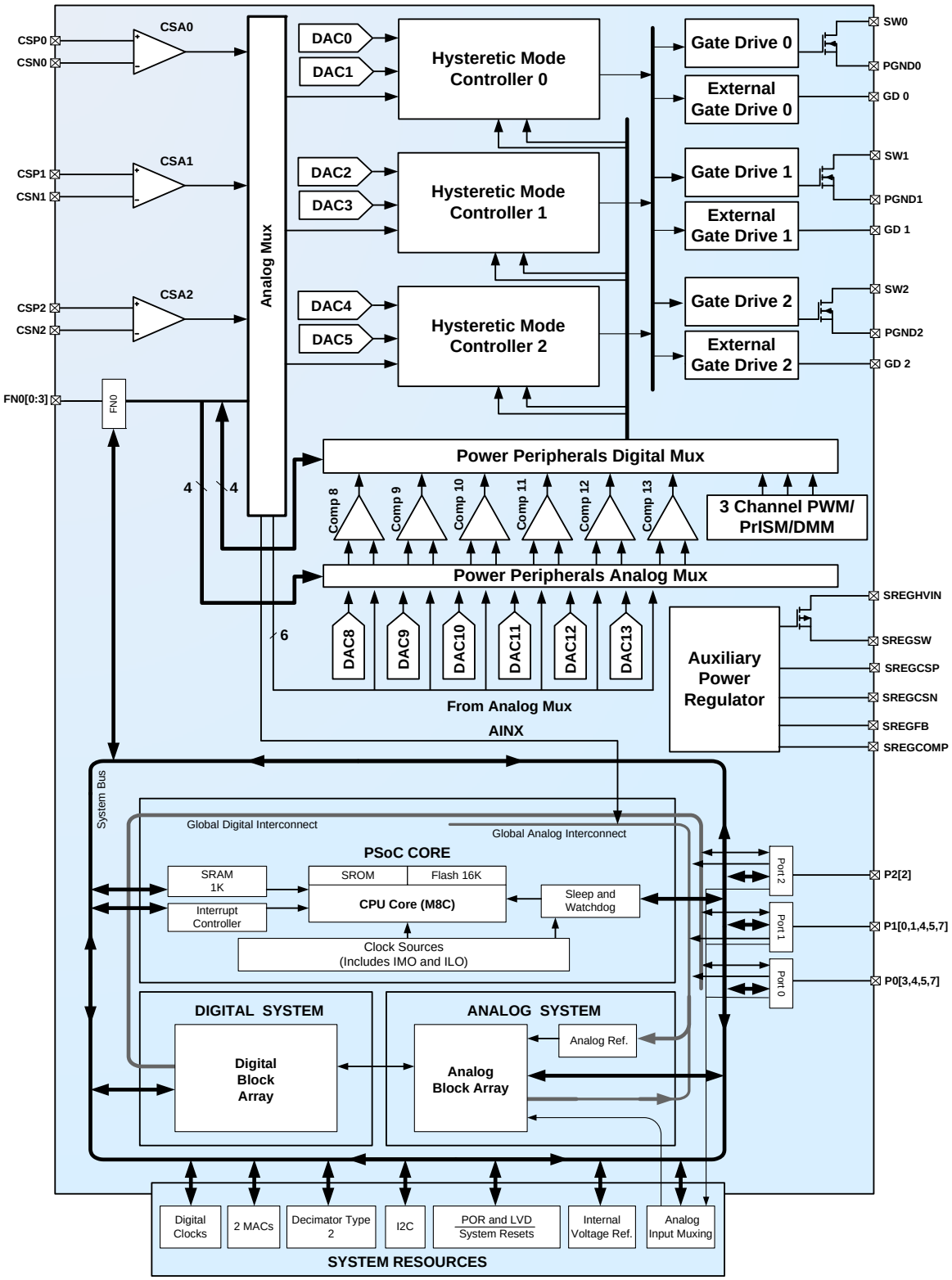


Figure 3-6. CY8CLED01D01 Logic Block Diagram

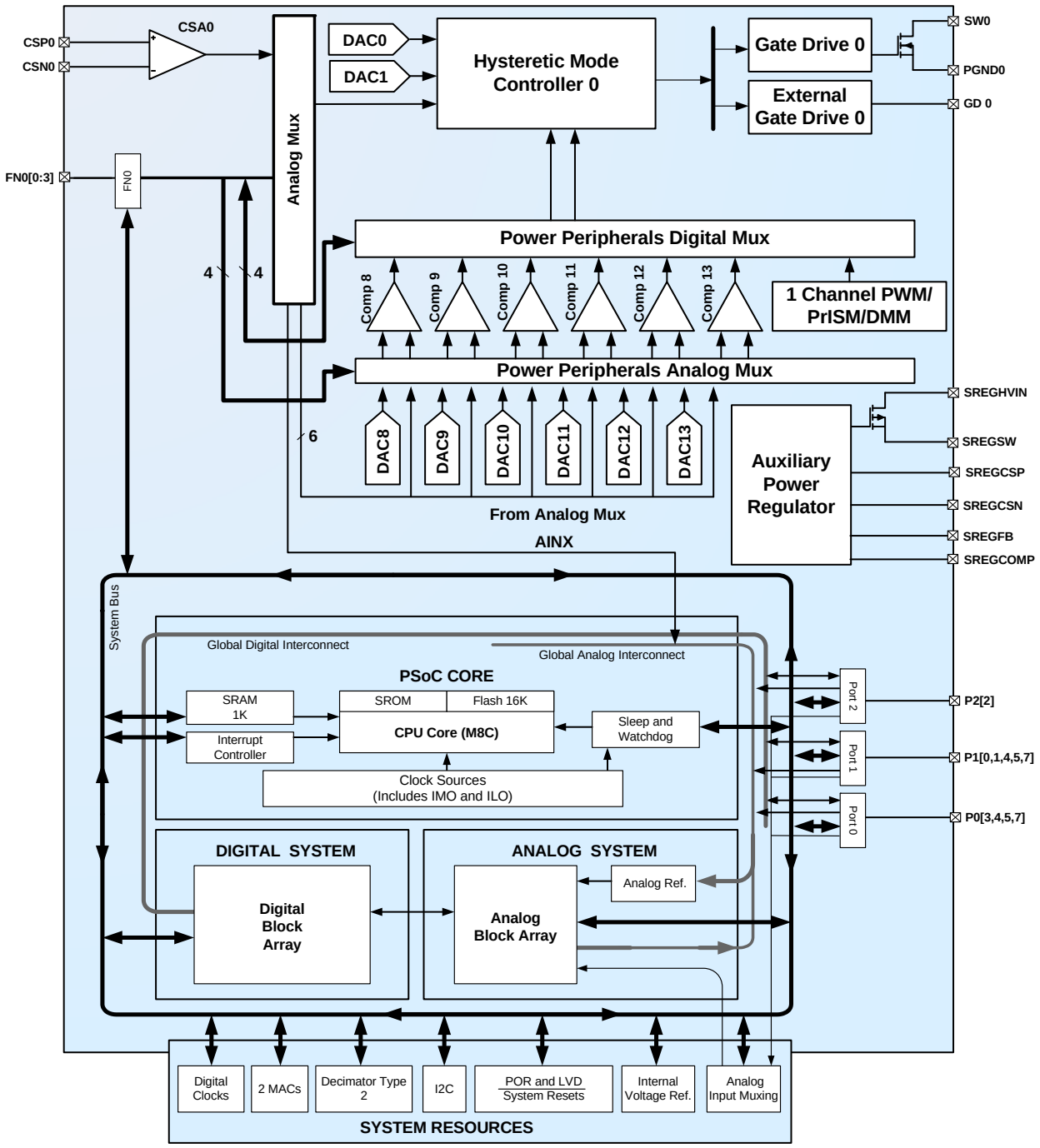
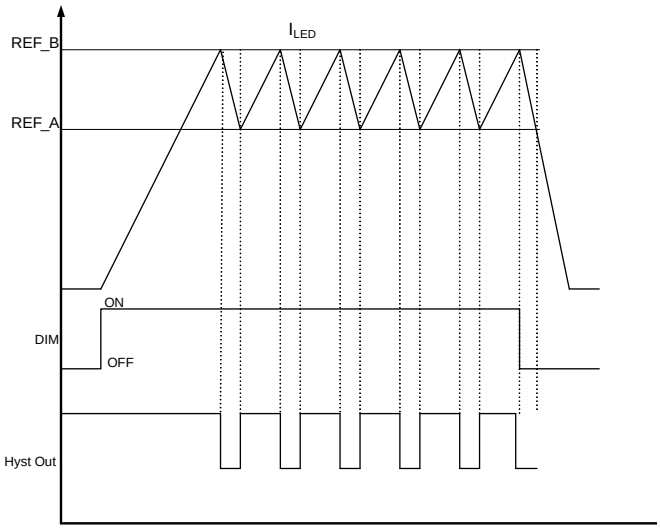


Figure 5-2. Current Waveforms



The minimum on-time and off-time circuits in the PowerPSoC prevent oscillations at very high frequencies, which can be very destructive to output switches.

5.2 Low Side N-Channel FETs

The internal low side N-Channel FETs are designed to enhance system integration. The low side N-Channel FETs include the following key features:

- Drive capability up to 1 A
- Switching times of 20 ns (rise and fall times) to ensure high efficiency (more than 90%)
- Drain source voltage rating 32 V
- Low $R_{DS(ON)}$ to ensure high efficiency
- Switching frequency up to 2 MHz

5.3 External Gate Drivers

These gate drivers enable the use of external FETs with higher current capabilities or lower $R_{DS(ON)}$. The external gate drivers directly drive MOSFETs that are used in switching applications. The gate driver provides multiple programmable drive strength steps to enable improved EMI management. The external gate drivers include the following key features:

- Programmable drive strength options (25%, 50%, 75%, 100%) for EMI management
- Rise and fall times at 55 ns with 4 nF load

5.4 Dimming Modulation Schemes

There are three dimming modulation schemes available with the PowerPSoC. The configurable modulation schemes are:

- Precise intensity signal modulation (PrISM)
- Delta Sigma modulation mode (DMM)
- Pulse-width modulation (PWM)

5.4.1 PrISM Mode Configuration

- High resolution operation up to 16 bits
- Dedicated PrISM module enables customers to use core PSoC digital blocks for other needs
- Clocking up to 48 MHz
- Selectable output signal density
- Reduced EMI

The PrISM mode compares the output of a pseudo-random counter with a signal density value. The comparator output asserts when the count value is less than or equal to the value in the signal density register.

5.4.2 DMM Mode Configuration

- High resolution operation up to 16 bits
- Configurable output frequency and delta sigma modulator width to trade off repeat rates versus resolution
- Dedicated DMM module enables customers to use PSoC digital blocks for other uses
- Clocking up to 48 MHz

The DMM modulator consists of a 12-bit PWM block and a 4-bit delta sigma modulator (DSM) block. The width of the PWM, the width of the DMM, and the clock defines the output frequency. The duty cycle of the PWM output is dithered by using the DSM block which has a user-selectable resolution up to 4 bits.

5.4.3 PWM Mode Configuration

- High resolution operation up to 16 bits
- User programmable period from 1 to 65535 clocks
- Dedicated PWM module enables customers to use core PSoC digital blocks for other use
- Interrupt on rising edge of the output or terminal count
- Precise PWM phase control to manage system current edges
- Phase synchronization among the four channels
- PWM output can be aligned to left, right, or center

The PWM features a down counter and a pulse width register. A comparator output is asserted when the count value is less than or equal to the value in the pulse width register.

5.5 Current Sense Amplifier

The high side current sense amplifiers provide a differential sense capability to sense the voltage across current sense resistors in lighting systems. The current sense amplifier includes the following key features:

- Operation with high common mode voltage to 32 V
- High common mode rejection ratio
- Programmable bandwidth to optimize system noise immunity

An off-chip resistor R_{sense} is used for high side current measurement as shown in Figure 5-3. on page 11. The output of the current sense amplifier goes to the power peripherals analog multiplexer where, you select the hysteretic controller to which

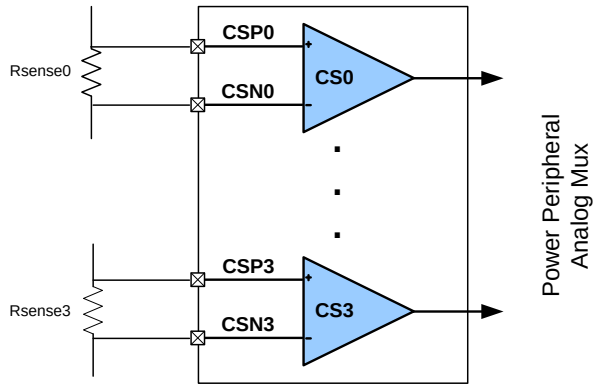
the routing is done. Table 5-1 illustrates example values of R_{sense} for different currents.

The method to calculate the R_{sense} value for a desired average current is explained in the application note CY8CLED0xx0x: Topology and Design Guide for Circuits using PowerPSoC - AN52699

Table 5-1. R_{sense} Values for Different Currents

Max Load Current (mA)	Typical R_{sense} (mΩ)
1000	100
750	130
500	200
350	300

Figure 5-3. High Side Current Measurement



5.6 Voltage Comparators

There are six comparators that provide high speed comparator operation for over voltage, over current, and various other system event detections. For example, the comparators may be used for zero crossing detection for an AC input line or monitoring total DC bus current. Programmable internal analog routing enables these comparators to monitor various analog signals. These comparators include the following key features:

- High speed comparator operation: 100 ns response time
- Programmable interrupt generation
- Low input offset voltage and input bias currents

Six precision voltage comparators are available. The differential positive and negative inputs of the comparators are routed from the analog multiplexer and the output goes to the digital multiplexer. A programmable inverter is used to select the output polarity. User-selectable hysteresis can be enabled or disabled to trade-off noise immunity versus comparator sensitivity.

5.7 Reference DACs

The reference DACs are used to generate set points for various analog modules such as Hysteretic controllers and comparators. The reference DACs include the following key features:

- 8-bit resolution
- Guaranteed monotonic operation
- Low gain errors
- 10 us settling time

These DACs are available to provide programmable references for the various analog and comparator functions and are controlled by memory mapped registers.

DAC[0:7] are embedded in the hysteretic controllers and are required to set the upper and lower thresholds for channel 0 to 3.

DAC [8:13] are connected to the Power Peripherals Analog Multiplexer and provide programmable references to the comparator bank. These are used to set trip points which enable over voltage, over current, and other system event detection.

5.8 Built-in Switching Regulator

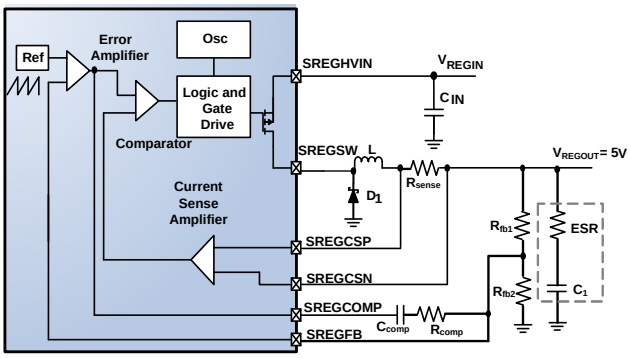
The switching regulator is used to power the low voltage (5 V portion of the PowerPSoC) from the input line. This regulator is based upon a peak current control loop which can support up to 250 mA of output current. The current not being consumed by PowerPSoC is used to power additional system peripherals. The key features of the built-in switching regulator include:

- Ability to self power device from input line
- Small filter component sizes
- Fast response to transients

Refer to Table 15-20 for component values.

The 'Ref' signal that forms the reference to the Error Amplifier is internally generated and there is no user control over it.

Figure 5-4. Built-in Switching Regulator



5.9 Analog Multiplexer

The PowerPSoC family's analog MUX is designed to route signals from the CSA output, function I/O pins and the DACs to comparator inputs and the current sense inputs of the hysteretic controllers. Additionally, CSA outputs can be routed to the AINX block using this MUX.

For a full matrix representation of all possible routing using this MUX, refer to the PowerPSoC Technical Reference Manual.

The CPU configures the Power Peripherals Analog Multiplexer connections using memory mapped registers. The analog multiplexer includes the following key features:

- Signal integrity for minimum signal corruption

5.10 Digital Multiplexer

The PowerPSoC family's digital MUX is a configurable switching matrix that connects the power peripheral digital resources.

For a full matrix representation of all possible routing using this MUX, refer to the PowerPSoC Technical Reference Manual.

This power peripheral digital multiplexer is independent of the main PSoC digital buses or global interconnect of the PSoC core. The digital multiplexer includes the following key features:

- Connect signals to ensure needed flexibility

5.11 Function Pins (FN0[0:3])

The function I/O pins are a set of dedicated control pins used to perform system level functions with the power peripheral blocks of the PowerPSoC. These pins are dynamically configurable, enabling them to perform a multitude of input and output functions. These I/Os have direct access to the input and output of the voltage comparators, input of the hysteretic controller, and output of the digital PWM blocks for the device. The function I/O pins are register mapped. The microcontroller can control and read the state of these pins and the interrupt function.

Some of the key system benefits of the function I/O are:

- Enabling an external higher voltage current-sense amplifier as shown in Figure 5-5.
- Synchronizing dimming of multiple PowerPSoC controllers as shown in Figure 5-6.
- Programmable fail-safe monitor and dedicated shutdown of hysteretic controller as shown in Figure 5-7.

Along with the these functions, these I/Os also provide interrupt functionality, enabling intelligent system responses to power control lighting system status.

Figure 5-5. External CSA and FET Application

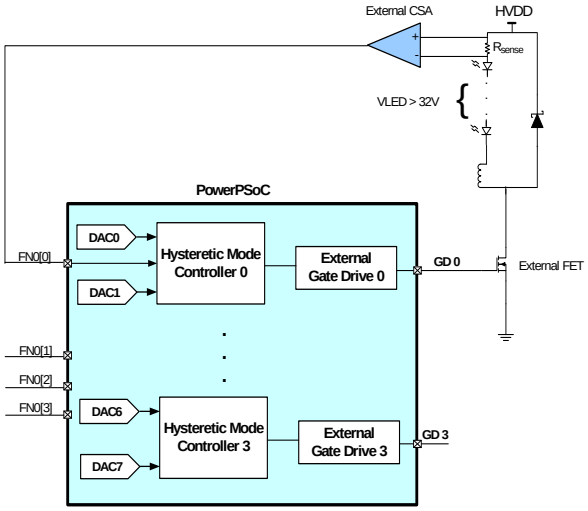


Figure 5-6. PowerPSoC in Master/Slave Configuration

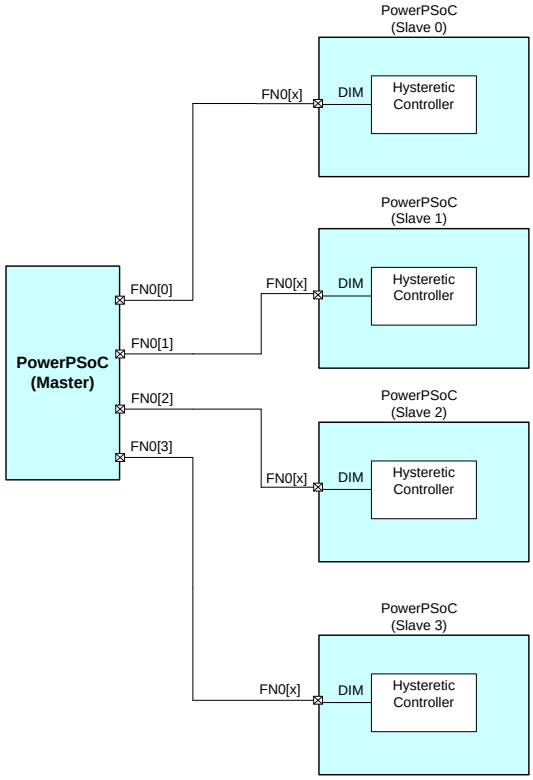


Figure 5-7. Event Detection

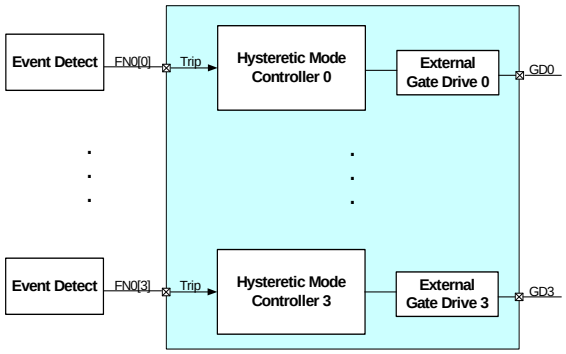


Figure 7-2. LED Lighting with RGBA Color Mixing Driving External MOSFETS as Floating Load Buck Converter

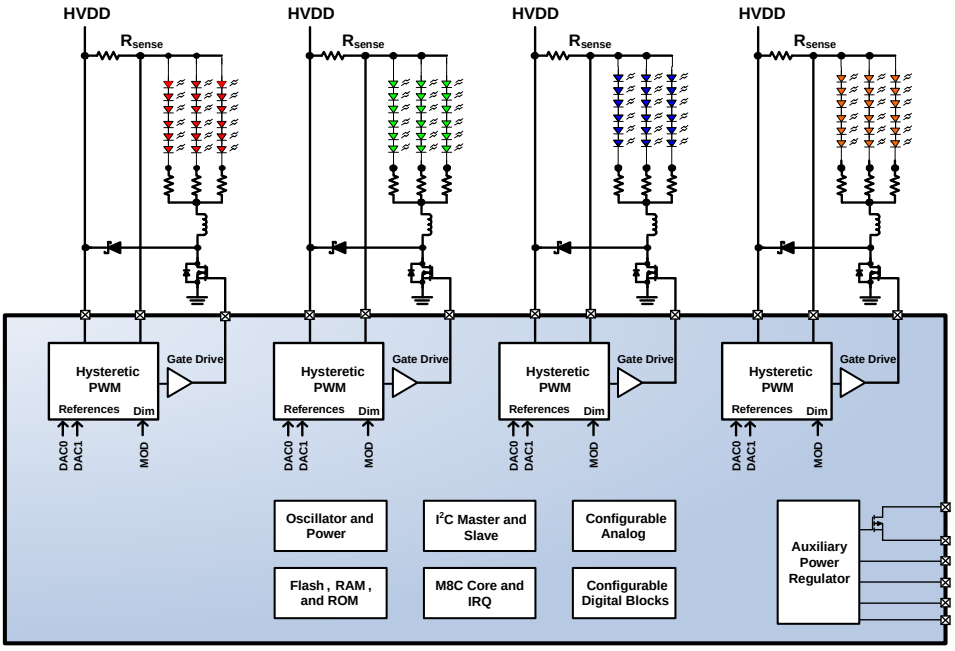
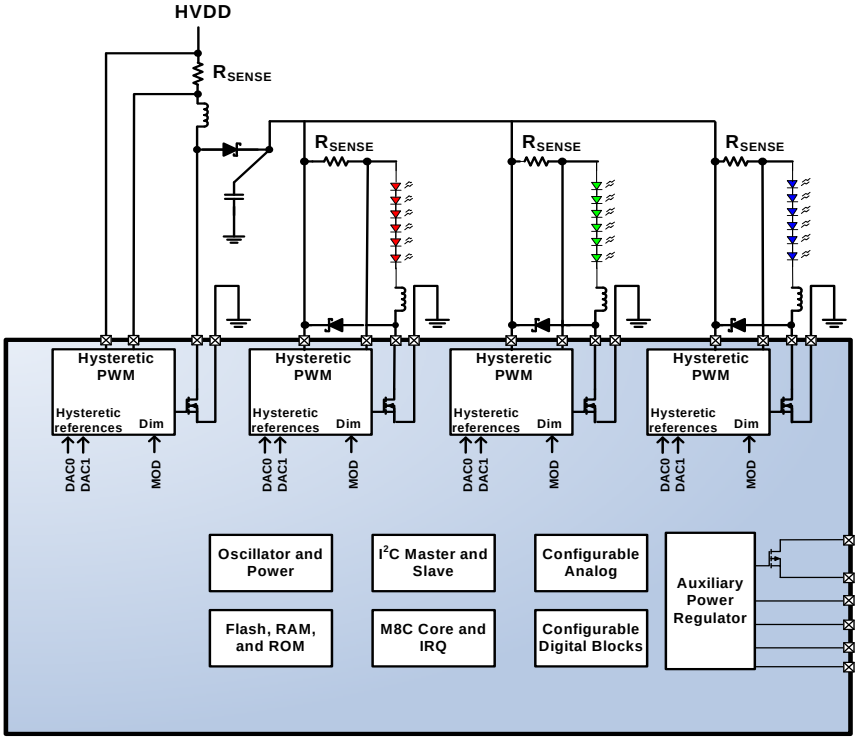


Figure 7-3. LED Lighting with a Single Channel Boost Driving Three Floating Load Buck Channels



12.2 CY8CLED04G01 56-Pin Part Pinout (without OCD)

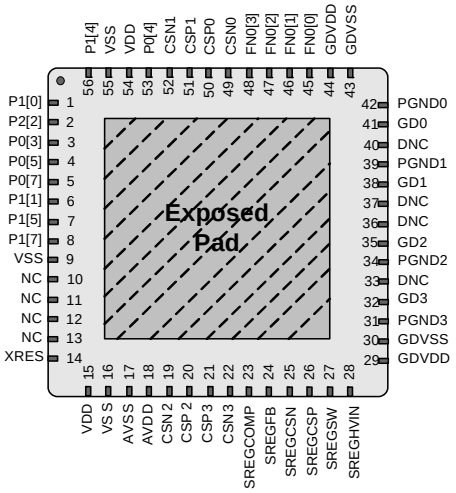
The CY8CLED04G01 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-2. CY8CLED04G01 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I^2C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I^2C SCL (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I^2C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I^2C SCL (Primary)
9				V_{SS}	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19			I	CSN2	Current Sense Negative Input 2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				CSP3	Current Sense Positive Input and Power Supply - CSA3
22			I	CSN3	Current Sense Negative Input 3
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[3]	Power FET Ground 3
32			O	GD3	External Low Side Gate Driver 3
33				DNC[2]	Do Not Connect
34				PGND2[3]	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				DNC[2]	Do Not Connect
37				DNC[2]	Do Not Connect
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[3]	Power FET Ground 1
40				DNC[2]	Do Not Connect
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[3]	Power FET Ground 0
43				GDV_{SS}	Gate Driver Ground

Figure 12-2. CY8CLED04G01 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Notes

2. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
3. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

12.3 CY8CLED04DOCD1 56-Pin Part Pinout (with OCD)

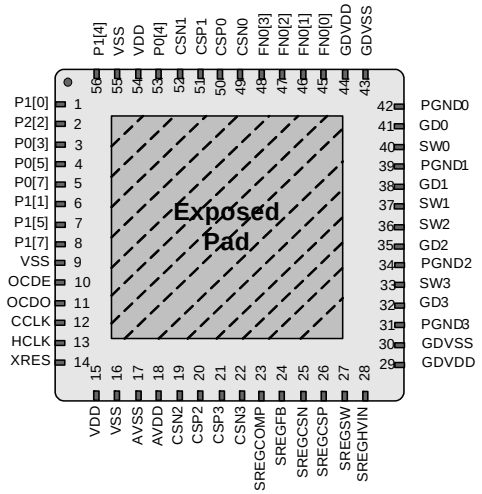
The CY8CLED04DOCD1 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-3. CY8CLED04DOCD1 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I^{2}C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1) / Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I^{2}C SCL (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I^{2}C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I^{2}C SCL (Primary)
9				V_{SS}	Digital Ground
10	I/O			OCDE	On Chip Debugger Port
11	I/O			OCDO	On Chip Debugger Port
12	I/O			CCLK	On Chip Debugger Port
13	I/O			HCLK	On Chip Debugger Port
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19			I	CSN2	Current Sense Negative Input 2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				CSP3	Current Sense Positive Input and Power Supply - CSA3
22			I	CSN3	Current Sense Negative Input 3
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[4]	Power FET Ground 3
32			O	GD3	External Low Side Gate Driver 3
33				SW3	Power Switch 3
34				PGND2[4]	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				SW2	Power Switch 2
37				SW1	Power Switch 1
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[4]	Power FET Ground 1
40				SW0	Power Switch 0
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[4]	Power FET Ground 0
43				GDV_{SS}	Gate Driver Ground

Figure 12-3. CY8CLED04DOCD1 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Note
4. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

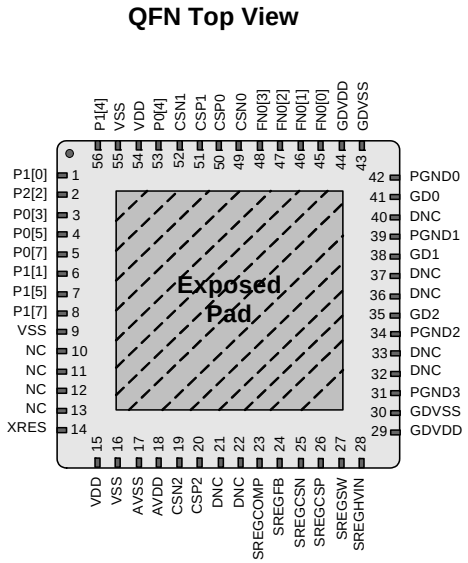
12.5 CY8CLED03G01 56-Pin Part Pinout (without OCD)

The CY8CLED03G01 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-5. CY8CLED03G01 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I^2C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I^2C SCL (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I^2C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I^2C SCL (Primary)
9				V_{SS}	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19			I	CSN2	Current Sense Negative Input 2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				DNC[7]	Do Not Connect
22				DNC[7]	Do Not Connect
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[8]	Power FET Ground 3
32				DNC[7]	Do Not Connect
33				DNC[7]	Do Not Connect
34				PGND2[8]	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				DNC[7]	Do Not Connect
37				DNC[7]	Do Not Connect
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[8]	Power FET Ground 1
40				DNC[7]	Do Not Connect
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[8]	Power FET Ground 0
43				GDV_{SS}	Gate Driver Ground

Figure 12-5. CY8CLED03G01 56-Pin PowerPSoC Device



*** Connect Exposed Pad to PGNDx**

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Notes

7. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
8. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

13.4 Register Map Bank 0 Table

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DPWM0PCF	40	RW	ASC10CR0	80	RW	VDAC0_CR	C0	RW
PRT0IE	01	RW	DPWM0PDH	41	RW	ASC10CR1	81	RW	VDAC0_DR0	C1	RW
PRT0GS	02	RW	DPWM0PDL	42	RW	ASC10CR2	82	RW	VDAC0_DR1	C2	RW
PRT0DM2	03	RW	DPWM0PWH	43	RW	ASC10CR3	83	RW		C3	
PRT1DR	04	RW	DPWM0PWL	44	RW	ASD11CR0	84	RW	VDAC1_CR	C4	RW
PRT1IE	05	RW	DPWM0PCH	45	RW	ASD11CR1	85	RW	VDAC1_DR0	C5	RW
PRT1GS	06	RW	DPWM0PCL	46	RW	ASD11CR2	86	RW	VDAC1_DR1	C6	RW
PRT1DM2	07	RW	DPWM0GCFG	47	RW	ASD11CR3	87	RW		C7	
PRT2DR	08	RW	DPWM1PCF	48	RW		88		VDAC2_CR	C8	RW
PRT2IE	09	RW	DPWM1PDH	49	RW		89		VDAC2_DR0	C9	RW
PRT2GS	0A	RW	DPWM1PDL	4A	RW		8A		VDAC2_DR1	CA	RW
PRT2DM2	0B	RW	DPWM1PWH	4B	RW		8B			CB	
FN0DR	0C	RW	DPWM1PWL	4C	RW		8C		VDAC3_CR	CC	RW
FN0IE	0D	RW	DPWM1PCH	4D	RW		8D		VDAC3_DR0	CD	RW
FN0GS	0E	RW	DPWM1PCL	4E	RW		8E		VDAC3_DR1	CE	RW
FN0DM2	0F	RW	DPWM1GCFG	4F	RW		8F			CF	
	10		DPWM2PCF	50	RW	ASD20CR0	90	RW	CUR_PP	D0	RW
	11		DPWM2PDH	51	RW	ASD20CR1	91	RW	STK_PP	D1	RW
	12		DPWM2PDL	52	RW	ASD20CR2	92	RW		D2	
	13		DPWM2PWH	53	RW	ASD20CR3	93	RW	IDX_PP	D3	RW
	14		DPWM2PWL	54	RW	ASC21CR0	94	RW	MVR_PP	D4	RW
	15		DPWM2PCH	55	RW	ASC21CR1	95	RW	MVW_PP	D5	RW
	16		DPWM2PCL	56	RW	ASC21CR2	96	RW	I2C_CFG	D6	RW
	17		DPWM2GCFG	57	RW	ASC21CR3	97	RW	I2C_SCR	D7	#
PDMUX_S1	18	RW	DPWM3PCF	58	RW		98		I2C_DR	D8	RW
PDMUX_S2	19	RW	DPWM3PDH	59	RW		99		I2C_MSCR	D9	#
PDMUX_S3	1A	RW	DPWM3PDL	5A	RW		9A		INT_CLR0	DA	RW
PDMUX_S4	1B	RW	DPWM3PWH	5B	RW		9B		INT_CLR1	DB	RW
PDMUX_S5	1C	RW	DPWM3PWL	5C	RW	VDAC6_CR	9C	RW	INT_CLR2	DC	RW
PDMUX_S6	1D	RW	DPWM3PCH	5D	RW	VDAC6_DR0	9D	RW	INT_CLR3	DD	RW
	1E		DPWM3PCL	5E	RW	VDAC6_DR1	9E	RW	INT_MSK3	DE	RW
CHBOND_CR	1F	RW	DPWM3GCFG	5F	RW		9F		INT_MSK2	DF	RW
DBB00DR0	20	#	AMX_IN	60	RW	VDAC4_CR	A0	RW	INT_MSK0	E0	RW
DBB00DR1	21	W	AMUX_CFG	61	RW	VDAC4_DR0	A1	RW	INT_MSK1	E1	RW
DBB00DR2	22	RW		62		VDAC4_DR1	A2	RW	INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#	VDAC5_CR	A4	RW	DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#	VDAC5_DR0	A5	RW	DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW	VDAC5_DR1	A6	RW	DEC_CR0	E6	RW
DBB01CR0	27	#	PAMUX_S1	67	RW		A7		DEC_CR1	E7	RW
DCB02DR0	28	#	PAMUX_S2	68	RW	MUL1_X	A8	W	MUL0_X	E8	W
DCB02DR1	29	W	PAMUX_S3	69	RW	MUL1_Y	A9	W	MUL0_Y	E9	W
DCB02DR2	2A	RW	PAMUX_S4	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCB02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBB10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBB10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBB11CR0	37	#	ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12DR0	38	#	DPWM0PCFG	78	RW	RDI1RI	B8	RW		F8	
DCB12DR1	39	W	DPWM1PCFG	79	RW	RDI1SYN	B9	RW		F9	
DCB12DR2	3A	RW	DPWM2PCFG	7A	RW	RDI1IS	BA	RW		FA	
DCB12CR0	3B	#	DPWM3PCFG	7B	RW	RDI1LT0	BB	RW		FB	
DCB13DR0	3C	#	DPWMINTFLG	7C	RW	RDI1LT1	BC	RW		FC	
DCB13DR1	3D	W	DPWMINTMSK	7D	RW	RDI1RO0	BD	RW	DAC_D	FD	RW
DCB13DR2	3E	RW	DPWMSYNC	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCB13CR0	3F	#		7F			BF		CPU_SCR0	FF	#

13.5 Register Map Bank 1 Table: User Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	CSA0_CR	40	RW	ASC10CR0	80	RW	CMPCH0_CR	C0	RW
PRT0DM1	01	RW		41		ASC10CR1	81	RW	CMPCH2_CR	C1	RW
PRT0IC0	02	RW		42		ASC10CR2	82	RW	CMPCH4_CR	C2	RW
PRT0IC1	03	RW		43		ASC10CR3	83	RW	CMPCH6_CR	C3	RW
PRT1DM0	04	RW	CSA1_CR	44	RW	ASD11CR0	84	RW	CMPBNK8_CR	C4	RW
PRT1DM1	05	RW		45		ASD11CR1	85	RW	CMPBNK9_CR	C5	RW
PRT1IC0	06	RW		46		ASD11CR2	86	RW	CMPBNK10_CR	C6	RW
PRT1IC1	07	RW		47		ASD11CR3	87	RW	CMPBNK11_CR	C7	RW
PRT2DM0	08	RW	CSA2_CR	48	RW		88		CMPBNK12_CR	C8	RW
PRT2DM1	09	RW		49			89		CMPBNK13_CR	C9	RW
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
FN0DM0	0C	RW	CSA3_CR	4C	RW		8C			CC	
FN0DM1	0D	RW		4D			8D			CD	
FN0IC0	0E	RW		4E			8E			CE	
FN0IC1	0F	RW		4F			8F			CF	
	10			50		ASD20CR0	90	RW	GDI_O_IN	D0	RW
	11			51		ASD20CR1	91	RW	GDI_E_IN	D1	RW
	12			52		ASD20CR2	92	RW	GDI_O_OU	D2	RW
	13			53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
	14			54		ASC21CR0	94	RW	HYSCTLR0CR	D4	RW
	15			55		ASC21CR1	95	RW	HYSCTLR1CR	D5	RW
	16			56		ASC21CR2	96	RW	HYSCTLR2CR	D6	RW
	17			57		ASC21CR3	97	RW	HYSCTLR3CR	D7	RW
	18			58			98		MUX_CR0	D8	RW
	19			59			99		MUX_CR1	D9	RW
	1A			5A			9A		MUX_CR2	DA	RW
	1B			5B			9B			DB	
	1C			5C			9C		SREG_TST	DC	RW
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW	CMP_GO_EN	64	RW		A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7		DEC_CR2	E7	RW
DCB02FN	28	RW	ALT_CR1	68	RW		A8		IMO_TR	E8	RW
DCB02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	RW
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB			EB	
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBB10FN	30	RW	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10IN	31	RW	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10OU	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11FN	34	RW	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB01IN	35	RW	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB01OU	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCB12IN	39	RW	GDRV0_CR	79	RW	RDI1SYN	B9	RW		F9	
DCB12OU	3A	RW		7A		RDI1IS	BA	RW		FA	
	3B		GDRV1_CR	7B	RW	RDI1LT0	BB	RW		FB	
DCB13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCB13IN	3D	RW	GDRV2_CR	7D	RW	RDI1RO0	BD	RW	DAC_CR	FD	RW
DCB13OU	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
	3F		GDRV3_CR	7F	RW		BF		CPU_SCR0	FF	#

Table 15-9. Hysteretic Controller AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ON} / t_{OFF}	Minimum ON/OFF timer					
	MONOSHOT<1:0> = 00	10	–	30	ns	
	MONOSHOT<1:0> = 01	20	–	60	ns	
	MONOSHOT<1:0> = 10	40	–	110	ns	
	MONOSHOT<1:0> = 11	–	–	–	ns	Timers disabled

15.6 Power Peripheral Comparator

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

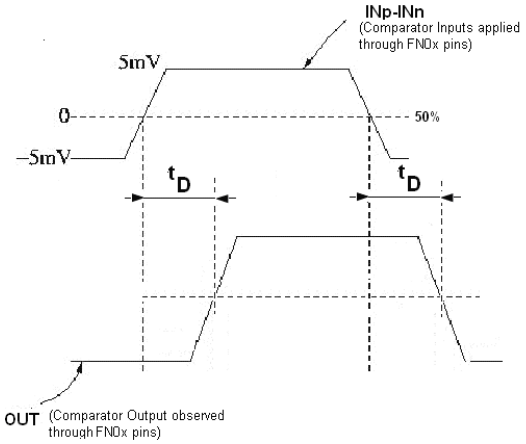
Table 15-10. Comparator DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{IN}	Input voltage range	0	–	V_{DD}	V	–
V_{IO}	Comparator input offset voltage	– – –	– – –	7.5 10 15	mV mV mV	1 V ≤ V_{ICM} ≤ 3 V (Industrial rated) 1 V ≤ V_{ICM} ≤ 3 V (Extended Temperature rated) 0 V ≤ V_{ICM} ≤ V_{DD}
V_{HYS}	Hysteresis voltage	2.5 4.5 4.5	– – –	30 11 13	mV mV mV	0 V < V_{ICM} < V_{DD} 1.5 V ≤ V_{ICM} ≤ 2.5 V (Industrial rated) 1.5 V ≤ V_{ICM} ≤ 2.5 V (Extended Temperature rated)
V_{OVDRV}	Overdrive voltage	5	–	–	mV	–
I_{SCOMP}	Supply current - comparator	–	–	650	µA	–
$V_{ICM,COMP}$	Comparator input common mode voltage range	0	–	V_{DD}	V	–

Table 15-11. Comparator AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_D	Comparator delay time (FN0[x] pin to FN0[x] pin)	–	150	–	ns	V_{OVDRV} = 5 mV, C_L = 10 pF at V_{DD} = 5 V

Figure 15-3. Comparator Timing Diagram



15.7 Power Peripheral Current Sense Amplifier

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to V_{DD} of 5 V and HV_{DD} of 32 V at 25 °C. These are for design guidance only.

Table 15-12. Current Sense Amplifier DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ICM}	Input common mode voltage operating range	7	–	32	V	Either terminal of the amplifier must not exceed this range for functionality
$V_{ICM(Tolerant)}$	Non functional operating range	0	–	32		Absolute maximum rating for V_{SENSE} should never be exceeded. See Absolute Maximum Ratings on page 30
V_{SENSE}	Input differential voltage range	0	–	150	mV	
$I_{S,CSA}$	Supply current - CSA	–	–	1	mA	Enabling CSA causes an incremental draw of 1 mA on the AV_{DD} rail.
I_{BIASP}	Input bias current (+)	–	–	600	µA	
I_{BIASN}	Input bias current (-)	–	–	1	µA	
PSR_{HV}	Power supply rejection (CSP pin)	–	–	–25	dB	f_{SW} < 2 MHz
K	Gain	19.7 19.4	20 20	20.3 20.6	V/V V/V	V_{SENSE} = 50 mV to 130 mV (Industrial rated) V_{SENSE} = 50 mV to 130 mV (Extended Temperature rated)
V_{IOS}	Input offset	–	2	4	mV	V_{SENSE} = 50 mV to 130 mV
C_{IN_CSP}	CSP input capacitance	–	–	5	pF	
C_{IN_CSN}	CSN input capacitance	–	–	2	pF	

Table 15-13. Current Sense Amplifier AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{SETTLE}	Output settling time to 1% of final value	–	–	5	µs	
$t_{POWERUP}$	Power up time to 1% of final value	–	–	5	µs	

Figure 15-4. Current Sense Amplifier Timing Diagram

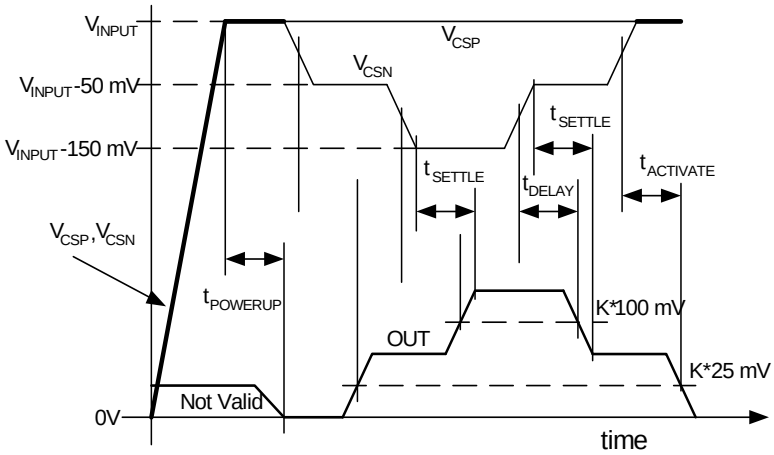


Table 15-18. Built-in Switching Regulator DC Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
$Load_{REG}$	Load regulation	–	1	–	mV	V_{REGIN} = 24 V, I_{LOAD} = 2.5 mA to 250 mA
PSRR	Power supply rejection ratio	–	–60	–	dB	V_{RIPPLE} = 0.2 * V_{REGIN}, f_{RIPPLE} = 1 kHz to 10 kHz
E_{BSR}	Built-in switching regulator efficiency	80	–	–	%	V_{REGIN} = 24 V, I_{LOAD} = 250 mA

Table 15-19. Built-in Switching Regulator AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
f_{SW}	Switching frequency	0.956	1	1.04	MHz	–
t_{RESP}	Response time to within 0.5% of final value	–	10	–	µs	–
t_{SU}	Startup time	–	–	1	ms	–
t_{PD}	Power down time	–	–	100	µs	–
t_{PD_ACT}	Time from power down to active mode	–	–	1	ms	–
t_{ACT_PD}	Time from active mode to power down mode	–	–	50	µs	–
SR_{REGIN}	Ramp rate for the SREGHVIN pin	–	–	32	V/µs	See Absolute Maximum Ratings on page 30

Table 15-20. Built-in Switching Regulator Recommended Components

Component Name	Value	Unit	Notes
R_{fb1}	2	kΩ	Tolerance 1% and 0.05-W rated or better
R_{fb2}	0.698	kΩ	Tolerance 1% and 0.05-W rated or better
C_{comp}	2200	pF	Tolerance 20% and 6.3-V rated or better
R_{comp}	20	kΩ	Tolerance 5% and 0.05-W rated or better
L	47	µH	Tolerance 20% or better, Saturation current rating of 1.5 A or higher
R_{sense}	0.5	Ω	Tolerance 1% and 0.05 W (I_{LOAD} = 0.250 A) rated or better
C_1	10	µF	Ceramic, X7R grade, Minimum ESR of 0.1 Ω, 6.3-V rated
C_{in}	1	µF	Ceramic, X7R grade, 50-V rated (V_{REGIN} = 32 V)
D1	40/0.5	V/A	Schottky diode - Reverse voltage 40 V, average rectified forward current 0.5 A (V_{REGIN} = 32 V)

Note If the built-in switching regulator is not being used in a design, it must be configured as per the following instructions to ensure it is disabled in a safe state.

SREGFB: 5 V

SREGCSN: 5 V

SREGCSP: 5 V

SREGCOMP: Floating

SREGHVIN: ≥ VDD rail

SREGSW: Floating/Tie to SREGHVIN

If the switching regulator is disabled through wiring its input pins (as previously explained) then it must be disabled through software as well (bit SREG_TST[0] = 1), which is set in the Global Resources in the Interconnect View of PSoC Designer.

Figure 15-5. Built-in Switching Regulator Timing Diagram

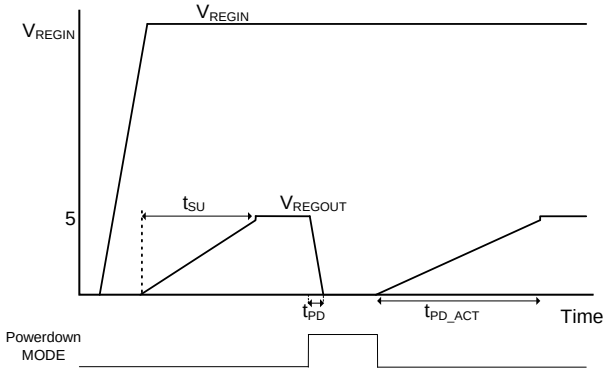
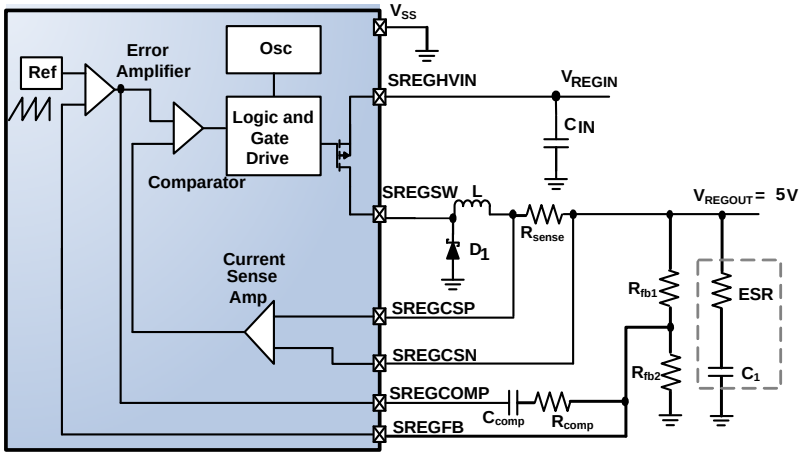


Figure 15-6. Built-in Switching Regulator



15.14 PSoC Core Analog Output Buffer

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-27. Analog Output Buffer DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input offset voltage (absolute value)	– –	3 3	12 18	mV mV	Industrial rated Extended Temperature rated
TCV_{OSOB}	Average input offset voltage drift	–	+6	–	µV/°C	–
V_{CMOB}	Common-mode input voltage range	0.5	–	V_{DD} – 1.0	V	–
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 0.6 0.6	 – –	 Ω Ω	–
$V_{OHIGHOB}$	High output voltage swing (load = 32 ohms to $V_{DD}/2$) Power = low Power = high	0.5 x V_{DD} + 1.1 0.5 x V_{DD} + 1.1	– –	– –	V V	–
V_{OLOWOB}	Low output voltage swing (load = 32 ohms to $V_{DD}/2$) Power = low Power = high	– –	– –	0.5 x V_{DD} – 1.3 0.5 x V_{DD} – 1.3	V V	–
I_{SOB}	Supply current including bias cell (no load) Power = low Power = high	 – –	 1.1 2.6	 5.1 8.8	 mA mA	–
$PSRR_{OB}$	Supply voltage rejection ratio	52	64	–	dB	(0.5 x V_{DD} – 1.3) ≤ V_{OUT} ≤ (V_{DD} – 2.3).

Table 15-28. Analog Output Buffer AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROB}	Rising settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high	 – –	 – –	 2.5 2.5	 µs µs	–
t_{SOB}	Falling settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high	 – –	 – –	 2.2 2.2	 µs µs	–

Table 15-28. Analog Output Buffer AC Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
SR_{ROB}	Rising slew rate (20% to 80%), 1 V step, 100 pF load Power = low Power = high	 0.65 0.65	 – –	 – –	 V/µs V/µs	–
SR_{FOB}	Falling slew rate (80% to 20%), 1 V step, 100 pF load Power = low Power = high	 0.65 0.65	 – –	 – –	 V/µs V/µs	–
BW_{OBSS}	Small signal bandwidth, 20 mV_{pp}, 3 dB BW, 100 pF load Power = low Power = high	 0.8 0.8	 – –	 – –	 MHz MHz	–
BW_{OBLS}	Large signal bandwidth, 1 V_{pp}, 3 dB BW, 100 pF load Power = low Power = high	 300 300	 – –	 – –	 kHz kHz	–

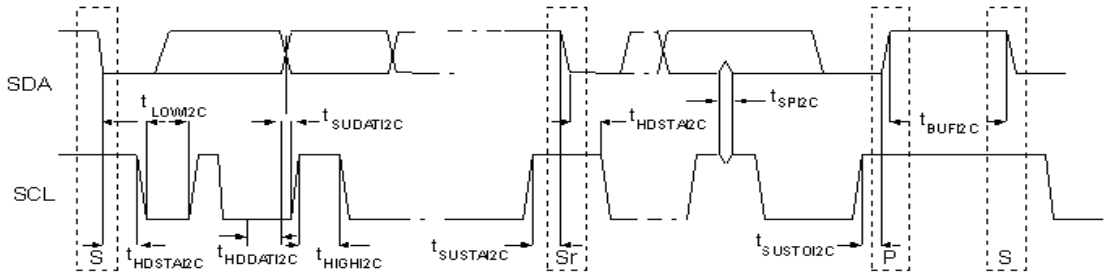
15.20 PSoC Core I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-35. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
f_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz	–
$t_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	–
t_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs	–
$t_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs	–
$t_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs	–
$t_{HDDATI2C}$	Data hold time	0	–	0	–	µs	–
$t_{SUDATI2C}$	Data setup time	250	–	100[21]	–	ns	–
$t_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs	–
t_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs	–
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	0	50	ns	–

Figure 15-8. Definition of Timing for Fast/Standard Mode on the I²C Bus



Note

21. A fast mode I²C bus device can be used in a standard mode I²C bus system, but the requirement $t_{SUDATI2} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line trmax + $t_{SUDATI2}$ = 1000 + 250 = 1250 ns (according to the standard mode I²C bus specification) before the SCL line is released.

18. Acronyms

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CSA	current sense amplifier
CT	continuous time
DAC	digital-to-analog converter
DALI	digital addressable lighting interface
DC	direct current
DMM	delta sigma modulation mode
DMX	digital multiplexing
DSM	delta sigma modulator
DTMF	dual-tone multi frequency
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
FAQ	frequently asked questions
FET	field effect transistor
FSR	full scale range
GPIO	general purpose i/o
GUI	graphical user interface
HBM	human body model
IC	integrated circuit
ICE	in-circuit emulator
IDE	integrated development environment
ILO	internal low-speed oscillator
IMO	internal main oscillator
ISSP	in-system serial programming
I/O	input/output
IPOR	imprecise power on reset
LED	light emitting diode
LSB	least-significant bit
LVD	low voltage detect
MCU	microcontroller
MOSFET	metal-oxide-semiconductor field effect transistor
MSB	most-significant bit
OCD	on chip debugger
PC	program counter
POR	power on reset
PPOR	precision power on reset
PowerPSoC	power programmable system-on-chip™
PrISM	precise intensity signal modulation
PSoC	programmable system-on-chip™
PWM	pulse width modulator
QFN	quad flat no leads package
RGBA	red, green, blue, amber
RGGB	red, green, green, blue
SAR	successive approximation register
SC	switched capacitor
SCL	serial I^2C
SCLK	serial issp clock
SDA	serial i^2c data
SDATA	serial issp data
SPI	serial peripheral interface
SRAM	static random access memory
TRM	technical reference manual
UART	universal asynchronous receiver/transmitter
USB	universal serial bus
WDT	watch dog timer

19. Document Conventions

19.1 Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibels
Hz	Hertz
pp	peak-to-peak
σ	sigma:one standard deviation
V	volt
Ω	ohm
KB	1024 bytes
ppm	parts per million
sps	samples per second
W	watt
A	ampere
Kbit	1024 bits
KHz	kilohertz
KΩ	kilohm
MHz	megahertz
MΩ	megaohm
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µVrms	microvolts root-mean-square