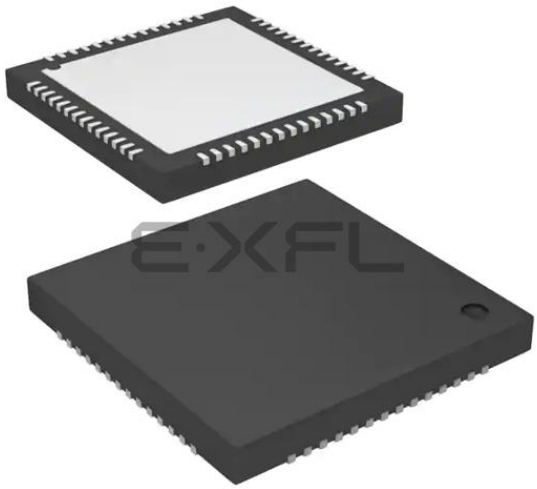

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Intelligent LED Driver
Core Processor	M8C
Program Memory Type	FLASH (16KB)
Controller Series	CY8CLED
RAM Size	1K x 8
Interface	DALI, DMX512, I²C, IrDA, SPI, UART/USART
Number of I/O	14
Voltage - Supply	4.75V ~ 5.25V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad
Supplier Device Package	56-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8cled04d01-56ltxi

2. Contents

Figure 3-2. CY8CLED04G01 Logic Block Diagram

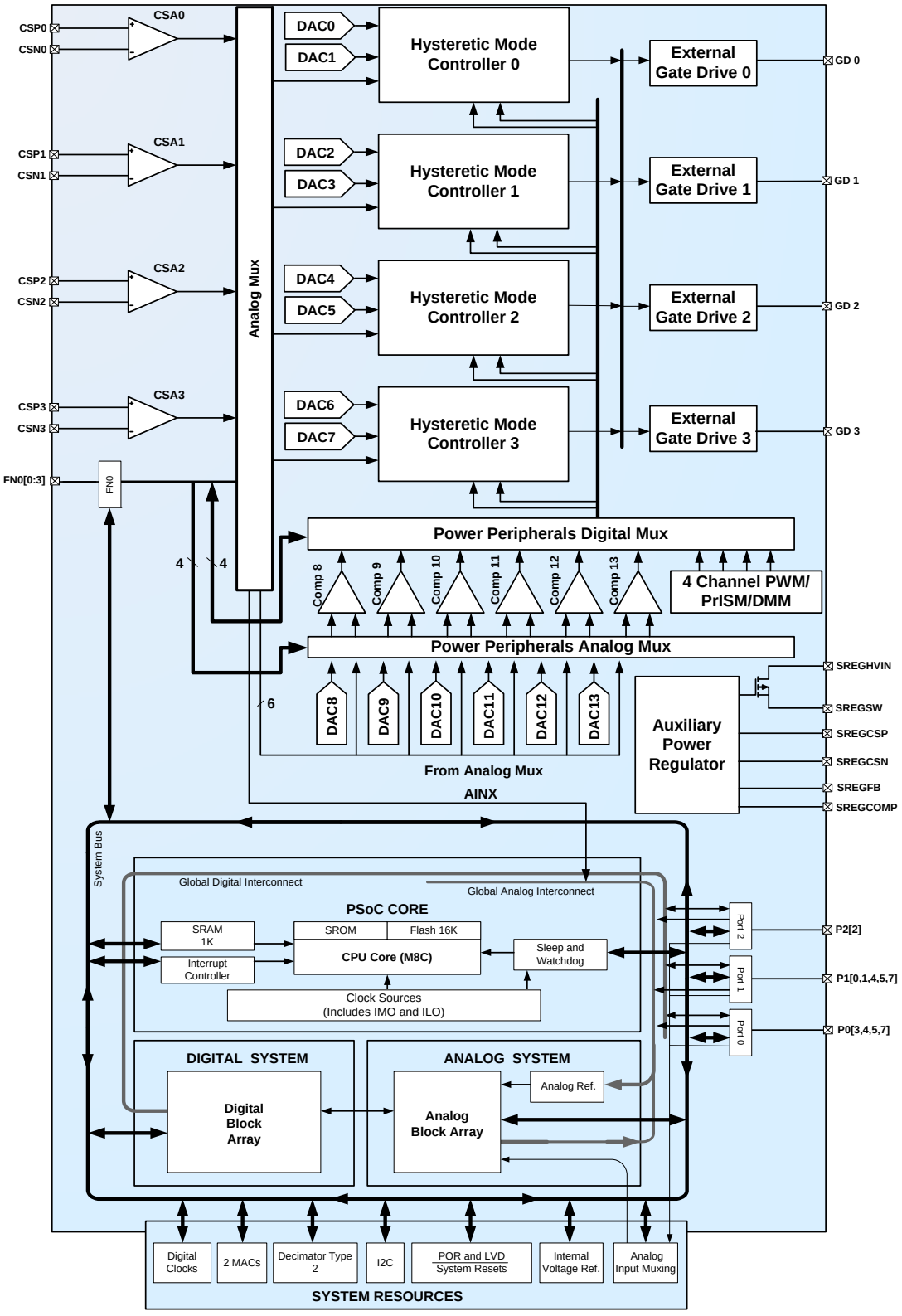


Figure 3-6. CY8CLED01D01 Logic Block Diagram

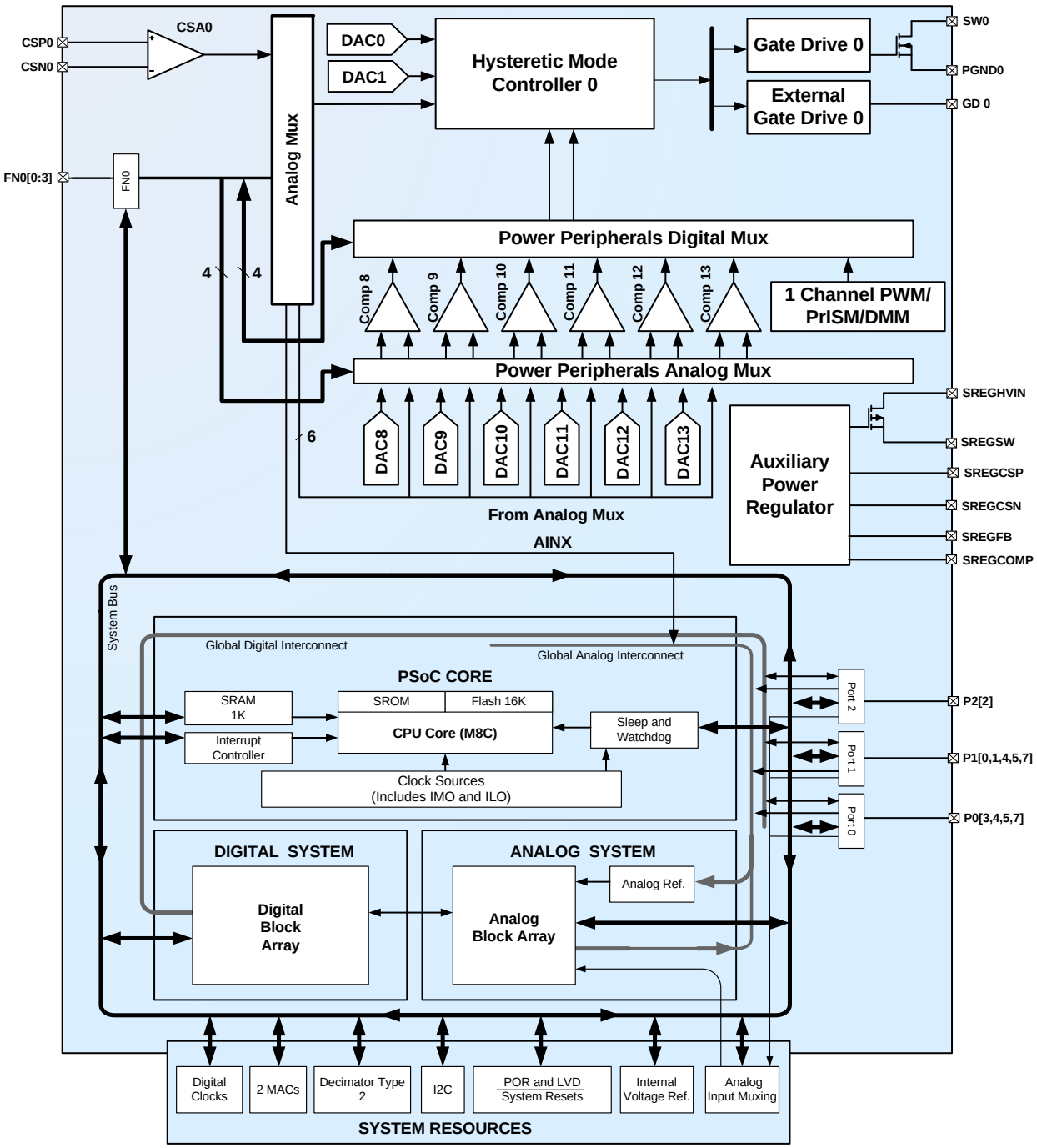
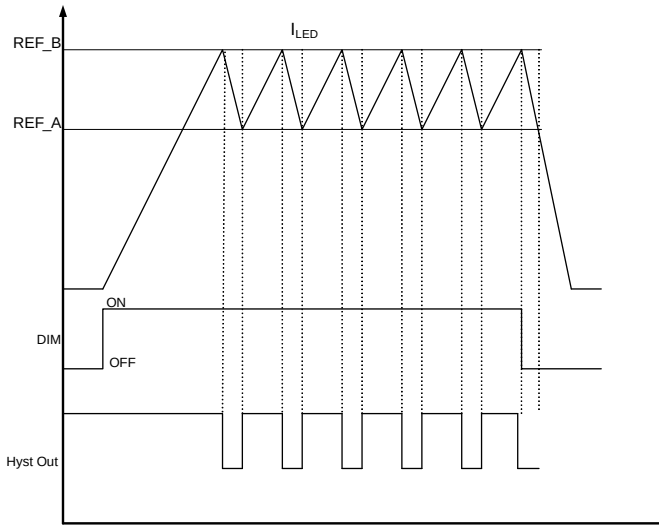


Figure 5-2. Current Waveforms



The minimum on-time and off-time circuits in the PowerPSoC prevent oscillations at very high frequencies, which can be very destructive to output switches.

5.2 Low Side N-Channel FETs

The internal low side N-Channel FETs are designed to enhance system integration. The low side N-Channel FETs include the following key features:

- Drive capability up to 1 A
- Switching times of 20 ns (rise and fall times) to ensure high efficiency (more than 90%)
- Drain source voltage rating 32 V
- Low $R_{DS(ON)}$ to ensure high efficiency
- Switching frequency up to 2 MHz

5.3 External Gate Drivers

These gate drivers enable the use of external FETs with higher current capabilities or lower $R_{DS(ON)}$. The external gate drivers directly drive MOSFETs that are used in switching applications. The gate driver provides multiple programmable drive strength steps to enable improved EMI management. The external gate drivers include the following key features:

- Programmable drive strength options (25%, 50%, 75%, 100%) for EMI management
- Rise and fall times at 55 ns with 4 nF load

5.4 Dimming Modulation Schemes

There are three dimming modulation schemes available with the PowerPSoC. The configurable modulation schemes are:

- Precise intensity signal modulation (PrISM)
- Delta Sigma modulation mode (DMM)
- Pulse-width modulation (PWM)

5.4.1 PrISM Mode Configuration

- High resolution operation up to 16 bits
- Dedicated PrISM module enables customers to use core PSoC digital blocks for other needs
- Clocking up to 48 MHz
- Selectable output signal density
- Reduced EMI

The PrISM mode compares the output of a pseudo-random counter with a signal density value. The comparator output asserts when the count value is less than or equal to the value in the signal density register.

5.4.2 DMM Mode Configuration

- High resolution operation up to 16 bits
- Configurable output frequency and delta sigma modulator width to trade off repeat rates versus resolution
- Dedicated DMM module enables customers to use PSoC digital blocks for other uses
- Clocking up to 48 MHz

The DMM modulator consists of a 12-bit PWM block and a 4-bit delta sigma modulator (DSM) block. The width of the PWM, the width of the DMM, and the clock defines the output frequency. The duty cycle of the PWM output is dithered by using the DSM block which has a user-selectable resolution up to 4 bits.

5.4.3 PWM Mode Configuration

- High resolution operation up to 16 bits
- User programmable period from 1 to 65535 clocks
- Dedicated PWM module enables customers to use core PSoC digital blocks for other use
- Interrupt on rising edge of the output or terminal count
- Precise PWM phase control to manage system current edges
- Phase synchronization among the four channels
- PWM output can be aligned to left, right, or center

The PWM features a down counter and a pulse width register. A comparator output is asserted when the count value is less than or equal to the value in the pulse width register.

5.5 Current Sense Amplifier

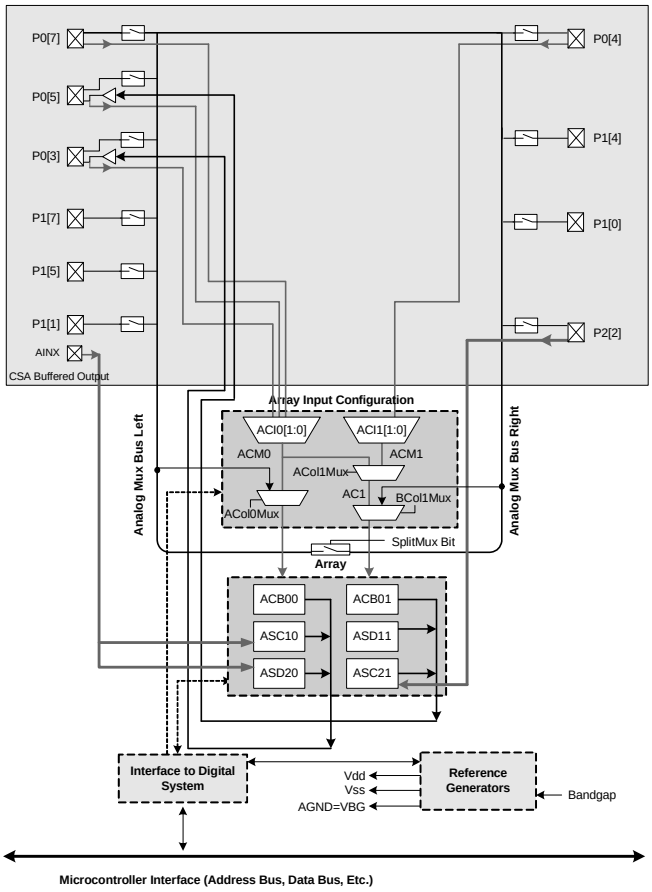
The high side current sense amplifiers provide a differential sense capability to sense the voltage across current sense resistors in lighting systems. The current sense amplifier includes the following key features:

- Operation with high common mode voltage to 32 V
- High common mode rejection ratio
- Programmable bandwidth to optimize system noise immunity

An off-chip resistor R_{sense} is used for high side current measurement as shown in Figure 5-3. on page 11. The output of the current sense amplifier goes to the power peripherals analog multiplexer where, you select the hysteretic controller to which

Analog blocks are arranged in two columns of three blocks each, which includes one continuous time (CT) and two switched capacitor (SC) blocks, as shown in Figure 6-2. on page 14.

Figure 6-2. Analog System Block Diagram



6.3 Analog Multiplexer System

The Analog Mux Bus connects to every GPIO pin in ports 0 to 2. Pins can be connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters. It can be split into two sections for simultaneous dual-channel processing. An additional analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Track pad, finger sensing
- Crosspoint connection between any I/O pin combinations

Like other PSoC devices, PowerPSoC has specific pins allocated to the reference capacitor (Ref Cap) and modulation resistor (Mod resistor). These are indicated in the device pinouts (Section 13). For more details on capacitive sensing, see the design guide, Getting Started With CapSense. Apart from these, there are a number of application notes on Capacitive Sensing on the Cypress webbiest. The PowerPSoC Technical Reference Manual provides details on the analog system configuration that enables all I/Os in the device to be CapSense inputs.

6.4 Additional System Resources

System resources provide additional capability useful in complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power on reset. Brief statements describing the merits of each resource follow.

- Two multiply accumulates (MACs) provide fast 8-bit multipliers with 32-bit accumulate, to assist in both general math and digital filters.
- A decimator provides a custom hardware filter for digital signal processing applications including creation of delta sigma ADCs.
- Low-voltage detection (LVD) interrupts signal the application of falling voltage levels, while the advanced POR (power on reset) circuit eliminates the need for a system supervisor.
- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. The designer can generate additional clocks using digital PSoC blocks as clock dividers.
- The I^2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master applications are supported.
- An internal 1.3 V reference provides an absolute reference for the analog system, including ADCs and DACs.
- Versatile analog multiplexer system.

12. Pin Information

12.1 CY8CLED04D0x 56-Pin Part Pinout (without OCD)

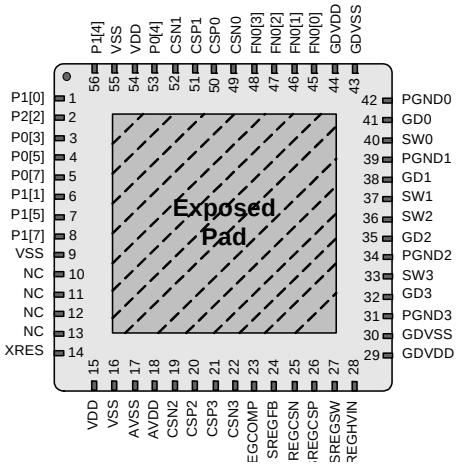
The CY8CLED04D01 and CY8CLED04D02 PowerPSoC devices are available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-1. CY8CLED04D0x 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I^{2}C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I^{2}C SCL (Secondary)/ISSP SCLK
7	I/O	I		P1[5]	GPIO/I^{2}C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I^{2}C SCL (Primary)
9				V_{SS}	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19			I	CSN2	Current Sense Negative Input - CSA2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				CSP3	Current Sense Positive Input and Power Supply - CSA3
22			I	CSN3	Current Sense Negative Input 3
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[1]	Power FET Ground 3
32			O	GD3	External Low Side Gate Driver 3
33				SW3	Power Switch 3
34				PGND2[1]	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				SW2	Power Switch 2
37				SW1	Power Switch 1
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[1]	Power FET Ground 1
40				SW0	Power Switch 0
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[1]	Power FETGround 0
43				GDV_{SS}	Gate Driver Ground

Figure 12-1. CY8CLED04D0x 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Note
1. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

12.3 CY8CLED04DOCD1 56-Pin Part Pinout (with OCD)

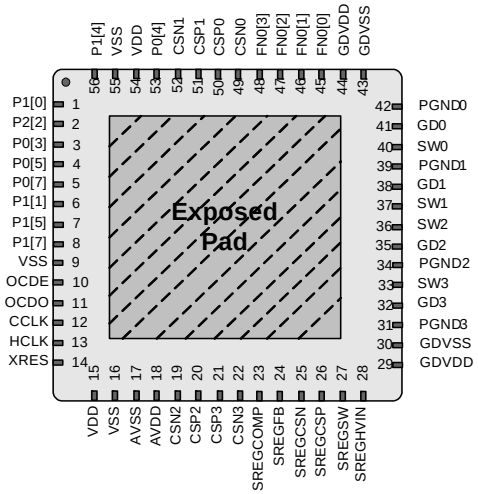
The CY8CLED04DOCD1 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-3. CY8CLED04DOCD1 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I2C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1) / Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCL (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I2C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I2C SCL (Primary)
9				V_{SS}	Digital Ground
10	I/O			OCDE	On Chip Debugger Port
11	I/O			OCDO	On Chip Debugger Port
12	I/O			CCLK	On Chip Debugger Port
13	I/O			HCLK	On Chip Debugger Port
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19			I	CSN2	Current Sense Negative Input 2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				CSP3	Current Sense Positive Input and Power Supply - CSA3
22			I	CSN3	Current Sense Negative Input 3
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[4]	Power FET Ground 3
32			O	GD3	External Low Side Gate Driver 3
33				SW3	Power Switch 3
34				PGND2[4]	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				SW2	Power Switch 2
37				SW1	Power Switch 1
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[4]	Power FET Ground 1
40				SW0	Power Switch 0
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[4]	Power FET Ground 0
43				GDV_{SS}	Gate Driver Ground
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Figure 12-3. CY8CLED04DOCD1 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Note
4. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

12.4 CY8CLED03D0x 56-Pin Part Pinout (without OCD)

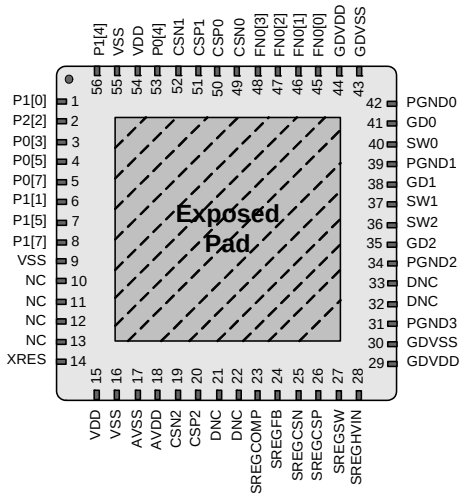
The CY8CLED03D01 and CY8CLED03D02 PowerPSoC devices are available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-4. CY8CLED03D0x 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I2C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCL (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I2C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I2C SCL (Primary)
9				V_{SS}	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19			I	CSN2	Current Sense Negative Input - CSA2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				DNC[5]	Do Not Connect
22				DNC[5]	Do Not Connect
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[6]	Power FET Ground 3
32				DNC[5]	Do Not Connect
33				DNC[5]	Do Not Connect
34				PGND2[6]	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				SW2	Power Switch 2
37				SW1	Power Switch 1
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[6]	Power FET Ground 1
40				SW0	Power Switch 0
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[6]	Power FETGround 0
43				GDV_{SS}	Gate Driver Ground

Figure 12-4. CY8CLED03D0x 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Notes
5. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
6. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

13.4 Register Map Bank 0 Table

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DPWM0PCF	40	RW	ASC10CR0	80	RW	VDAC0_CR	C0	RW
PRT0IE	01	RW	DPWM0PDH	41	RW	ASC10CR1	81	RW	VDAC0_DR0	C1	RW
PRT0GS	02	RW	DPWM0PDL	42	RW	ASC10CR2	82	RW	VDAC0_DR1	C2	RW
PRT0DM2	03	RW	DPWM0PWH	43	RW	ASC10CR3	83	RW		C3	
PRT1DR	04	RW	DPWM0PWL	44	RW	ASD11CR0	84	RW	VDAC1_CR	C4	RW
PRT1IE	05	RW	DPWM0PCH	45	RW	ASD11CR1	85	RW	VDAC1_DR0	C5	RW
PRT1GS	06	RW	DPWM0PCL	46	RW	ASD11CR2	86	RW	VDAC1_DR1	C6	RW
PRT1DM2	07	RW	DPWM0GCFG	47	RW	ASD11CR3	87	RW		C7	
PRT2DR	08	RW	DPWM1PCF	48	RW		88		VDAC2_CR	C8	RW
PRT2IE	09	RW	DPWM1PDH	49	RW		89		VDAC2_DR0	C9	RW
PRT2GS	0A	RW	DPWM1PDL	4A	RW		8A		VDAC2_DR1	CA	RW
PRT2DM2	0B	RW	DPWM1PWH	4B	RW		8B			CB	
FN0DR	0C	RW	DPWM1PWL	4C	RW		8C		VDAC3_CR	CC	RW
FN0IE	0D	RW	DPWM1PCH	4D	RW		8D		VDAC3_DR0	CD	RW
FN0GS	0E	RW	DPWM1PCL	4E	RW		8E		VDAC3_DR1	CE	RW
FN0DM2	0F	RW	DPWM1GCFG	4F	RW		8F			CF	
	10		DPWM2PCF	50	RW	ASD20CR0	90	RW	CUR_PP	D0	RW
	11		DPWM2PDH	51	RW	ASD20CR1	91	RW	STK_PP	D1	RW
	12		DPWM2PDL	52	RW	ASD20CR2	92	RW		D2	
	13		DPWM2PWH	53	RW	ASD20CR3	93	RW	IDX_PP	D3	RW
	14		DPWM2PWL	54	RW	ASC21CR0	94	RW	MVR_PP	D4	RW
	15		DPWM2PCH	55	RW	ASC21CR1	95	RW	MVW_PP	D5	RW
	16		DPWM2PCL	56	RW	ASC21CR2	96	RW	I2C_CFG	D6	RW
	17		DPWM2GCFG	57	RW	ASC21CR3	97	RW	I2C_SCR	D7	#
PDMUX_S1	18	RW	DPWM3PCF	58	RW		98		I2C_DR	D8	RW
PDMUX_S2	19	RW	DPWM3PDH	59	RW		99		I2C_MSCR	D9	#
PDMUX_S3	1A	RW	DPWM3PDL	5A	RW		9A		INT_CLR0	DA	RW
PDMUX_S4	1B	RW	DPWM3PWH	5B	RW		9B		INT_CLR1	DB	RW
PDMUX_S5	1C	RW	DPWM3PWL	5C	RW	VDAC6_CR	9C	RW	INT_CLR2	DC	RW
PDMUX_S6	1D	RW	DPWM3PCH	5D	RW	VDAC6_DR0	9D	RW	INT_CLR3	DD	RW
	1E		DPWM3PCL	5E	RW	VDAC6_DR1	9E	RW	INT_MSK3	DE	RW
CHBOND_CR	1F	RW	DPWM3GCFG	5F	RW		9F		INT_MSK2	DF	RW
DBB00DR0	20	#	AMX_IN	60	RW	VDAC4_CR	A0	RW	INT_MSK0	E0	RW
DBB00DR1	21	W	AMUX_CFG	61	RW	VDAC4_DR0	A1	RW	INT_MSK1	E1	RW
DBB00DR2	22	RW		62		VDAC4_DR1	A2	RW	INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#	VDAC5_CR	A4	RW	DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#	VDAC5_DR0	A5	RW	DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW	VDAC5_DR1	A6	RW	DEC_CR0	E6	RW
DBB01CR0	27	#	PAMUX_S1	67	RW		A7		DEC_CR1	E7	RW
DCB02DR0	28	#	PAMUX_S2	68	RW	MUL1_X	A8	W	MUL0_X	E8	W
DCB02DR1	29	W	PAMUX_S3	69	RW	MUL1_Y	A9	W	MUL0_Y	E9	W
DCB02DR2	2A	RW	PAMUX_S4	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCB02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBB10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBB10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBB11CR0	37	#	ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12DR0	38	#	DPWM0PCFG	78	RW	RDI1RI	B8	RW		F8	
DCB12DR1	39	W	DPWM1PCFG	79	RW	RDI1SYN	B9	RW		F9	
DCB12DR2	3A	RW	DPWM2PCFG	7A	RW	RDI1IS	BA	RW		FA	
DCB12CR0	3B	#	DPWM3PCFG	7B	RW	RDI1LT0	BB	RW		FB	
DCB13DR0	3C	#	DPWMINTFLG	7C	RW	RDI1LT1	BC	RW		FC	
DCB13DR1	3D	W	DPWMINTMSK	7D	RW	RDI1RO0	BD	RW	DAC_D	FD	RW
DCB13DR2	3E	RW	DPWMSYNC	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCB13CR0	3F	#		7F			BF		CPU_SCR0	FF	#

15.3 Power Peripheral Low Side N-Channel FET

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

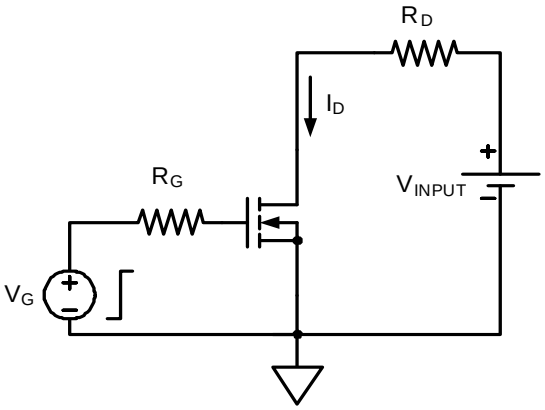
Table 15-4. Low Side N-Channel FET DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DS}	Operating drain to source voltage	–	–	32	V	
$V_{DS,INST}$	Instantaneous drain source voltage	–	–	36	V	
I_D	Average drain current	– –	– –	1 0.5	A A	CY8CLED04/3/2/1D01 devices CY8CLED04/3D02 devices
I_{DMAX}	Maximum instantaneous repetitive pulsed current	– –	– –	3 1.5	A A	Less than 33% duty cycle for an average current of 1 A, f_{SW} = 0.1 MHz. CY8CLED04/3/2/1D01 devices Less than 33% duty cycle for an average current of 0.5 A, f_{SW} = 0.1 MHz. CY8CLED04/3D02 devices
$R_{DS(ON)}$	Drain to source ON resistance	– –	– –	0.5 1	Ω Ω	I_D = 1 A, GDV_{DD} = 5 V, T_J = 25 °C CY8CLED04/3/2/1D01 devices I_D = 0.5 A, GDV_{DD} = 5 V, T_J = 25 °C CY8CLED04/3D02 devices
I_{DSS}	Switching node to PGND leakage	– –	– –	10 250	µA µA	T_J = 25 °C T_J = 115 °C (Industrial rated) and T_J = 125 °C (Extended Temperature rated)
I_{SFET}	Supply current per channel - FET (internal gate driver)	–	–	6.25	mA	f_{SW} = 2 MHz

Table 15-5. Low Side N-Channel FET AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_R	Rise time	–	–	20	ns	I_D = 1 A, R_D = 32 Ω
t_F	Fall time	–	–	20	ns	I_D = 1 A, R_D = 32 Ω

Figure 15-2. Low Side N-Channel FET Test Circuit for I_{DSS}, $t_{R, and}$ t_F



15.4 Power Peripheral External Power FET Driver

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-6. Power FET Driver DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OHN}	N-channel FET driver output voltage -drive high	V_{DD} – 0.45 V_{DD} – 0.10	– –	– –	V V	I_{OH} = 100 mA I_{OH} = 10 mA
V_{OLN}	N-channel FET driver output voltage -drive low	– –	– –	0.45 0.1	V V	I_{OL} = 100 mA I_{OL} = 10 mA
$I_{SFETDRV}$	Supply current per channel - external FET driver	–	–	25	mA	C_L = 4 nF F_{SW} = 1 MHz

Table 15-7. Power FET Driver AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_R	Rise time	–	45	55	ns	C_L = 4 nF
t_F	Fall time	–	45	55	ns	
$t_{P(LH)}$	Propagation delay (low-to-high)	–	–	10	ns	
$t_{P(HL)}$	Propagation delay (high-to-low))	–	–	10	ns	

15.5 Power Peripheral Hysteretic Controller

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-8. Hysteretic Controller DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{IO}	Comparator input offset voltage	– – –	– – –	7.5 10 15	mV mV mV	1 V ≤ V_{ICM} ≤ 3 V (industrial rated) 1 v ≤ v_{icm} ≤ 3 v (extended temperature rated) 0 V ≤ V_{ICM} ≤ V_{DD}
V_{ICM}	Input common mode voltage range	0	–	V_{DD}	V	
V_{HYS}	Hysteresis voltage	4.5 4.5	– –	11 13	mV mV	1.5 V ≤ V_{ICM} ≤ 2.5 V (industrial rated) 1.5 V ≤ V_{ICM} ≤ 2.5 V (extended temperature rated)
I_{SHYST}	Supply current - hysteretic controller	–	2	–	mA	Includes two power peripheral comparators and one reference DAC, f_{SW} = 2 MHz

15.8 Power Peripheral PWM/PrISM/DMM Specification Table

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only. See the *PowerPSoC Technical Reference Manual* for more information on PWM/PrISM/DMM.

Table 15-14. PWM/PrISM/DMM DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$I_{S,Modulation}$	Supply current - PWM, PrISM, or DMM	–	–	5	mA	

Table 15-15. PWM/PrISM/DMM AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
PWM Mode						
$f_{RANGE16}$	PWM output frequency range 16-bit period	24,000,000/(256*2^{16})	–	48,000,000/2^{16}	Hz	Period value = 2^{16} –1, Min: N = 255, Max: N = 0
f_{RANGE8}	PWM output frequency range 8-bit period	24,000,000/(256*2^{8})	–	48,000,000/2^{8}	Hz	Period value = 2^{8} –1, Min: N = 255, Max: N = 0
PrISM Mode						
f_{RANGE}	PrISM output frequency range	24,000,000/(256*(2^{M}–1)	–	48,000,000/2	Hz	Min: N = 255, Maqx: N = 0, M = 2 to 16
DMM Mode						
$f_{RANGE,Dimming}$	DMM dimming frequency range	24,000,000/ (256*Max DMM Period)	–	48,000,000/(Min DMM Period)	Hz	Min DMM Period: 2 (Right Aligned), 3 (Center Aligned), 4(Left Aligned) Max DMM Period: 2^{12} (Right Aligned), 8190 (Center Aligned), 2^{12} (Left Aligned)
$f_{RANGE,Dither}$	DMM dither frequency range	(1/16)*(Min $f_{RANGE,Dimming}$)	–	(15/16)*(Max $f_{RANGE,Dimming}$)	Hz	

15.9 Power Peripheral Reference DAC Specification

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-16. Reference DAC DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{SDAC}	Supply current - reference DAC	–	–	600	µA	Mode 0 and Mode1
INL	Integral non linearity	–1 –1.5	– –	1 1.5	LSB LSB	Mode 0 Mode 1
DNL	Differential non linearity	–0.5	–	0.5	LSB	Mode 0 and Mode1
A_{ERROR}	Gain error	–5 –7	– –	5 7	LSB LSB	Mode 0 Mode 1
OS_{ERROR}	Offset error	–	–	1	LSB	Mode 0 and Mode1
V_{DACFS}	Fullscale voltage - reference DAC	– –	– –	2.6 1.3	LSB LSB	Mode 0 Mode 1
V_{DACMM}	Fullscale voltage mismatch (pair of reference DACs - even and odd)	– – – –	– – – –	9 14 10.5 15.5	LSB LSB LSB LSB	Mode 0 (DAC0 through DAC7) Mode 1 (DAC0 through DAC7) Mode 0 (DAC8 through DAC13) Mode 1 (DAC8 through DAC13)

Table 15-17. Reference DAC AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{SETTLE}	Output settling time to 0.5 LSB of final value	–	–	10	µs	Mode 0 and Mode1
$t_{STARTUP}$	Startup time to within 0.5 LSB of final value	–	–	10.5	µs	Mode 0 and Mode1

15.10 Power Peripheral Built-in Switching Regulator

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-18. Built-in Switching Regulator DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REGIN}	Input supply voltage range	7 8	– –	32 32	V V	Industrial rated Extended temperature rated See Absolute Maximum Ratings on page 30
V_{REGOUT}	Output voltage range	4.8	5.0	5.2	V	Does not include V_{RIPPLE}
V_{RIPPLE}	Output ripple	–	–	100	mV	
V_{UVLO}	Under voltage lockout voltage	5.5	–	6.5	V	$V_{REGIN} < V_{UVLO}$: Power down mode $V_{REGIN} > V_{UVLO}$: Active mode
I_{LOAD}	DC output current -active mode	0.01	–	250	mA	–
$I_{S,BSR}$	Supply current - built-in switching regulator	–	–	4	mA	–
$I_{SB,HV}$	Standby current (high voltage)	–	–	250	µA	–
I_{INRUSH}	Inrush current	– –	– –	1.2 1.5	A A	V_{REGIN} = 32 V, SR_{REGIN} = 32 V/ms (Industrial rated) V_{REGIN} = 32 V, SR_{REGIN} = 32 V/ms (Extended Temperature rated)
$R_{DS(ON),PFET}$	PFET drain to source ON resistance	–	2.5	–	Ω	
$Line_{REG}$	Line regulation	–	1	–	mV	I_{LOAD} = 250 mA, V_{REGIN} = 7 V to 32 V

Table 15-18. Built-in Switching Regulator DC Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
$Load_{REG}$	Load regulation	–	1	–	mV	V_{REGIN} = 24 V, I_{LOAD} = 2.5 mA to 250 mA
PSRR	Power supply rejection ratio	–	–60	–	dB	V_{RIPPLE} = 0.2 * V_{REGIN}, f_{RIPPLE} = 1 kHz to 10 kHz
E_{BSR}	Built-in switching regulator efficiency	80	–	–	%	V_{REGIN} = 24 V, I_{LOAD} = 250 mA

Table 15-19. Built-in Switching Regulator AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
f_{SW}	Switching frequency	0.956	1	1.04	MHz	–
t_{RESP}	Response time to within 0.5% of final value	–	10	–	µs	–
t_{SU}	Startup time	–	–	1	ms	–
t_{PD}	Power down time	–	–	100	µs	–
t_{PD_ACT}	Time from power down to active mode	–	–	1	ms	–
t_{ACT_PD}	Time from active mode to power down mode	–	–	50	µs	–
SR_{REGIN}	Ramp rate for the SREGHVIN pin	–	–	32	V/µs	See Absolute Maximum Ratings on page 30

Table 15-20. Built-in Switching Regulator Recommended Components

Component Name	Value	Unit	Notes
R_{fb1}	2	kΩ	Tolerance 1% and 0.05-W rated or better
R_{fb2}	0.698	kΩ	Tolerance 1% and 0.05-W rated or better
C_{comp}	2200	pF	Tolerance 20% and 6.3-V rated or better
R_{comp}	20	kΩ	Tolerance 5% and 0.05-W rated or better
L	47	µH	Tolerance 20% or better, Saturation current rating of 1.5 A or higher
R_{sense}	0.5	Ω	Tolerance 1% and 0.05 W (I_{LOAD} = 0.250 A) rated or better
C_1	10	µF	Ceramic, X7R grade, Minimum ESR of 0.1 Ω, 6.3-V rated
C_{in}	1	µF	Ceramic, X7R grade, 50-V rated (V_{REGIN} = 32 V)
D1	40/0.5	V/A	Schottky diode - Reverse voltage 40 V, average rectified forward current 0.5 A (V_{REGIN} = 32 V)

Note If the built-in switching regulator is not being used in a design, it must be configured as per the following instructions to ensure it is disabled in a safe state.

SREGFB: 5 V

SREGCSN: 5 V

SREGCSP: 5 V

SREGCOMP: Floating

SREGHVIN: ≥ VDD rail

SREGSW: Floating/Tie to SREGHVIN

If the switching regulator is disabled through wiring its input pins (as previously explained) then it must be disabled through software as well (bit SREG_TST[0] = 1), which is set in the Global Resources in the Interconnect View of PSoC Designer.

Figure 15-5. Built-in Switching Regulator Timing Diagram

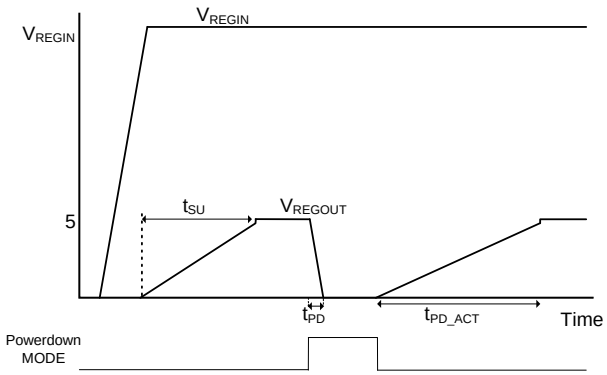
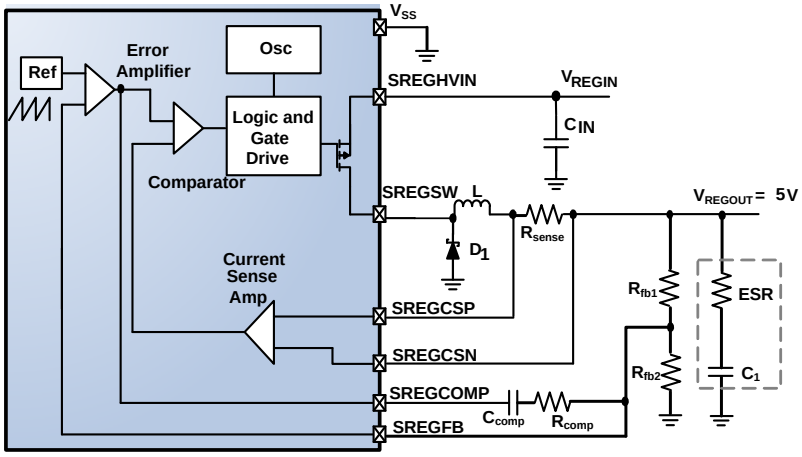


Figure 15-6. Built-in Switching Regulator



15.11 General Purpose I/O / Function Pin I/O

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-21. GPIO/FN0 Pin I/O DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	–
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	–
V_{OH}	High output level	V_{DD} – 1.0	–	–	V	I_{OH} = 10 mA, 80 mA maximum combined I_{OH} budget
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 25 mA, 200 mA maximum combined I_{OL} budget
I_{OH}	High level source current	10	–	–	mA	$V_{OH} = V_{DD}$–1.0 V, see the limitations of the total current in the note for V_{OH}
I_{OL}	Low level sink current	25	–	–	mA	V_{OL} = 0.75 V, see the limitations of the total current in the note for V_{OL}
V_{IL}	Input low level	–	–	0.8	V	–
V_{IH}	Input high level	2.1	–		V	–
V_H	Input hysterisis	–	60	–	mV	–
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	T_J = 25 °C.
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	T_J = 25 °C.

Table 15-22. GPIO/FN0 Pin I/O AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
f_{GPIO}	GPIO operating frequency	0	–	12	MHz	Normal strong mode
tRiseF	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	10% – 90%
tFallF	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	
tRiseS	Rise time, slow strong mode, Cload = 50 pF	10	27	–	ns	
tFallS	Fall time, slow strong mode, Cload = 50 pF	10	22	–	ns	

Figure 15-7. GPIO/Function I/O Timing Diagram

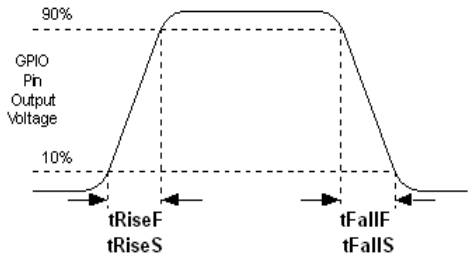


Table 15-24. Operational Amplifier AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROA}	Rising settling time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = low, opamp bias = low Power = medium, opamp bias = high Power = high, opamp bias = high	 – – –	 – – –	 3.9 0.72 0.62	 µs µs µs	–
t_{SOA}	Falling settling time from 20% of ΔV to 0.1% of ΔV (10 pF load, unity gain) Power = low, opamp bias = low Power = medium, opamp bias = high Power = high, opamp bias = high	 – – –	 – – –	 5.9 0.92 0.72	 µs µs µs	–
SR_{ROA}	Rising slew rate (20% to 80%) (10 pF load, unity gain) Power = low, opamp bias = low Power = medium, opamp bias = high Power = high, opamp bias = high	 0.15 1.7 6.5	 – – –	 – – –	 V/µs V/µs V/µs	–
SR_{FOA}	Falling slew rate (20% to 80%) (10 pF load, unity gain) Power = low, opamp bias = low Power = medium, opamp bias = high Power = high, opamp bias = high	 0.01 0.5 4.0	 – – –	 – – –	 V/µs V/µs V/µs	–
BW_{OA}	Gain bandwidth product Power = low, opamp bias = low Power = medium, opamp bias = high Power = high, opamp bias = high	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz	–
E_{NOA}	Noise at 1 kHz (power = medium, opamp bias = high)	–	100	–	nV/r-Hz	–

15.13 PSoC Core Low Power Comparator

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-25. Low Power Comparator DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	$V_{DD} - 1$	V	–
I_{SLPC}	LPC supply current	–	10	40	µA	–
V_{OSLPC}	LPC voltage offset	–	2.5	40	mV	–

Table 15-26. Low Power Comparator AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RLPC}	LPC response time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}.

15.15 PSoC Core Analog Reference

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for extended temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the analog continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Table 15-29. Analog Reference DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
BG	Bandgap voltage reference	1.28 1.27	1.30 1.30	1.32 1.33	V V	Industrial rated Extended Temperature rated
–	AGND = $V_{DD}/2$[16]	$V_{DD}/2 - 0.04$ $V_{DD}/2 - 0.02$	$V_{DD}/2 - 0.01$ $V_{DD}/2$	$V_{DD}/2 + 0.007$ $V_{DD}/2 + 0.02$	V V	Industrial rated Extended Temperature rated
–	AGND = 2 x BandGap[16]	2 x BG – 0.048	2 x BG – 0.030	2 x BG + 0.024	V	
–	AGND = BandGap[16]	BG – 0.009	BG + 0.008	BG + 0.016	V	
–	AGND = 1.6 x BandGap[16]	1.6 x BG – 0.022	1.6 x BG – 0.010	1.6 x BG + 0.018	V	
–	AGND Block to Block Variation (AGND = $V_{DD}/2$)[16]	–0.034	0.000	0.034	V	
–	RefHi = $V_{DD}/2$ + BandGap	$V_{DD}/2$ + BG – 0.10	$V_{DD}/2$ + BG	$V_{DD}/2$ + BG + 0.10	V	
–	RefHi = 3 x BandGap	3 x BG – 0.06	3 x BG	3 x BG + 0.06	V	
–	RefHi = 3.2 x BandGap	3.2 x BG – 0.112	3.2 x BG	3.2 x BG + 0.076	V	
–	RefLo = $V_{DD}/2$ – BandGap	$V_{DD}/2$ – BG – 0.04 $V_{DD}/2$ – BG – 0.06	$V_{DD}/2$ – BG + 0.024 $V_{DD}/2$ – BG	$V_{DD}/2$ – BG + 0.04 $V_{DD}/2$ – BG + 0.06	V V	Industrial rated Extended Temperature rated
–	RefLo = BandGap	BG – 0.06	BG	BG + 0.06	V	

15.16 PSoC Core Analog Block

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-30. Analog Block DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor unit value (continuous time)	–	12.2	–	kΩ	
C_{SC}	Capacitor unit value (switched capacitor)	–	80	–	fF	

Notes
16. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3 V ± 0.02 V.

15.17 PSoC Core POR and LVD

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the *PowerPSoC Technical Reference Manual* for more information on the VLT_CR register.

Table 15-31. POR and LVD DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PPOR2}	V_{DD} Value for PPOR Trip PORLEV[1:0] = 10b	–	4.55	4.70	V	–
	V_{DD} Value for LVD Trip					–
V_{LVD6}	VM[2:0] = 110b	4.62	4.73	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.81	4.95	V	

15.18 PSoC Core Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-32. Programming DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDP}	Supply current during programming or verify	–	15	30	mA	–
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	–
V_{IHP}	Input high voltage during programming or verify	2.1	–	–	V	–
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull down resistor.
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	–
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	–
$Flash_{ENPB}$	Flash endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[17]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention[18]	10	–	–	Years	–

Notes
17. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36 x 1 blocks of 50,000 maximum cycles each, 36 x 2 blocks of 25,000 maximum cycles each, or 36 x 4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36 x 50,000 and that no single block ever sees more than 50,000 cycles)
18. Guaranteed for –40 °C ≤ T_A ≤ 85 °C for Industrial rated devices and –40 °C ≤ T_A ≤ 105 °C for Extended Temperature rated devices.

16. Ordering Information

Table 16-1. Device Key Features and Ordering Information

PowerPSoC Part Number	No. of Pins	Package	Channels	Voltage	Internal FETs	Gate Drivers for External Low Side N-FETs
CY8CLED04D01-56LTXI	56 QFN	8 mm × 8 mm	4	32 V	4 × 1.0 A	4
CY8CLED04D02-56LTXI	56 QFN	8 mm × 8 mm	4	32 V	4 × 0.5 A	4
CY8CLED04G01-56LTXI	56 QFN	8 mm × 8 mm	4	32 V	0	4
CY8CLED04DOCD1-56LTXI	56 QFN	8 mm × 8 mm	4	32 V	4 × 1.0 A	4
CY8CLED03D01-56LTXI	56 QFN	8 mm × 8 mm	3	32 V	3 × 1.0 A	3
CY8CLED03D02-56LTXI	56 QFN	8 mm × 8 mm	3	32 V	3 × 0.5 A	3
CY8CLED03G01-56LTXI	56 QFN	8 mm × 8 mm	3	32 V	0	3
CY8CLED02D01-56LTXI	56 QFN	8 mm × 8 mm	2	32 V	2 × 1.0 A	2
CY8CLED01D01-56LTXI	56 QFN	8 mm × 8 mm	1	32 V	1 × 1.0 A	1
CY8CLED01D01-56LTXQ	56 QFN	8 mm × 8 mm	1	32 V	1 × 1.0 A	1

16.1 Ordering Code Definitions

CY 8 C LED0x xxx (xxxx) - xx xxxx