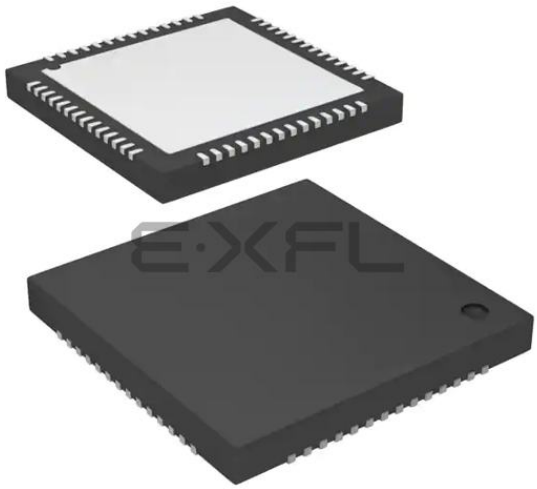


Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Intelligent LED Driver
Core Processor	M8C
Program Memory Type	FLASH (16KB)
Controller Series	CY8CLED
RAM Size	1K x 8
Interface	DALI, DMX512, I²C, IrDA, SPI, UART/USART
Number of I/O	14
Voltage - Supply	4.75V ~ 5.25V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad
Supplier Device Package	56-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8cled04d02-56ltxi

Figure 3-2. CY8CLED04G01 Logic Block Diagram

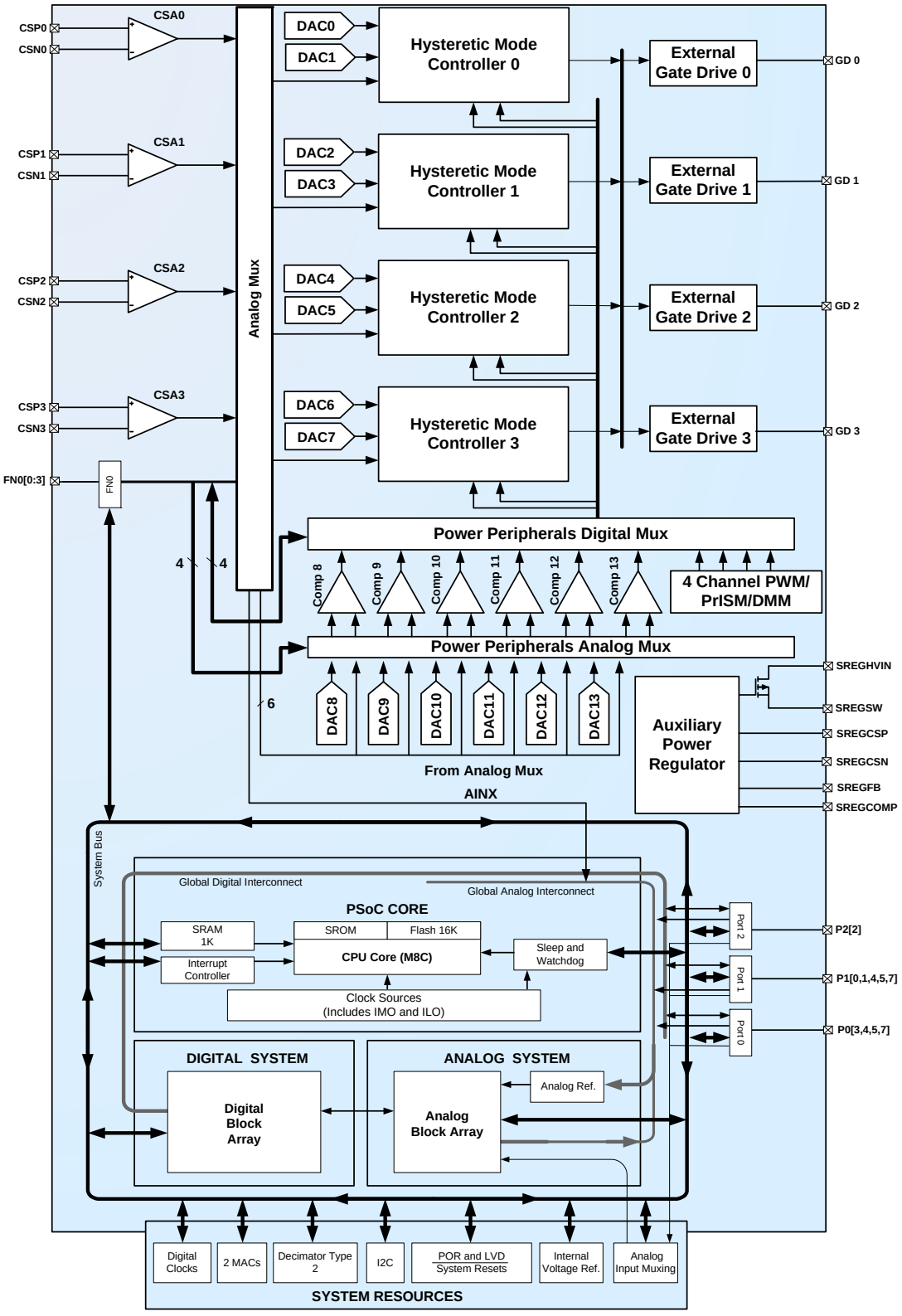


Figure 3-4. CY8CLED03G01 Logic Block Diagram

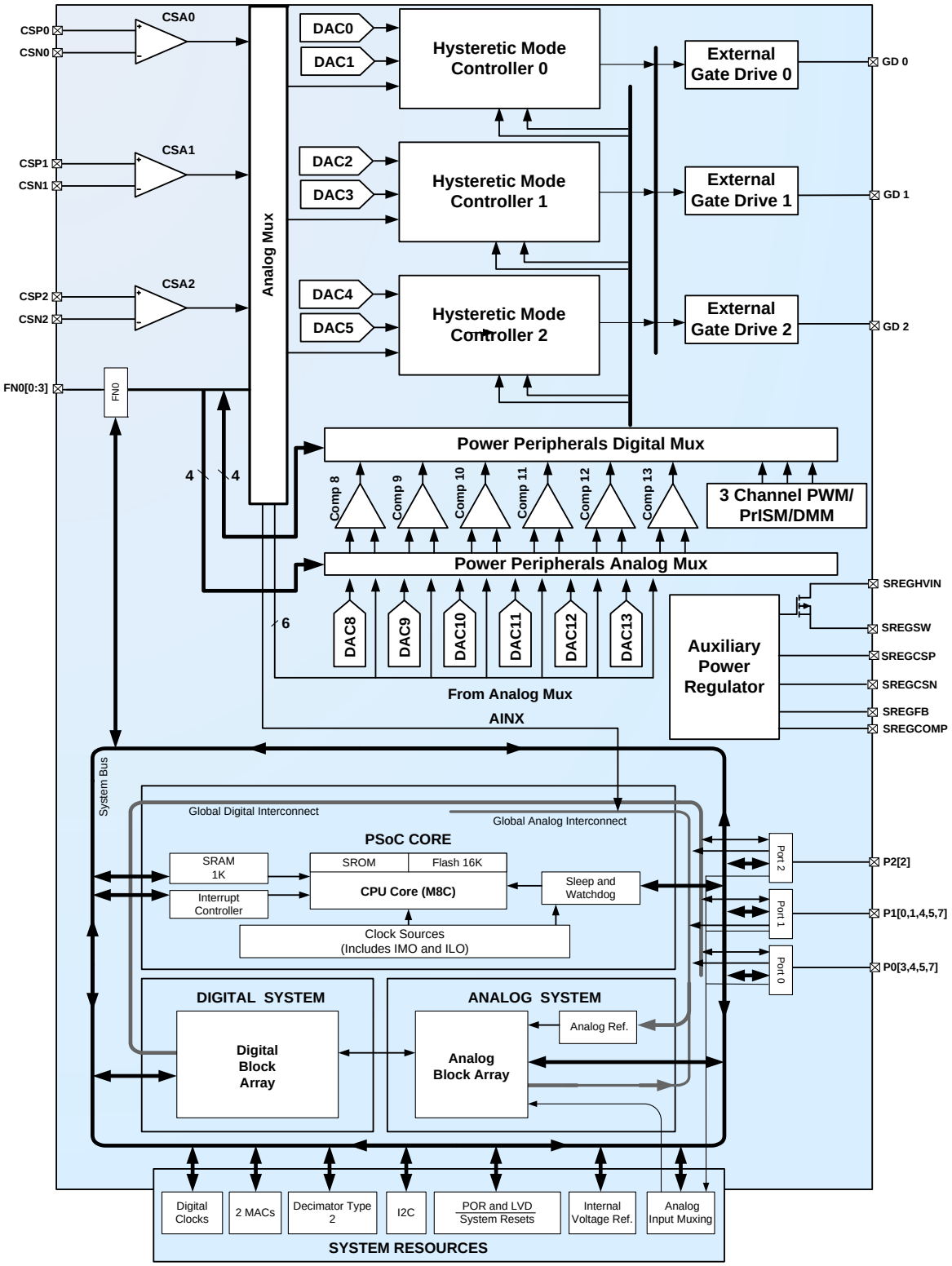
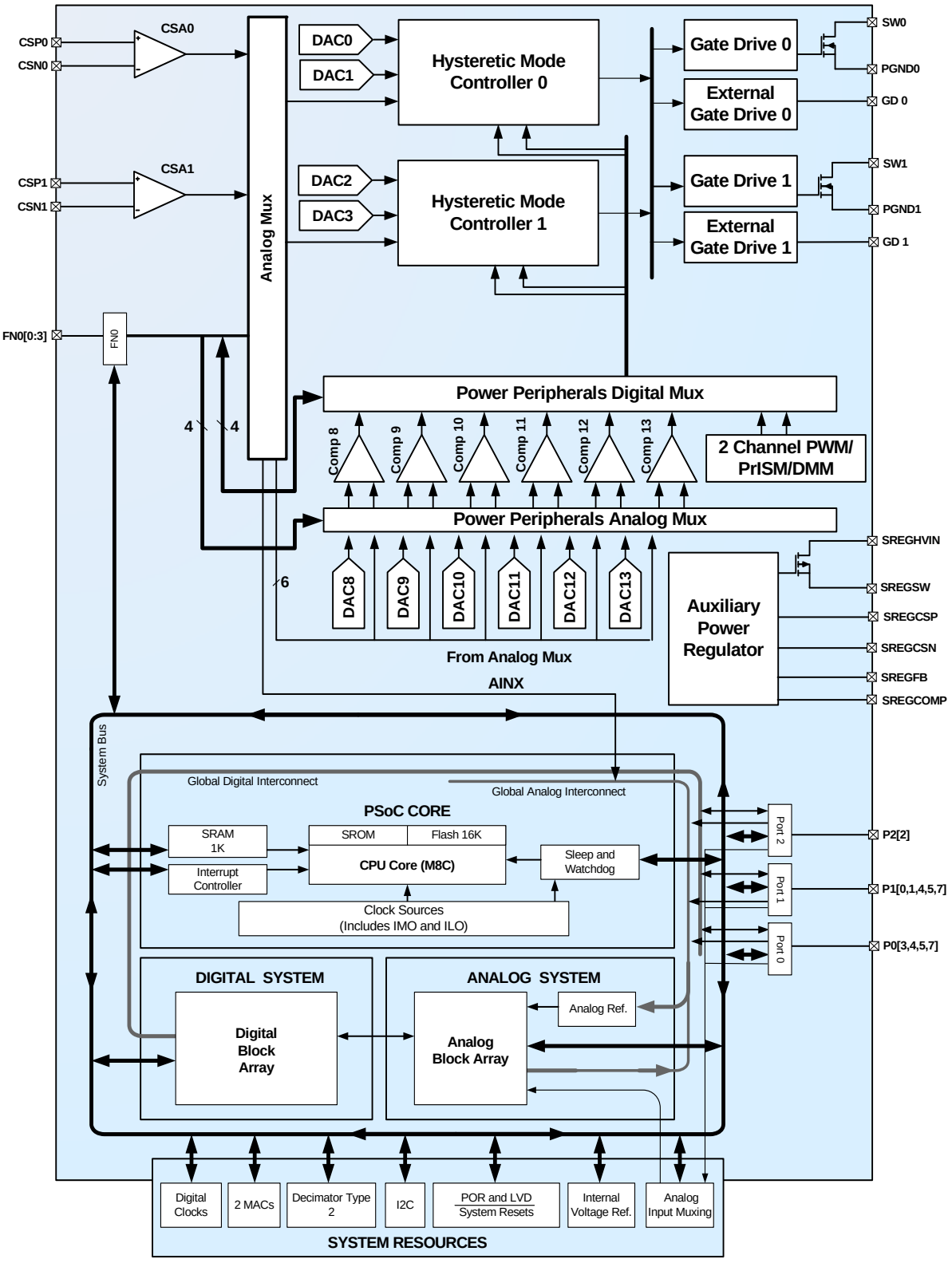


Figure 3-5. CY8CLED02D01 Logic Block Diagram



4. PowerPSoC® Functional Overview

The PowerPSoC family incorporates programmable system-on-chip technology with the best in class power electronics controllers and switching devices to create easy to use power-system-on-chip solutions for lighting applications.

All PowerPSoC family devices are designed to replace traditional MCUs, system ICs, and the numerous discrete components that surround them. PowerPSoC devices feature high performance power electronics including 1 ampere 2 MHz power FETs, hysteretic controllers, current sense amplifiers, and PrISM/PWM modulators to create a complete power electronics solution for LED power management. Configurable power, analog, digital, and interconnect circuitry enables a high level of integration in a host of industrial, commercial, and consumer LED lighting applications.

This architecture integrates programmable analog and digital blocks to enable you to create customized peripheral configurations that match the requirements of each individual application. Additionally, the device includes a 24 MHz CPU, Flash program memory, SRAM data memory, and configurable I/O in a range of convenient pinouts and packages.

The PowerPSoC architecture, as illustrated in the block diagrams, consists of five main areas: PSoC core, digital system, analog system, system resources, and power peripherals, which include power FETs, hysteretic controllers, current sense amplifiers, and PrISM/PWM modulators. Configurable global busing combines all of the device resources into a complete custom system. The PowerPSoC family of devices have 10-port I/Os that connect to the global digital and analog interconnects, providing access to eight digital blocks and six analog blocks.

5. Power Peripherals

PowerPSoC is designed to operate at voltages from 7 V to 32 V, drive up to 1 ampere of current using internal MOSFET switches, and over 1 ampere with external MOSFETs.

This family of devices (CY8CLED0xD/G0y) combines up to four independent channels of constant current drivers. These drivers feature hysteretic controllers with the Programmable System-on-Chip (PSoC) that contains an 8-bit microcontroller, configurable digital and analog peripherals, and embedded flash memory.

The CY8CLED0xD/G0y is the first product in the PowerPSoC family to integrate power peripherals to add further integration for your power electronics applications.The PowerPSoC family of intelligent power controller ICs are used in lighting applications that need traditional MCUs and discrete power electronics support. The power peripherals of the CY8CLED0xD/G0y include up to four 32 volt power MOSFETs with current ratings up to 1 ampere each. It also integrates gate drivers that enable applications to drive external MOSFETs for higher current and voltage capabilities. The controller is a programmable threshold hysteretic controller, with user-selectable feedback paths that uses the IC in current mode floating load buck, floating load buck-boost, and boost configurations.

5.1 Hysteretic Controllers

The PowerPSoC contains four hysteretic controllers. There is one hysteretic controller for each channel of the device.

The hysteretic controllers provide cycle by cycle switch control with fast transient response, which simplifies system design by requiring no external compensation. The hysteretic controllers include the following key features:

- Four independent channels
- DAC configurable thresholds
- Wide switching frequency range from 20 kHz to 2 MHz
- Programmable minimum on and off time
- Floating load buck, floating load buck-boost and boost topology controller

The reference inputs (REF_A and REF_B in Figure 5-1.) of the hysteretic controller are provided by the reference DACs as illustrated in the top level block diagram (see Figure 3-1. on page 3).

The hysteretic control function output is generated by comparing the feedback value to two thresholds. Going below the lower threshold turns the switch ON and exceeding the upper threshold turns the switch OFF as shown in Figure 5-1. The output current waveforms are shown in Figure 5-2.

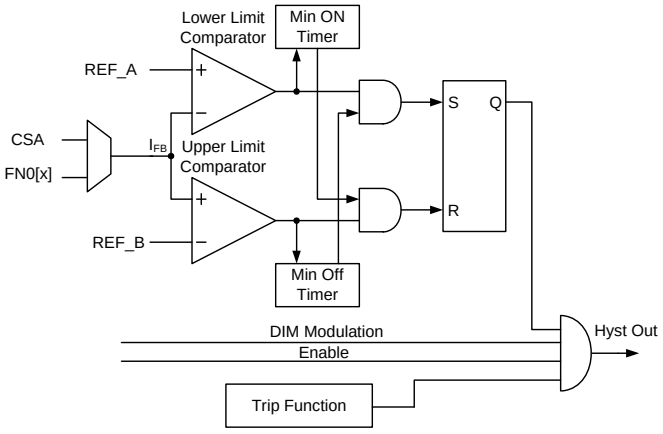
The hysteretic controller also controls the minimum on-time and off-time. This circuit prevents oscillation at very high frequencies; which can be very destructive to output switches.

The output to the gate drivers is gated by the Trip, DIM and Enable signals. The Enable signal is a direct result of the enable bit in the control register for the hysteretic controller.

The Trip signal can be any digital signal that follows TTL logic (logic high and logic low). It is an active high input.

The DIM Modulation signal is the output of the dedicated modulators that are present in the power peripherals, or any other digital modulation signal.

Figure 5-1. Generating Hysteretic Control Function Output



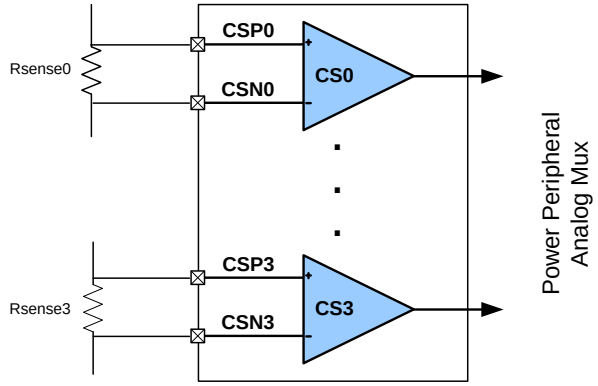
the routing is done. Table 5-1 illustrates example values of R_{sense} for different currents.

The method to calculate the R_{sense} value for a desired average current is explained in the application note CY8CLED0xx0x: Topology and Design Guide for Circuits using PowerPSoC - AN52699

Table 5-1. R_{sense} Values for Different Currents

Max Load Current (mA)	Typical R_{sense} (mΩ)
1000	100
750	130
500	200
350	300

Figure 5-3. High Side Current Measurement



5.6 Voltage Comparators

There are six comparators that provide high speed comparator operation for over voltage, over current, and various other system event detections. For example, the comparators may be used for zero crossing detection for an AC input line or monitoring total DC bus current. Programmable internal analog routing enables these comparators to monitor various analog signals. These comparators include the following key features:

- High speed comparator operation: 100 ns response time
- Programmable interrupt generation
- Low input offset voltage and input bias currents

Six precision voltage comparators are available. The differential positive and negative inputs of the comparators are routed from the analog multiplexer and the output goes to the digital multiplexer. A programmable inverter is used to select the output polarity. User-selectable hysteresis can be enabled or disabled to trade-off noise immunity versus comparator sensitivity.

5.7 Reference DACs

The reference DACs are used to generate set points for various analog modules such as Hysteretic controllers and comparators. The reference DACs include the following key features:

- 8-bit resolution
- Guaranteed monotonic operation
- Low gain errors
- 10 us settling time

These DACs are available to provide programmable references for the various analog and comparator functions and are controlled by memory mapped registers.

DAC[0:7] are embedded in the hysteretic controllers and are required to set the upper and lower thresholds for channel 0 to 3.

DAC [8:13] are connected to the Power Peripherals Analog Multiplexer and provide programmable references to the comparator bank. These are used to set trip points which enable over voltage, over current, and other system event detection.

5.8 Built-in Switching Regulator

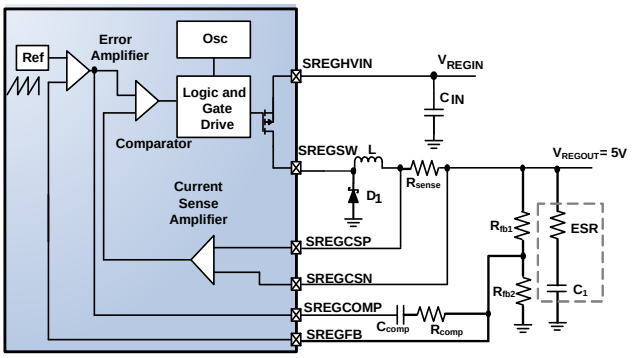
The switching regulator is used to power the low voltage (5 V portion of the PowerPSoC) from the input line. This regulator is based upon a peak current control loop which can support up to 250 mA of output current. The current not being consumed by PowerPSoC is used to power additional system peripherals. The key features of the built-in switching regulator include:

- Ability to self power device from input line
- Small filter component sizes
- Fast response to transients

Refer to Table 15-20 for component values.

The 'Ref' signal that forms the reference to the Error Amplifier is internally generated and there is no user control over it.

Figure 5-4. Built-in Switching Regulator



5.9 Analog Multiplexer

The PowerPSoC family's analog MUX is designed to route signals from the CSA output, function I/O pins and the DACs to comparator inputs and the current sense inputs of the hysteretic controllers. Additionally, CSA outputs can be routed to the AINX block using this MUX.

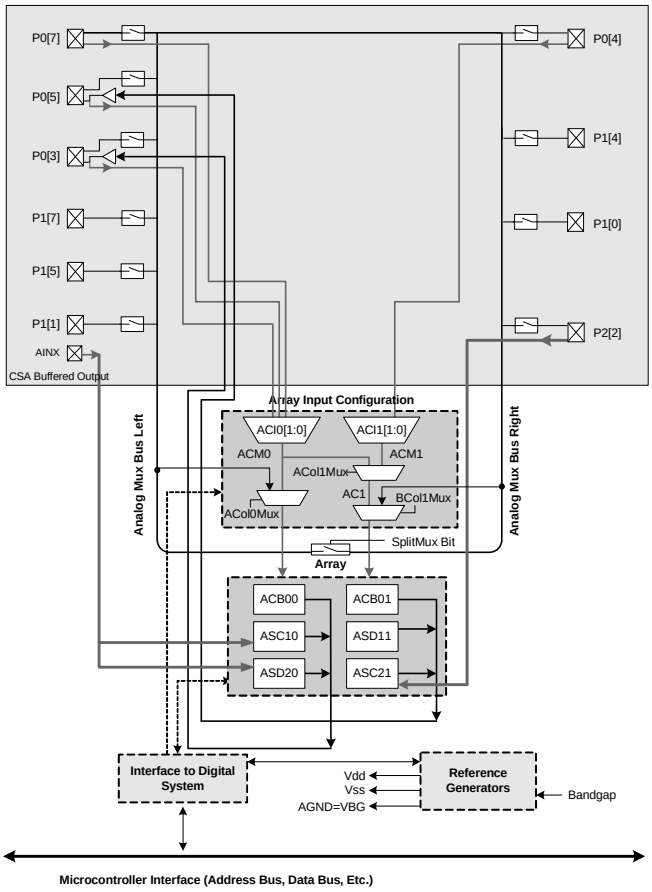
For a full matrix representation of all possible routing using this MUX, refer to the PowerPSoC Technical Reference Manual.

The CPU configures the Power Peripherals Analog Multiplexer connections using memory mapped registers. The analog multiplexer includes the following key features:

- Signal integrity for minimum signal corruption

Analog blocks are arranged in two columns of three blocks each, which includes one continuous time (CT) and two switched capacitor (SC) blocks, as shown in Figure 6-2. on page 14.

Figure 6-2. Analog System Block Diagram



6.3 Analog Multiplexer System

The Analog Mux Bus connects to every GPIO pin in ports 0 to 2. Pins can be connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters. It can be split into two sections for simultaneous dual-channel processing. An additional analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Track pad, finger sensing
- Crosspoint connection between any I/O pin combinations

Like other PSoC devices, PowerPSoC has specific pins allocated to the reference capacitor (Ref Cap) and modulation resistor (Mod resistor). These are indicated in the device pinouts (Section 13). For more details on capacitive sensing, see the design guide, Getting Started With CapSense. Apart from these, there are a number of application notes on Capacitive Sensing on the Cypress webbiest. The PowerPSoC Technical Reference Manual provides details on the analog system configuration that enables all I/Os in the device to be CapSense inputs.

6.4 Additional System Resources

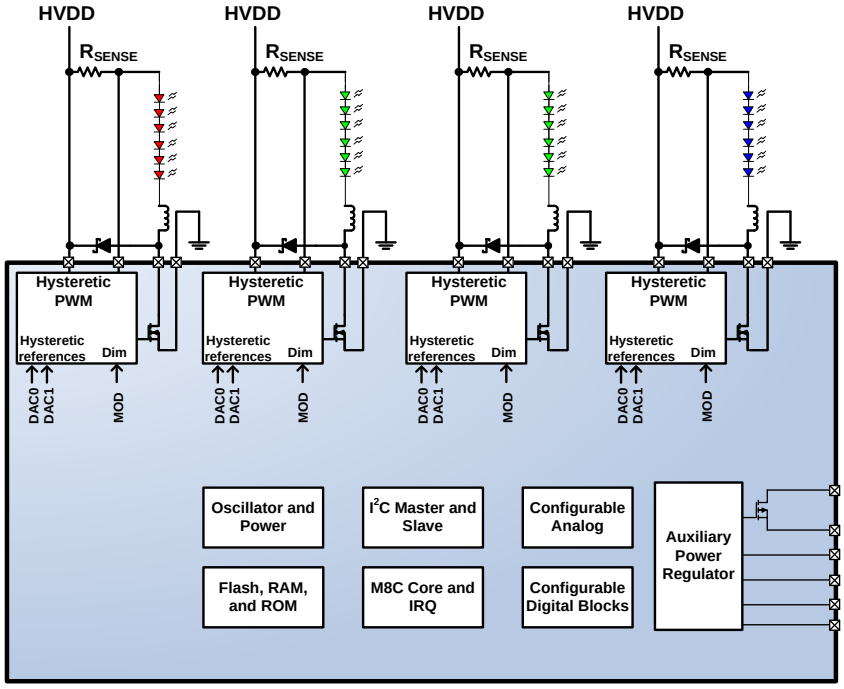
System resources provide additional capability useful in complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power on reset. Brief statements describing the merits of each resource follow.

- Two multiply accumulates (MACs) provide fast 8-bit multipliers with 32-bit accumulate, to assist in both general math and digital filters.
- A decimator provides a custom hardware filter for digital signal processing applications including creation of delta sigma ADCs.
- Low-voltage detection (LVD) interrupts signal the application of falling voltage levels, while the advanced POR (power on reset) circuit eliminates the need for a system supervisor.
- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. The designer can generate additional clocks using digital PSoC blocks as clock dividers.
- The I^2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master applications are supported.
- An internal 1.3 V reference provides an absolute reference for the analog system, including ADCs and DACs.
- Versatile analog multiplexer system.

7. Applications

The PowerPSoC family of devices can be used to add hysteretic current control capability to power applications. The devices can be used to control current in devices such as LEDs, heating elements, and solenoids. For LED applications, all high-brightness LEDs (HBLEDs) can be controlled using the PowerPSoC. The following figures show examples of applications in which the PowerPSoC family of devices adds intelligent power control for power applications.

Figure 7-1. LED Lighting with RGGB Color Mixing Configured as Floating Load Buck Converter



9. Getting Started

The quickest way to understand the PowerPSoC device is to read this datasheet and then use the PSoC Designer integrated development environment (IDE). This datasheet is an overview of the PowerPSoC integrated circuit and presents specific pin, register, and electrical specifications. For in depth information, along with detailed programming information, refer to the *PowerPSoC Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PowerPSoC device datasheets on the web at www.cypress.com.

9.1 Application Notes

Application notes are an excellent introduction to a wide variety of possible PowerPSoC designs. Layout guidelines, thermal management and firmware design guidelines are some of the topics covered. To view the PowerPSoC application notes, go to htttp://www.cypress.com/powerpsoc and click on the Application Notes link.

9.2 Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store contains development kits, C compilers, and all accessories for PowerPSoC development. For more information on the kits or to purchase a kit from the Cypress web site, go to htttp://www.cypress.com/powerpsoc and click on the Development Kits link.

9.3 Training

Free PowerPSoC technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

9.4 CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PowerPSoC designs. To contact or become a PSoC Consultant go to www.cypress.com/cypros.

9.5 Technical Support

PowerPSoC application engineers take pride in fast and accurate response. They can be reached with a 24-hour guaranteed response at http://www.cypress.com/support/. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

10. Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE runs on Windows XP, Windows Vista, or Windows 7.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built-in support for third-party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PowerPSoC family.

10.1 PSoC Designer Software Subsystems

10.1.1 Chip-Level View

The chip-level view is a more traditional integrated development environment (IDE) based on PSoC Designer. Choose a base device to work with and then select different onboard analog and digital components called user modules that use the PowerPSoC blocks. Examples of user modules are current sense amplifiers, PrISM, PWM, DMM, Floating Load Buck, and Boost. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

10.1.2 Code Generation Tools

PSoC Designer supports multiple third party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to merge seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PowerPSoC family of devices. The products allow you to create complete C programs for the PowerPSoC family of devices.

The optimizing C compilers provide all the features of C tailored to the PowerPSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

10.1.3 Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PowerPSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

10.1.4 Online Help System

The online help system displays online, context-sensitive help for you. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to faqs and an Online Support Forum to aid the designer in getting started.

12.4 CY8CLED03D0x 56-Pin Part Pinout (without OCD)

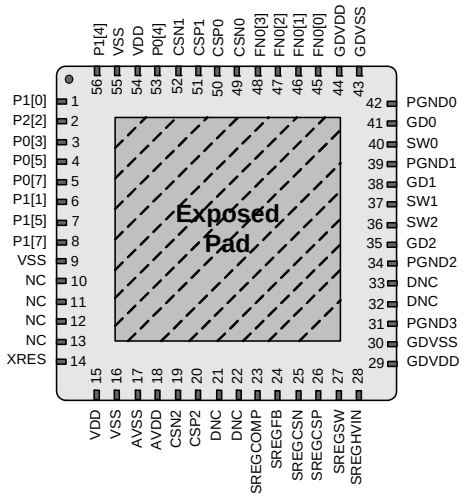
The CY8CLED03D01 and CY8CLED03D02 PowerPSoC devices are available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-4. CY8CLED03D0x 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I2C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCL (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I2C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I2C SCL (Primary)
9				V_{SS}	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19			I	CSN2	Current Sense Negative Input - CSA2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				DNC[5]	Do Not Connect
22				DNC[5]	Do Not Connect
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[6]	Power FET Ground 3
32				DNC[5]	Do Not Connect
33				DNC[5]	Do Not Connect
34				PGND2[6]	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				SW2	Power Switch 2
37				SW1	Power Switch 1
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[6]	Power FET Ground 1
40				SW0	Power Switch 0
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[6]	Power FETGround 0
43				GDV_{SS}	Gate Driver Ground

Figure 12-4. CY8CLED03D0x 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Notes
5. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
6. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

12.5 CY8CLED03G01 56-Pin Part Pinout (without OCD)

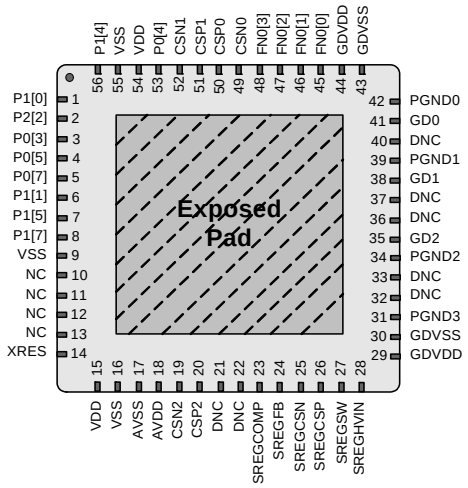
The CY8CLED03G01 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-5. CY8CLED03G01 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I2C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCL (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I2C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I2C SCL (Primary)
9				V_{SS}	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19			I	CSN2	Current Sense Negative Input 2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				DNC[7]	Do Not Connect
22				DNC[7]	Do Not Connect
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[8]	Power FET Ground 3
32				DNC[7]	Do Not Connect
33				DNC[7]	Do Not Connect
34				PGND2[8]	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				DNC[7]	Do Not Connect
37				DNC[7]	Do Not Connect
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[8]	Power FET Ground 1
40				DNC[7]	Do Not Connect
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[8]	Power FET Ground 0
43				GDV_{SS}	Gate Driver Ground

Figure 12-5. CY8CLED03G01 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Notes
7. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
8. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

12.6 CY8CLED02D01 56-Pin Part Pinout (without OCD)

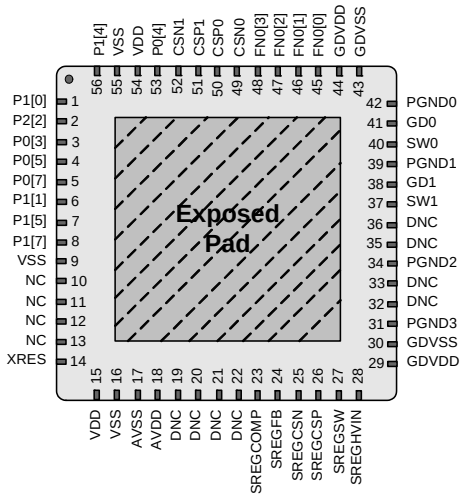
The CY8CLED02D01 PowerPSoC devices are available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-6. CY8CLED02D01 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I2C SDA (Secondary)/ ISSP SDATA
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Analog Input (Column 0)/ Analog Output (Column 0)
4	I/O	I/O		P0[5]	GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Analog Input (Column 0)/ Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCLK (Secondary)/ ISSP SCLK
7	I/O	I		P1[5]	GPIO/I2C SDA (Primary)
8	I/O	I		P1[7]	GPIO/I2C SCL (Primary)
9				V_{SS}	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				V_{DD}	Digital Power Supply
16				V_{SS}	Digital Ground
17				AV_{SS}	Analog Ground
18				AV_{DD}	Analog Power Supply
19				DNC[9]	Do Not Connect
20				DNC[9]	Do Not Connect
21				DNC[9]	Do Not Connect
22				DNC[9]	Do Not Connect
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDV_{DD}	Gate Driver Power Supply
30				GDV_{SS}	Gate Driver Ground
31				PGND3[10]	Power FET Ground 3
32				DNC[9]	Do Not Connect
33				DNC[9]	Do Not Connect
34				PGND2[10]	Power FET Ground 2
35				DNC[9]	Do Not Connect
36				DNC[9]	Do Not Connect
37				SW1	Power Switch 1
38			O	GD1	External Low Side Gate Driver 1
39				PGND1[10]	Power FET Ground 1
40				SW0	Power Switch 0
41			O	GD0	External Low Side Gate Driver 0
42				PGND0[10]	Power FETGround 0
43				GDV_{SS}	Gate Driver Ground

Figure 12-6. CY8CLED02D01 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
44				GDV_{DD}	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Analog Input (Column 1) / Bandgap Output
54				V_{DD}	Digital Power Supply
55				V_{SS}	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Notes
9. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
10. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

15.3 Power Peripheral Low Side N-Channel FET

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-4. Low Side N-Channel FET DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DS}	Operating drain to source voltage	–	–	32	V	
$V_{DS,INST}$	Instantaneous drain source voltage	–	–	36	V	
I_D	Average drain current	– –	– –	1 0.5	A A	CY8CLED04/3/2/1D01 devices CY8CLED04/3D02 devices
I_{DMAX}	Maximum instantaneous repetitive pulsed current	– –	– –	3 1.5	A A	Less than 33% duty cycle for an average current of 1 A, f_{SW} = 0.1 MHz. CY8CLED04/3/2/1D01 devices Less than 33% duty cycle for an average current of 0.5 A, f_{SW} = 0.1 MHz. CY8CLED04/3D02 devices
$R_{DS(ON)}$	Drain to source ON resistance	– –	– –	0.5 1	Ω Ω	I_D = 1 A, GDV_{DD} = 5 V, T_J = 25 °C CY8CLED04/3/2/1D01 devices I_D = 0.5 A, GDV_{DD} = 5 V, T_J = 25 °C CY8CLED04/3D02 devices
I_{DSS}	Switching node to PGND leakage	– –	– –	10 250	µA µA	T_J = 25 °C T_J = 115 °C (Industrial rated) and T_J = 125 °C (Extended Temperature rated)
I_{SFET}	Supply current per channel - FET (internal gate driver)	–	–	6.25	mA	f_{SW} = 2 MHz

Table 15-5. Low Side N-Channel FET AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_R	Rise time	–	–	20	ns	I_D = 1 A, R_D = 32 Ω
t_F	Fall time	–	–	20	ns	I_D = 1 A, R_D = 32 Ω

Figure 15-2. Low Side N-Channel FET Test Circuit for I_{DSS}, $t_{R, and}$ t_F

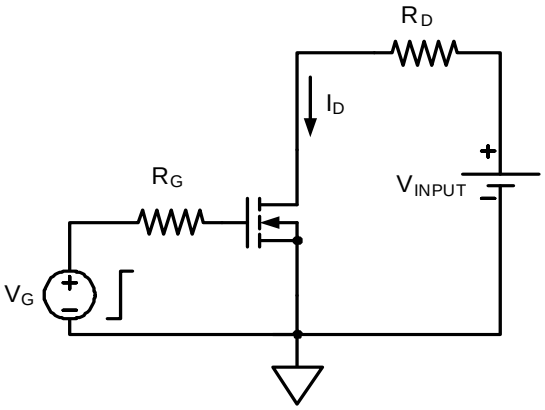


Table 15-9. Hysteretic Controller AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ON} / t_{OFF}	Minimum ON/OFF timer					
	MONOSHOT<1:0> = 00	10	–	30	ns	
	MONOSHOT<1:0> = 01	20	–	60	ns	
	MONOSHOT<1:0> = 10	40	–	110	ns	
	MONOSHOT<1:0> = 11	–	–	–	ns	Timers disabled

15.6 Power Peripheral Comparator

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-10. Comparator DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{IN}	Input voltage range	0	–	V_{DD}	V	–
V_{IO}	Comparator input offset voltage	– – –	– – –	7.5 10 15	mV mV mV	1 V ≤ V_{ICM} ≤ 3 V (Industrial rated) 1 V ≤ V_{ICM} ≤ 3 V (Extended Temperature rated) 0 V ≤ V_{ICM} ≤ V_{DD}
V_{HYS}	Hysteresis voltage	2.5 4.5 4.5	– – –	30 11 13	mV mV mV	0 V < V_{ICM} < V_{DD} 1.5 V ≤ V_{ICM} ≤ 2.5 V (Industrial rated) 1.5 V ≤ V_{ICM} ≤ 2.5 V (Extended Temperature rated)
V_{OVDRV}	Overdrive voltage	5	–	–	mV	–
I_{SCOMP}	Supply current - comparator	–	–	650	µA	–
$V_{ICM,COMP}$	Comparator input common mode voltage range	0	–	V_{DD}	V	–

Table 15-11. Comparator AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_D	Comparator delay time (FN0[x] pin to FN0[x] pin)	–	150	–	ns	V_{OVDRV} = 5 mV, C_L = 10 pF at V_{DD} = 5 V

Figure 15-3. Comparator Timing Diagram

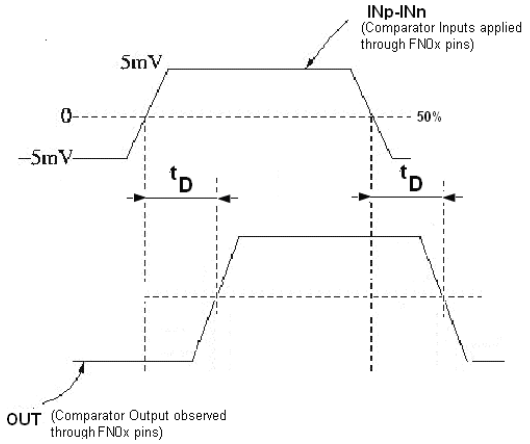


Table 15-24. Operational Amplifier AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROA}	Rising settling time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = low, opamp bias = low Power = medium, opamp bias = high Power = high, opamp bias = high	 – – –	 – – –	 3.9 0.72 0.62	 µs µs µs	–
t_{SOA}	Falling settling time from 20% of ΔV to 0.1% of ΔV (10 pF load, unity gain) Power = low, opamp bias = low Power = medium, opamp bias = high Power = high, opamp bias = high	 – – –	 – – –	 5.9 0.92 0.72	 µs µs µs	–
SR_{ROA}	Rising slew rate (20% to 80%) (10 pF load, unity gain) Power = low, opamp bias = low Power = medium, opamp bias = high Power = high, opamp bias = high	 0.15 1.7 6.5	 – – –	 – – –	 V/µs V/µs V/µs	–
SR_{FOA}	Falling slew rate (20% to 80%) (10 pF load, unity gain) Power = low, opamp bias = low Power = medium, opamp bias = high Power = high, opamp bias = high	 0.01 0.5 4.0	 – – –	 – – –	 V/µs V/µs V/µs	–
BW_{OA}	Gain bandwidth product Power = low, opamp bias = low Power = medium, opamp bias = high Power = high, opamp bias = high	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz	–
E_{NOA}	Noise at 1 kHz (power = medium, opamp bias = high)	–	100	–	nV/r-Hz	–

15.13 PSoC Core Low Power Comparator

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-25. Low Power Comparator DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	$V_{DD} - 1$	V	–
I_{SLPC}	LPC supply current	–	10	40	µA	–
V_{OSLPC}	LPC voltage offset	–	2.5	40	mV	–

Table 15-26. Low Power Comparator AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RLPC}	LPC response time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}.

Table 15-28. Analog Output Buffer AC Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
SR_{ROB}	Rising slew rate (20% to 80%), 1 V step, 100 pF load					–
	Power = low	0.65	–	–	V/µs	
	Power = high	0.65	–	–	V/µs	
SR_{FOB}	Falling slew rate (80% to 20%), 1 V step, 100 pF load					–
	Power = low	0.65	–	–	V/µs	
	Power = high	0.65	–	–	V/µs	
BW_{OBSS}	Small signal bandwidth, 20 mV_{pp}, 3 dB BW, 100 pF load					–
	Power = low	0.8	–	–	MHz	
	Power = high	0.8	–	–	MHz	
BW_{OBLS}	Large signal bandwidth, 1 V_{pp}, 3 dB BW, 100 pF load					–
	Power = low	300	–	–	kHz	
	Power = high	300	–	–	kHz	

15.17 PSoC Core POR and LVD

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the *PowerPSoC Technical Reference Manual* for more information on the VLT_CR register.

Table 15-31. POR and LVD DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PPOR2}	V_{DD} Value for PPOR Trip PORLEV[1:0] = 10b	–	4.55	4.70	V	–
	V_{DD} Value for LVD Trip					–
V_{LVD6}	VM[2:0] = 110b	4.62	4.73	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.81	4.95	V	

15.18 PSoC Core Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-32. Programming DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDP}	Supply current during programming or verify	–	15	30	mA	–
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	–
V_{IHP}	Input high voltage during programming or verify	2.1	–	–	V	–
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull down resistor.
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	–
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	–
$Flash_{ENPB}$	Flash endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[17]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention[18]	10	–	–	Years	–

Notes
17. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36 x 1 blocks of 50,000 maximum cycles each, 36 x 2 blocks of 25,000 maximum cycles each, or 36 x 4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36 x 50,000 and that no single block ever sees more than 50,000 cycles)
18. Guaranteed for –40 °C ≤ T_A ≤ 85 °C for Industrial rated devices and –40 °C ≤ T_A ≤ 105 °C for Extended Temperature rated devices.

Table 15-33. Programming AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RSCLK}	Rise time of SCLK	1	–	20	ns	–
t_{FSCLK}	Fall time of SCLK	1	–	20	ns	–
t_{SSCLK}	Data set up time to falling edge of SCLK	40	–	–	ns	–
t_{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	–
f_{SCLK}	Frequency of SCLK	0	–	8	MHz	–
t_{ERASEB}	Flash erase time (block)	–	10	–	ms	–
t_{WRITE}	Flash block write time	–	40	–	ms	–
t_{DSCLK}	Data out delay from falling edge of SCLK	–	–	50	ns	–
$t_{ERASEALL}$	Flash erase time (bulk)	–	40	–	ms	Erase all blocks and protection fields immediately
$t_{PROGRAM\_HOT}$	Flash block erase + flash block write time	–	–	100[19]	ms	0 °C ≤ Tj ≤ 100 °C
$t_{PROGRAM\_COLD}$	Flash block erase + flash block write time	–	–	200[19]	ms	–40 °C ≤ Tj ≤ 0 °C

15.19 PSoC Core Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \le 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \le 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-34. Digital Block AC Specifications

Function	Description	Min	Typ	Max	Units	Notes
Timer	Capture pulse width	50[20]	–	–	ns	–
	Input frequency, no capture	–	–	49.92	MHz	–
	Input frequency, with capture	–	–	24.96	MHz	–
Counter	Enable pulse width	50[20]	–	–	ns	–
	Input frequency, no enable input	–	–	49.92	MHz	–
	Input frequency, enable input	–	–	24.96	MHz	–
Dead Band	Kill pulse width:					–
	Asynchronous restart mode	20	–	–	ns	–
	Synchronous restart mode	50[20]	–	–	ns	–
	Disable mode	50[20]	–	–	ns	–
	Input frequency	–	–	49.92	MHz	–
CRCPRS (PRS Mode)	Input clock frequency	–	–	49.92	MHz	–
CRCPRS (CRC Mode)	Input clock frequency	–	–	24.96	MHz	–
SPIM	Input clock frequency	–	–	8.32	MHz	Maximum data rate at 4.1 MHz due to 2 x over clocking.
SPIS	Input clock frequency	–	–	4.16	MHz	–
	Width of SS_ Negated between transmissions	50[20]	–	–	ns	–
Transmitter	Input clock frequency	–	–	24.96	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
	Input clock frequency with $V_{DD} \ge 4.75$ V, 2 stop bits	–	–	49.92	MHz	Maximum data rate at 6.15 MHz due to 8 x over clocking.
Receiver	Input clock frequency	–	–	24.96	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
	Input clock frequency with $V_{DD} \ge 4.75$ V, 2 stop bits	–	–	49.92	MHz	Maximum data rate at 6.15 MHz due to 8 x over clocking.

Notes
19. For the full industrial range, you must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.
20. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

18. Acronyms

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CSA	current sense amplifier
CT	continuous time
DAC	digital-to-analog converter
DALI	digital addressable lighting interface
DC	direct current
DMM	delta sigma modulation mode
DMX	digital multiplexing
DSM	delta sigma modulator
DTMF	dual-tone multi frequency
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
FAQ	frequently asked questions
FET	field effect transistor
FSR	full scale range
GPIO	general purpose i/o
GUI	graphical user interface
HBM	human body model
IC	integrated circuit
ICE	in-circuit emulator
IDE	integrated development environment
ILO	internal low-speed oscillator
IMO	internal main oscillator
ISSP	in-system serial programming
I/O	input/output
IPOR	imprecise power on reset
LED	light emitting diode
LSB	least-significant bit
LVD	low voltage detect
MCU	microcontroller
MOSFET	metal-oxide-semiconductor field effect transistor
MSB	most-significant bit
OCD	on chip debugger
PC	program counter
POR	power on reset
PPOR	precision power on reset
PowerPSoC	power programmable system-on-chip™
PrISM	precise intensity signal modulation
PSoC	programmable system-on-chip™
PWM	pulse width modulator
QFN	quad flat no leads package
RGBA	red, green, blue, amber
RGGB	red, green, green, blue
SAR	successive approximation register
SC	switched capacitor
SCL	serial I^2C
SCLK	serial issp clock
SDA	serial i^2c data
SDATA	serial issp data
SPI	serial peripheral interface
SRAM	static random access memory
TRM	technical reference manual
UART	universal asynchronous receiver/transmitter
USB	universal serial bus
WDT	watch dog timer

19. Document Conventions

19.1 Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibels
Hz	Hertz
pp	peak-to-peak
σ	sigma:one standard deviation
V	volt
Ω	ohm
KB	1024 bytes
ppm	parts per million
sps	samples per second
W	watt
A	ampere
Kbit	1024 bits
KHz	kilohertz
KΩ	kilohm
MHz	megahertz
MΩ	megaohm
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µVrms	microvolts root-mean-square

Symbol	Unit of Measure
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
mW	milliwatt
nA	nanoampere
ns	nanosecond
nV	nanovolt
pA	picoampere
pF	picofarads
ps	picoseconds
fF	femtofarad

21. Sales, Solutions, and Legal Information

21.1 Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC® Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Community | Forums | Blogs | Video | Training

Technical Support

cypress.com/go/support

© Cypress Semiconductor Corporation, 2008-2015. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

PSoC Designer™, Programmable System-on-Chip™, and PrISM™ are trademarks and PSoC® and, PowerPSoC® are registered trademarks of Cypress Semiconductor Corp. All other trademarks or registered trademarks referenced herein are property of the respective corporations.