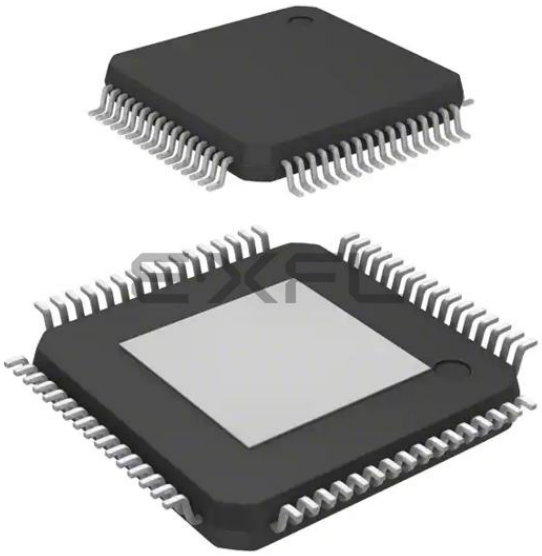
Infineon Technologies - XC2336B40F80LAAKXUMA1 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	34K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-64-6
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2336b40f80laakxuma1

16/32-Bit

Architecture

XC2336B

16/32-Bit Single-Chip Microcontroller
with 32-Bit Performance
XC2000 Family / Value Line

Data Sheet

V1.5 2014-06

Microcontrollers

Table of Contents

16/32-Bit Single-Chip Microcontroller with 32-Bit Performance

XC2336B (XC2000 Family)

1 Summary of Features

For a quick overview and easy reference, the features of the XC2336B are summarized here.

- High-performance CPU with five-stage pipeline and MPU
  - 12.5 ns instruction cycle @ 80 MHz CPU clock (single-cycle execution)
  - One-cycle 32-bit addition and subtraction with 40-bit result
  - One-cycle multiplication (16 × 16 bit)
  - Background division (32 / 16 bit) in 21 cycles
  - One-cycle multiply-and-accumulate (MAC) instructions
  - Enhanced Boolean bit manipulation facilities
  - Zero-cycle jump execution
  - Additional instructions to support HLL and operating systems
  - Register-based design with multiple variable register banks
  - Fast context switching support with two additional local register banks
  - 16 Mbytes total linear address space for code and data
  - 1,024 Bytes on-chip special function register area (C166 Family compatible)
  - Integrated Memory Protection Unit (MPU)
- Interrupt system with 16 priority levels providing 96 interrupt nodes
  - Selectable external inputs for interrupt generation and wake-up
  - Fastest sample-rate 12.5 ns
- Eight-channel interrupt-driven single-cycle data transfer with Peripheral Event Controller (PEC), 24-bit pointers cover total address space
- Clock generation from internal or external clock sources, using on-chip PLL or prescaler
- Hardware CRC-Checker with Programmable Polynomial to Supervise On-Chip Memory Areas
- On-chip memory modules
  - 8 Kbytes on-chip stand-by RAM (SBRAM)
  - 2 Kbytes on-chip dual-port RAM (DPRAM)
  - Up to 16 Kbytes on-chip data SRAM (DSRAM)
  - Up to 16 Kbytes on-chip program/data SRAM (PSRAM)
  - Up to 320 Kbytes on-chip program memory (Flash memory)
  - Memory content protection through Error Correction Code (ECC)

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
43	P10.3	O0 / I	St/B	**Bit 3 of Port 10, General Purpose Input/Output**
	CCU60_COUT60	O2	St/B	**CCU60 Channel 0 Output**
	U0C0_DX2A	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2A	I	St/B	**USIC0 Channel 1 Shift Control Input**
44	P10.4	O0 / I	St/B	**Bit 4 of Port 10, General Purpose Input/Output**
	U0C0_SELO3	O1	St/B	**USIC0 Channel 0 Select/Control 3 Output**
	CCU60_COUT61	O2	St/B	**CCU60 Channel 1 Output**
	U0C0_DX2B	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2B	I	St/B	**USIC0 Channel 1 Shift Control Input**
	ESR1_9	I	St/B	**ESR1 Trigger Input 9**
45	P10.5	O0 / I	St/B	**Bit 5 of Port 10, General Purpose Input/Output**
	U0C1_SCLKOUT	O1	St/B	**USIC0 Channel 1 Shift Clock Output**
	CCU60_COUT62	O2	St/B	**CCU60 Channel 2 Output**
	U0C1_DX1B	I	St/B	**USIC0 Channel 1 Shift Clock Input**
46	P10.6	O0 / I	St/B	**Bit 6 of Port 10, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	U1C0_SELO0	O3	St/B	**USIC1 Channel 0 Select/Control 0 Output**
	U0C0_DX0C	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U1C0_DX2D	I	St/B	**USIC1 Channel 0 Shift Control Input**
	CCU60_CTRAPA	I	St/B	**CCU60 Emergency Trap Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
53	P10.10	O0 / I	St/B	**Bit 10 of Port 10, General Purpose Input/Output**
	U0C0_SELO 0	O1	St/B	**USIC0 Channel 0 Select/Control 0 Output**
	CCU60_COU T63	O2	St/B	**CCU60 Channel 3 Output**
	U0C0_DX2C	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX1A	I	St/B	**USIC0 Channel 1 Shift Clock Input**
	TDI_B	IH	St/B	**JTAG Test Data Input** If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.
54	P10.11	O0 / I	St/B	**Bit 11 of Port 10, General Purpose Input/Output**
	U1C0_SCLK OUT	O1	St/B	**USIC1 Channel 0 Shift Clock Output**
	$\overline{\text{BRKOUT}}$	O2	St/B	**OCDS Break Signal Output**
	U1C0_DX1D	I	St/B	**USIC1 Channel 0 Shift Clock Input**
	TMS_B	IH	St/B	**JTAG Test Mode Selection Input** If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.
55	P10.12	O0 / I	St/B	**Bit 12 of Port 10, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	TDO_B	OH / IH	St/B	**JTAG Test Data Output / DAP1 Input/Output** If DAP pos. 1 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	U1C0_DX0C	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX1E	I	St/B	**USIC1 Channel 0 Shift Clock Input**
56	P10.13	O0 / I	St/B	**Bit 13 of Port 10, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	U1C0_SELO 3	O3	St/B	**USIC1 Channel 0 Select/Control 3 Output**
	U1C0_DX0D	I	St/B	**USIC1 Channel 0 Shift Data Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
6	V_{DDIM}	-	PS/M	**Digital Core Supply Voltage for Domain M** Decouple with a ceramic capacitor, see Data Sheet for details.
24, 41, 57	V_{DDI1}	-	PS/1	**Digital Core Supply Voltage for Domain 1** Decouple with a ceramic capacitor, see Data Sheet for details. All V_{DDI1} pins must be connected to each other.
9	V_{DDPA}	-	PS/A	**Digital Pad Supply Voltage for Domain A** Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. *Note: The A/D_Converters and ports P5, P6 and P15 are fed from supply voltage V_{DDPA}.*
2, 16, 18, 32, 34, 48, 50, 64	V_{DDPB}	-	PS/B	**Digital Pad Supply Voltage for Domain B** Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. *Note: The on-chip voltage regulators and all ports except P5, P6 and P15 are fed from supply voltage V_{DDPB}.*
1, 17, 33, 49	V_{SS}	-	PS/--	**Digital Ground** All V_{SS} pins must be connected to the ground-line or ground-plane. *Note: Also the exposed pad is connected internally to V_{SS}. To improve the EMC behavior, it is recommended to connect the exposed pad to the board ground.* *For thermal aspects, please refer to the Data Sheet. Board layout examples are given in an application note.*

3.1 Memory Subsystem and Organization

The memory space of the XC2336B is configured in the von Neumann architecture. In this architecture all internal and external resources, including code memory, data memory, registers and I/O ports, are organized in the same linear address space.

Table 8 XC2336B Memory Map [1)]

Address Area	Start Loc.	End Loc.	Area Size[2)]	Notes
IMB register space	FF'FF00$_H$	FF'FFFF$_H$	256 Bytes	
Reserved	F0'0000$_H$	FF'FEFF$_H$	< 1 Mbyte	Minus IMB registers
Reserved for EPSRAM	E8'4000$_H$	EF'FFFF$_H$	496 Kbytes	Mirrors EPSRAM
Emulated PSRAM	E8'0000$_H$	E8'3FFF$_H$	up to 16 Kbytes	With Flash timing
Reserved for PSRAM	E0'4000$_H$	E7'FFFF$_H$	496 Kbytes	Mirrors PSRAM
PSRAM	E0'0000$_H$	E0'3FFF$_H$	up to 16 Kbytes	Program SRAM
Reserved for Flash	C5'0000$_H$	DF'FFFF$_H$	1,728 Kbytes	
Flash 1	C4'0000$_H$	C4'FFFF$_H$	64 Kbytes	
Flash 0	C0'0000$_H$	C3'FFFF$_H$	256 Kbytes[3)]	Minus res. seg.
External memory area	40'0000$_H$	BF'FFFF$_H$	8 Mbytes	
External IO area[4)]	21'0000$_H$	3F'FFFF$_H$	1,984 Kbytes	
Reserved	20'BC00$_H$	20'FFFF$_H$	17 Kbytes	
USIC0–2 alternate regs.	20'B000$_H$	20'BBFF$_H$	3 Kbytes	Accessed via EBC
MultiCAN alternate regs.	20'8000$_H$	20'AFFF$_H$	12 Kbytes	Accessed via EBC
Reserved	20'5800$_H$	20'7FFF$_H$	10 Kbytes	
USIC0–2 registers	20'4000$_H$	20'57FF$_H$	6 Kbytes	Accessed via EBC
Reserved	20'6800$_H$	20'7FFF$_H$	6 Kbytes	
MultiCAN registers	20'0000$_H$	20'3FFF$_H$	16 Kbytes	Accessed via EBC
External memory area	01'0000$_H$	1F'FFFF$_H$	1984 Kbytes	
SFR area	00'FE00$_H$	00'FFFF$_H$	0.5 Kbytes	
Dualport RAM (DPRAM)	00'F600$_H$	00'FDFF$_H$	2 Kbytes	
Reserved for DPRAM	00'F200$_H$	00'F5FF$_H$	1 Kbytes	
ESFR area	00'F000$_H$	00'F1FF$_H$	0.5 Kbytes	
XSFR area	00'E000$_H$	00'EFFF$_H$	4 Kbytes	
Data SRAM (DSRAM)	00'A000$_H$	00'DFFF$_H$	16 Kbytes	

to a dedicated vector table location). The occurrence of a hardware trap is also indicated by a single bit in the trap flag register (TFR). Unless another higher-priority trap service is in progress, a hardware trap will interrupt any ongoing program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Depending on the package option up to 3 External Service Request (ESR) pins are provided. The ESR unit processes their input values and allows to implement user controlled trap functions (System Requests SR0 and SR1). In this way reset, wakeup and power control can be efficiently realized.

Software interrupts are supported by the 'TRAP' instruction in combination with an individual trap (interrupt) number. Alternatively to emulate an interrupt by software a program can trigger interrupt requests by writing the Interrupt Request (IR) bit of an interrupt control register.

3.6 On-Chip Debug Support (OCDS)

The On-Chip Debug Support system built into the XC2336B provides a broad range of debug and emulation features. User software running on the XC2336B can be debugged within the target system environment.

The OCDS is controlled by an external debugging device via the debug interface. This either consists of the 2-pin Device Access Port (DAP) or of the JTAG port conforming to IEEE-1149. The debug interface can be completed with an optional break interface.

The debugger controls the OCDS with a set of dedicated registers accessible via the debug interface (DAP or JTAG). In addition the OCDS system can be controlled by the CPU, e.g. by a monitor program. An injection interface allows the execution of OCDS-generated instructions by the CPU.

Multiple breakpoints can be triggered by on-chip hardware, by software, or by an external trigger input. Single stepping is supported, as is the injection of arbitrary instructions and read/write access to the complete internal address space. A breakpoint trigger can be answered with a CPU halt, a monitor call, a data transfer, or/and the activation of an external signal.

Tracing of data can be obtained via the debug interface, or via the external bus interface for increased performance.

Tracing of program execution is supported by the XC2000 Family emulation device. With this device the DAP can operate on clock rates of up to 20 MHz.

The DAP interface uses two interface signals, the JTAG interface uses four interface signals, to communicate with external circuitry. The debug interface can be amended with two optional break lines.

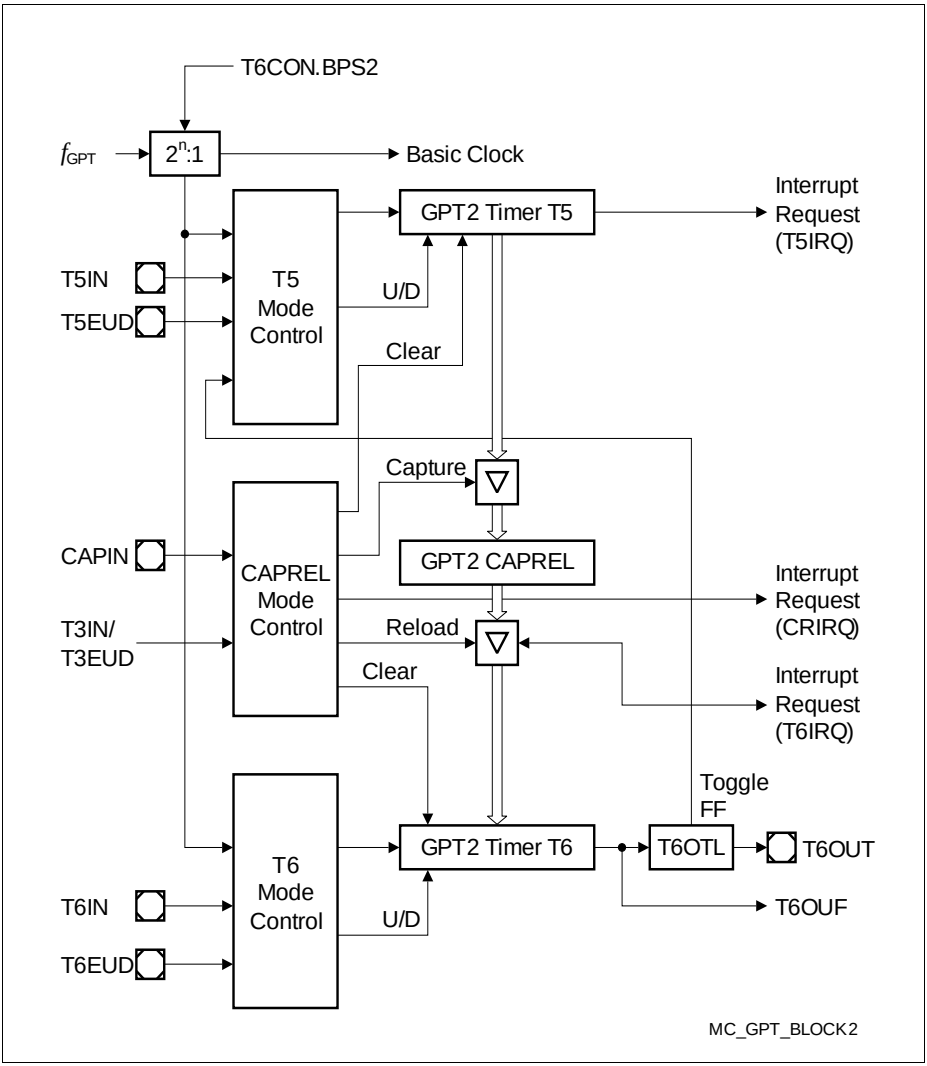


Figure 9 Block Diagram of GPT2

3.12 Universal Serial Interface Channel Modules (USIC)

The XC2336B features the USIC modules USIC0, USIC1. Each module provides two serial communication channels.

The Universal Serial Interface Channel (USIC) module is based on a generic data shift and data storage structure which is identical for all supported serial communication protocols. Each channel supports complete full-duplex operation with a basic data buffer structure (one transmit buffer and two receive buffer stages). In addition, the data handling software can use FIFOs.

The protocol part (generation of shift clock/data/control signals) is independent of the general part and is handled by protocol-specific preprocessors (PPPs).

The USIC's input/output lines are connected to pins by a pin routing unit. The inputs and outputs of each USIC channel can be assigned to different interface pins, providing great flexibility to the application software. All assignments can be made during runtime.

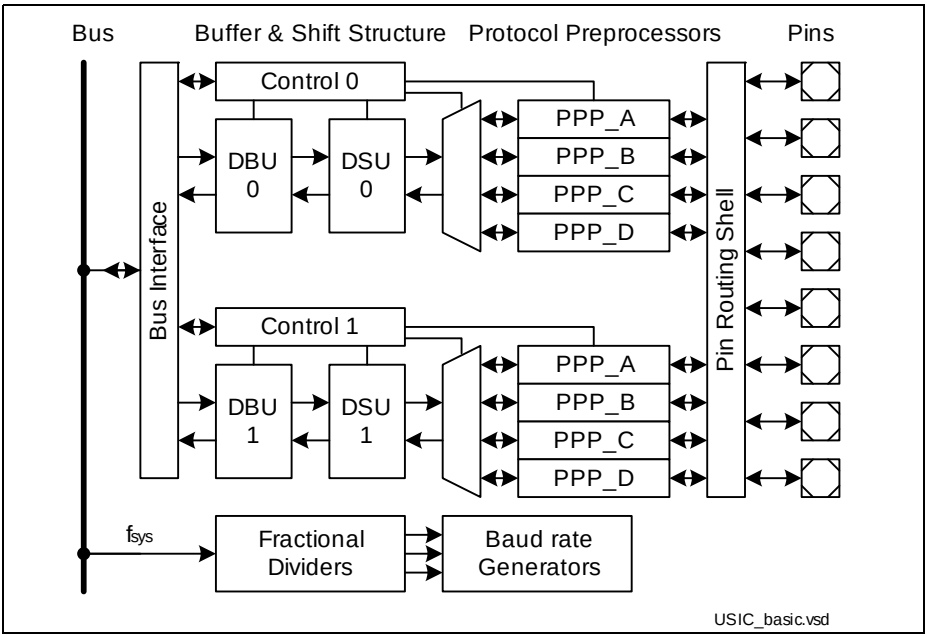


Figure 11 General Structure of a USIC Module

The regular structure of the USIC module brings the following advantages:

- Higher flexibility through configuration with same look-and-feel for data management
- Reduced complexity for low-level drivers serving different protocols
- Wide range of protocols with improved performances (baud rate, buffer handling)

Target Protocols

Each USIC channel can receive and transmit data frames with a selectable data word width from 1 to 16 bits in each of the following protocols:

- **UART** (asynchronous serial channel)
  - module capability: maximum baud rate = f_{SYS} / 4
  - data frame length programmable from 1 to 63 bits
  - MSB or LSB first
- **LIN** Support (Local Interconnect Network)
  - module capability: maximum baud rate = f_{SYS} / 16
  - checksum generation under software control
  - baud rate detection possible by built-in capture event of baud rate generator
- **SSC/SPI** (synchronous serial channel with or without data buffer)
  - module capability: maximum baud rate = f_{SYS} / 2, limited by loop delay
  - number of data bits programmable from 1 to 63, more with explicit stop condition
  - MSB or LSB first
  - optional control of slave select signals
- **IIC** (Inter-IC Bus)
  - supports baud rates of 100 kbit/s and 400 kbit/s
- **IIS** (Inter-IC Sound Bus)
  - module capability: maximum baud rate = f_{SYS} / 2

Note: Depending on the selected functions (such as digital filters, input synchronization stages, sample point adjustment, etc.), the maximum achievable baud rate can be limited. Please note that there may be additional delays, such as internal or external propagation delays and driver delays (e.g. for collision detection in UART mode, for IIC, etc.).

3.17 Parallel Ports

The XC2336B provides up to 40 I/O lines which are organized into 4 input/output ports and 2 input ports. All port lines are bit-addressable, and all input/output lines can be individually (bit-wise) configured via port control registers. This configuration selects the direction (input/output), push/pull or open-drain operation, activation of pull devices, and edge characteristics (shape) and driver characteristics (output current) of the port drivers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. During the internal reset, all port pins are configured as inputs without pull devices active.

All port lines have alternate input or output functions associated with them. These alternate functions can be programmed to be assigned to various port pins to support the best utilization for a given application. For this reason, certain functions appear several times in **Table 10**.

All port lines that are not used for alternate functions may be used as general purpose I/O lines.

Table 10 Summary of the XC2336B's Ports

Port	Width	I/O	Connected Modules
P2	11	I/O	CAN, CC2, GPT12E, USIC, DAP/JTAG
P5	7	I	Analog Inputs, CCU6, DAP/JTAG, GPT12E, CAN
P6	2	I/O	ADC, CAN, GPT12E
P7	1	I/O	CAN, GPT12E, SCU, DAP/JTAG, USIC
P10	16	I/O	CCU6, USIC, DAP/JTAG, CAN
P15	2	I	Analog Inputs, GPT12E

Table 13 Operating Conditions (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload current coupling factor for digital I/O pins	K_{OVD} CC	–	1.0 x 10^{-2}	3.0 x 10^{-2}	-	I_{OV}< 0 mA; not subject to production test
		–	1.0 x 10^{-4}	5.0 x 10^{-3}	-	I_{OV}> 0 mA; not subject to production test
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$ SR	–	–	50	mA	not subject to production test
Digital core supply voltage for domain M[8)]	V_{DDIM} CC	–	1.5	–		
Digital core supply voltage for domain 1[8)]	V_{DDI1} CC	–	1.5	–		
Digital supply voltage for IO pads and voltage regulators	V_{DDP} SR	3.0	–	5.5	V	
Digital ground voltage	V_{SS} SR	–	0	–	V	

1) To ensure the stability of the voltage regulators the EVRs must be buffered with ceramic capacitors. Separate buffer capacitors with the recomended values shall be connected as close as possible to each V_{DDIM} and V_{DDI1} pin to keep the resistance of the board tracks below 2 Ohm. Connect all V_{DDI1} pins together. The minimum capacitance value is required for proper operation under all conditions (e.g. temperature). Higher values slightly increase the startup time.

2) Use one Capacitor for each pin.

3) This is the reference load. For bigger capacitive loads, use the derating factors listed in the pad properties section.

4) The timing is valid for pin drivers operating in default current mode (selected after reset). Reducing the output current may lead to increased delays or reduced driving capability (C_L).

5) The operating frequency range may be reduced for specific device types. This is indicated in the device designation (...FxxL). 80 MHz devices are marked ...F80L.

6) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: $V_{OV} > V_{IHmax}$ ($I_{OV} > 0$) or $V_{OV} < V_{ILmin}$ (($I_{OV} < 0$). The absolute sum of input overload currents on all pins may not exceed 50 mA. The supply voltages must remain within the specified limits. Proper operation under overload conditions depends on the application. Overload conditions must not occur on pin XTAL1 (powered by V_{DDIM}).

7) An overload current (I_{OV}) through a pin injects a certain error current (I_{INJ}) into the adjacent pins. This error current adds to the respective pins leakage current (I_{OZ}). The amount of error current depends on the overload current and is defined by the overload coupling factor K_{OV}. The polarity of the injected error current is inverse compared to the polarity of the overload current that produces it.The total current through a pin is $|I_{TOT}| = |I_{OZ}| + (|I_{OV}| \ K_{OV})$. The additional error current may distort the input voltage on analog inputs.

8) Value is controlled by on-chip regulator

4.2 Voltage Range definitions

The XC2336B timing depends on the supply voltage. If such a dependency exists the timing values are given for 2 voltage areas commonly used. The voltage areas are defined in the following tables.

Table 14 Upper Voltage Range Definition

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage for IO pads and voltage regulators	V_{DDP} SR	4.5	5	5.5	V	

Table 15 Lower Voltage Range Definition

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage for IO pads and voltage regulators	V_{DDP} SR	3.0	3.3	4.5	V	

4.2.1 Parameter Interpretation

The parameters listed in the following include both the characteristics of the XC2336B and its demands on the system. To aid in correctly interpreting the parameters when evaluating them for a design, they are marked accordingly in the column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the XC2336B provides signals with the specified characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the specified characteristics to the XC2336B.

4.4 Analog/Digital Converter Parameters

These parameters describe the conditions for optimum ADC performance.

Note: Operating Conditions apply.

Table 20 ADC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switched capacitance at an analog input	C_{AINSW} CC	–	–	4	pF	not subject to production test [1]
Total capacitance at an analog input	C_{AINT} CC	–	–	10	pF	not subject to production test [1]
Switched capacitance at the reference input	C_{AREFSW} CC	–	–	7	pF	not subject to production test [1]
Total capacitance at the reference input	C_{AREFT} CC	–	–	15	pF	not subject to production test [1]
Differential Non-Linearity Error	$\lvert EA_{DNL}\rvert$ CC	–	0.8	1	LSB	
Gain Error	$\lvert EA_{GAIN}\rvert$ CC	–	0.4	0.8	LSB	
Integral Non-Linearity	$\lvert EA_{INL}\rvert$ CC	–	0.8	1.2	LSB	
Offset Error	$\lvert EA_{OFF}\rvert$ CC	–	0.5	0.8	LSB	
Analog clock frequency	f_{ADCI} SR	0.5	–	16.5	MHz	voltage_range= lower
		0.5	–	20	MHz	voltage_range= upper
Input resistance of the selected analog channel	R_{AIN} CC	–	–	2	kOhm	not subject to production test [1]
Input resistance of the reference input	R_{AREF} CC	–	–	2	kOhm	not subject to production test [1]

2) This parameter is tested for the fastest and the slowest selection. The medium selections are not subject to production test - verified by design/characterization
3) f_{WU} in MHz
4) This value includes a hysteresis of approximately 50 mV for rising voltage.
5) V_{LV} = selected SWD voltage level
6) The limit V_{LV} - 0.10 V is valid for the OK1 level. The limit for the OK2 level is V_{LV} - 0.15 V.

Conditions for t_{SPO} Timing Measurement

The time required for the transition from **Power-on** to **Base** mode is called t_{SPO}. It is measured under the following conditions:

Precondition: The pad supply is valid, i.e. V_{DDPB} is above 3.0V and remains above 3.0V even though the XC2336B is starting up. No debugger is attached.

Start condition: Power-on reset is removed ($\overline{\text{PORST}}$ = 1).

End condition: External pin toggle caused by first user instruction executed from FLASH after startup.

Conditions for t_{SSO} Timing Measurement

The time required for the transition from **Stopover** to **Stopover Waked-Up** mode is called t_{SSO}. It is measured under the following conditions:

Precondition: The **Stopover** mode has been entered using the procedure defined in the Programmer's Guide.

Start condition: Pin toggle on $\overline{\text{ESR}}$ pin triggering the startup sequence.

End condition: External pin toggle caused by first user instruction executed from PSRAM after startup.

4.7.2 Definition of Internal Timing

The internal operation of the XC2336B is controlled by the internal system clock f_{SYS}.

Because the system clock signal f_{SYS} can be generated from a number of internal and external sources using different mechanisms, the duration of the system clock periods (TCSs) and their variation (as well as the derived external timing) depend on the mechanism used to generate f_{SYS}. This must be considered when calculating the timing for the XC2336B.

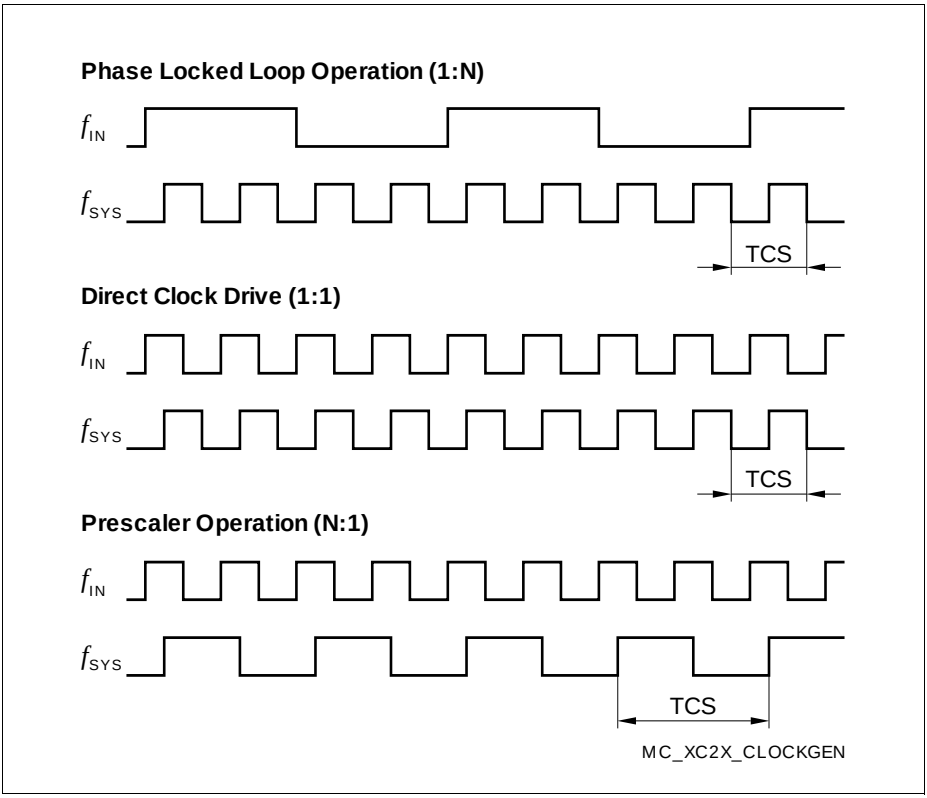


Figure 19 Generation Mechanisms for the System Clock

*Note: The example of PLL operation shown in **Figure 19** uses a PLL factor of 1:4; the example of prescaler operation uses a divider factor of 2:1.*

The specification of the external timing (AC Characteristics) depends on the period of the system clock (TCS).

4.7.3 External Clock Input Parameters

These parameters specify the external clock generation for the XC2336B. The clock can be generated in two ways:

- By connecting a **crystal or ceramic resonator** to pins XTAL1/XTAL2.
- By supplying an **external clock signal**
  - This clock signal can be supplied either to pin XTAL1 (core voltage domain) or to pin CLKIN1 (IO voltage domain).

If connected to CLKIN1, the input signal must reach the defined input levels V_{IL} and V_{IH}. If connected to XTAL1, a minimum amplitude V_{AX1} (peak-to-peak voltage) is sufficient for the operation of the on-chip oscillator.

Note: The given clock timing parameters (t_1 … t_4) are only valid for an external clock input signal.

Note: Operating Conditions apply.

Table 27 External Clock Input Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Oscillator frequency	f_{OSC} SR	4	–	40	MHz	Input= Clock Signal
		4	–	16	MHz	Input= Crystal or Ceramic Resonator
XTAL1 input current absolute value	$\|I_{IL}\|$ CC	–	–	20	µA	
Input clock high time	t_1 SR	6	–	–	ns	
Input clock low time	t_2 SR	6	–	–	ns	
Input clock rise time	t_3 SR	–	8	8	ns	
Input clock fall time	t_4 SR	–	8	8	ns	
Input voltage amplitude on XTAL1[1)]	V_{AX1} SR	0.3 x V_{DDIM}	–	–	V	$f_{OSC} \geq$ 4 MHz; $f_{OSC} <$ 16 MHz
		0.4 x V_{DDIM}	–	–	V	$f_{OSC} \geq$ 16 MHz; $f_{OSC} <$ 25 MHz
		0.5 x V_{DDIM}	–	–	V	$f_{OSC} \geq$ 25 MHz; $f_{OSC} \leq$ 40 MHz
Input voltage range limits for signal on XTAL1	V_{IX1} SR	-1.7 + V_{DDIM}	–	1.7	V	[2)]

4.7.5 Synchronous Serial Interface Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 30 is valid under the following conditions: C_L= 20 pF; *SSC*= master ; voltage_range= upper

Table 30 USIC SSC Master Mode Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	t_{SYS} - 8[1)]	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	t_{SYS} - 6[1)]	–	–	ns	
Data output DOUT valid time	t_3 CC	-6	–	9	ns	
Receive data input setup time to SCLKOUT receive edge	t_4 SR	31	–	–	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-4	–	–	ns	

1) $t_{SYS} = 1 / f_{SYS}$

Table 31 is valid under the following conditions: C_L= 20 pF; *SSC*= master ; voltage_range= lower

4.7.6 Debug Interface Timing

The debugger can communicate with the XC2336B either via the 2-pin DAP interface or via the standard JTAG interface.

Debug via DAP

The following parameters are applicable for communication through the DAP debug interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 34 is valid under the following conditions: C_L= 20 pF; voltage_range= upper

Table 34 DAP Interface Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period[1)]	t_{11} SR	25	–	–	ns	
DAP0 high time	t_{12} SR	8	–	–	ns	
DAP0 low time[1)]	t_{13} SR	8	–	–	ns	
DAP0 clock rise time	t_{14} SR	–	–	4	ns	
DAP0 clock fall time	t_{15} SR	–	–	4	ns	
DAP1 setup to DAP0 rising edge	t_{16} SR	6	–	–	ns	
DAP1 hold after DAP0 rising edge	t_{17} SR	6	–	–	ns	
DAP1 valid per DAP0 clock period[2)]	t_{19} CC	17	20	–	ns	

1) See the DAP chapter for clock rate restrictions in the Active::IDLE protocol state.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.

Table 35 is valid under the following conditions: C_L= 20 pF; voltage_range= lower