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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Audio Processor
Interface	Host Interface, I²C, SAI, SPI
Clock Rate	100MHz
Non-Volatile Memory	ROM (192kB)
On-Chip RAM	11.25kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=dspb56364af100

1.1 Features

1.1.1 Digital Signal Processing Core

- 100 Million Instructions Per Second (MIPS) with an 100 MHz clock at 3.3V.
- Object Code Compatible with the 56000 core.
- Data ALU with a 24 × 24 bit multiplier-accumulator and a 56-bit barrel shifter. 16-bit arithmetic support.
- Program Control with position independent code support and instruction cache support.
- Six-channel DMA controller.
- PLL based clocking with a wide range of frequency multiplications (1 to 4096), predivider factors (1 to 16) and power saving clock divider (2^i: i = 0 to 7). Reduces clock noise.
- Internal address tracing support and OnCE™ for Hardware/Software debugging.
- JTAG port.
- Very low-power CMOS design, fully static design with operating frequencies down to DC.
- STOP and WAIT low-power standby modes.

1.1.2 On-Chip Memory Configuration

- 1.5K × 24 Bit Y-Data RAM.
- 1K × 24 Bit X-Data RAM.
- 8K × 24 Bit Program ROM.
- 0.5K × 24 Bit Program RAM and 192 × 24 Bit Bootstrap ROM.
- 0.75K × 24 Bit from Y Data RAM can be switched to Program RAM resulting in up to 1.25K × 24 Bit of Program RAM.

1.1.3 Off-Chip Memory Expansion

- External Memory Expansion Port with 8-bit data bus.
- Off-chip expansion up to 2 × 16M × 8-bit word of Data/Program memory when using DRAM.
- Off-chip expansion up to 2 × 256k × 8-bit word of Data/Program memory when using SRAM.
- Simultaneous glueless interface to SRAM and DRAM.

1.1.4 Peripheral Modules

- Enhanced Serial Audio Interface (ESAI): 6 serial lines, 4 selectable as receive or transmit and 2 transmit only, master or slave. I^2S, Sony, AC97, network and other programmable protocols. Unused pins of ESAI may be used as GPIO lines.
- Serial Host Interface (SHI): SPI and I^2C protocols, 10-word receive FIFO, support for 8, 16 and 24-bit words.
- Four dedicated GPIO lines.

1.1.5 Packaging

- 100-pin plastic TQFP package.

1.2 Documentation

Table 1-1 lists the documents that provide a complete description of the DSP56364 and are required to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, a Freescale Literature Distribution Center, or through the Freescale DSP home page on the Internet (the source for the latest information).

Table 1-1 DSP56364 Documentation

Document Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the 56000-family architecture and the 24-bit core processor and instruction set	DSP56300FM
DSP56364 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56364UM
DSP56364 Product Brief	Brief description of the chip	DSP56364P
DSP56364 Technical Data Sheet (this document)	Electrical and timing specifications; pin and package descriptions	DSP56364

Table 3-7 Reset, Stop, Mode Select, and Interrupt Timing[1] (continued)

No.	Characteristics	Expression[2]	Min	Max	Unit
21	Delay from $\overline{WR}$ assertion to interrupt request deassertion for level sensitive fast interrupts[6, 7]				ns
	• DRAM for all WS	$(WS + 3.5) \times T_C - 10.94$	—	—	
	• SRAM WS = 1	$(WS + 3.5) \times T_C - 10.94$	—	—	
	• SRAM WS = 2, 3	$(WS + 3) \times T_C - 10.94$	—	—	
	• SRAM WS ≥ 4	$(WS + 2.5) \times T_C - 10.94$	—	—	
24	Duration for $\overline{IRQA}$ assertion to recover from Stop state		5.9	—	
25	Delay from $\overline{IRQA}$ assertion to fetch of first instruction (when exiting Stop)[3, 8]				
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (OMR Bit 6 = 0)	$PLC \times ET_C \times PDF + (128\ K - PLC/2) \times T_C$	1.3	13.6	ms
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (OMR Bit 6 = 1)	$PLC \times ET_C \times PDF + (23.75 \pm 0.5) \times T_C$	232.5 ns	12.3 ms	
	• PLL is active during Stop (PCTL Bit 17 = 1) (Implies No Stop Delay)	$(8.25 \pm 0.5) \times T_C$	77.5	87.5	ns
26	Duration of level sensitive $\overline{IRQA}$ assertion to ensure interrupt service (when exiting Stop)[3, 8]				
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (OMR Bit 6 = 0)	$PLC \times ET_C \times PDF + (128\ K - PLC/2) \times T_C$	13.6	—	ms
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (OMR Bit 6 = 1)	$PLC \times ET_C \times PDF + (20.5 \pm 0.5) \times T_C$	12.3	—	ms
	• PLL is active during Stop (PCTL Bit 17 = 1) (implies no Stop delay)	$5.5 \times T_C$	55.0	—	ns
27	Interrupt Requests Rate				
	• ESAI, SCI	$12T_C$	—	120.0	ns
	• DMA	$8T_C$	—	80.0	ns
	• $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	$8T_C$	—	80.0	ns
	• $\overline{IRQ}$, $\overline{NMI}$ (level trigger)	$12T_C$	—	120.0	ns
28	DMA Requests Rate				
	• Data read from ESAI, SCI	$6T_C$	—	60.0	ns
	• Data write to ESAI, SCI	$7T_C$	—	70.0	ns
	• $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	$3T_C$	—	30.0	ns

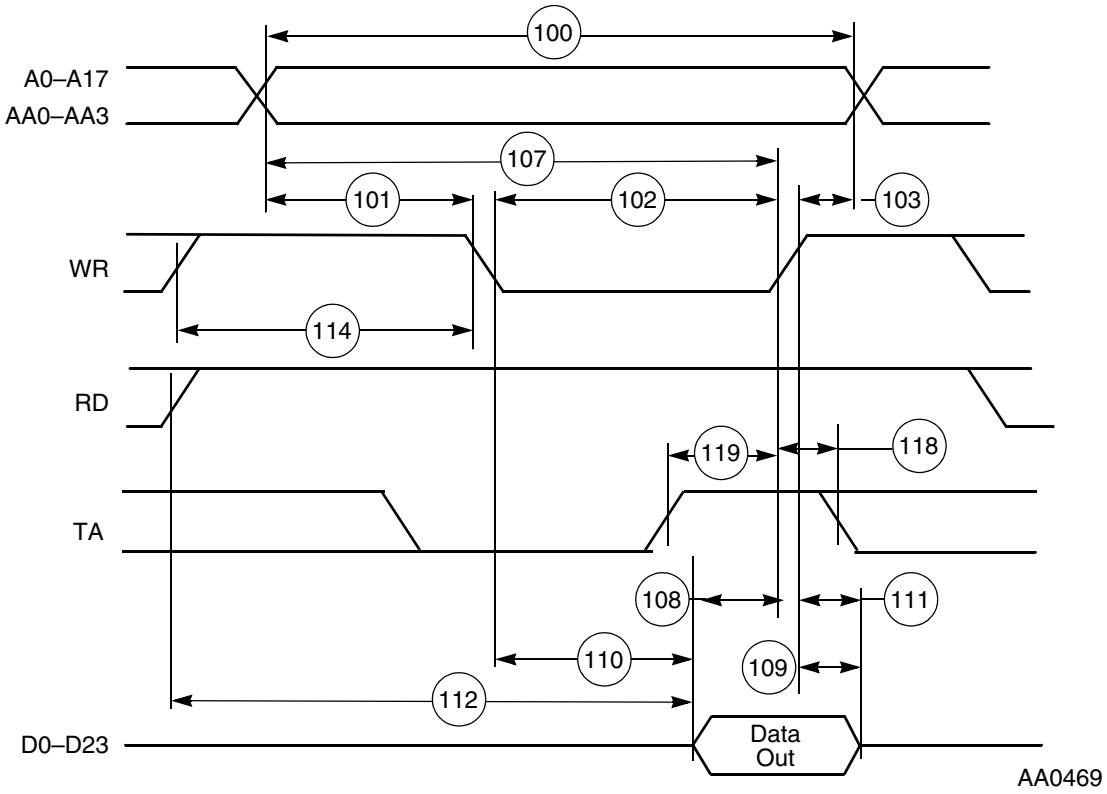


Figure 3-10 SRAM Write Access

3.10.2 DRAM Timing

The selection guides provided in Figure 3-11 and Figure 3-14 should be used for primary selection only. Final selection should be based on the timing provided in the following tables. As an example, the selection guide suggests that 4 wait states must be used for 100 MHz operation when using Page Mode DRAM. However, by using the information in the appropriate table, a designer may choose to evaluate whether fewer wait states might be used by determining which timing prevents operation at 100 MHz, running the chip at a slightly lower frequency (e.g., 95 MHz), using faster DRAM (if it becomes available), and control factors such as capacitive and resistive load to improve overall system performance.

Table 3-11 DRAM Page Mode Timings, Three Wait States[1, 2, 3] (continued)

No.	Characteristics	Symbol	Expression[4]	Min	Max	Unit
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$3.5 \times T_C - 4.0$	31.0	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	$2.5 \times T_C - 7.0$	—	18.0	ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	7.2	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.5	ns

1 The number of wait states for Page mode access is specified in the DCR.

2 The refresh period is specified in the DCR.

3 The asynchronous delays specified in the expressions are valid for DSP56364.

4 All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., tPC equals 4 ¥ TC for read-after-read or write-after-write sequences).

5 BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of page-access.

6 $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

Table 3-12 DRAM Page Mode Timings, Four Wait States[1, 2, 3]

No.	Characteristics	Symbol	Expression[4]	Min	Max	Unit
131	Page mode cycle time for two consecutive accesses of the same direction.	t_{PC}	$2 \times T_C$	50.0	—	ns
	Page mode cycle time for mixed (read and write) accesses.		$1.25 \times T_C$	45.0	—	ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$2.75 \times T_C - 7.0$	—	20.5	ns
133	Column address valid to data valid (read)	t_{AA}	$3.75 \times T_C - 7.0$	—	30.5	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$3.5 \times T_C - 4.0$	31.0	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$6 \times T_C - 4.0$	56.0	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$2.5 \times T_C - 4.0$	21.0	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ assertion[5]					
	• BRW[1:0] = 00	t_{CRP}	$2.75 \times T_C - 6.0$	—	—	ns
	• BRW[1:0] = 01		$4.25 \times T_C - 6.0$	—	—	ns
	• BRW[1:0] = 10		$5.25 \times T_C - 6.0$	46.5	—	ns
	• BRW[1:0] = 11		$7.25 \times T_C - 6.0$	66.5	—	ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$2 \times T_C - 4.0$	16.0	—	ns

Table 3-15 DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1, 2] (continued)

No.	Characteristics[3]	Symbol	Expression[4]	Min	Max	Unit
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$11.5 \times T_C - 4.0$	111.0	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	$10 \times T_C - 7.0$	—	93.0	ns
193	$\overline{RD}$ deassertion to data not valid[3]	t_{GZ}		0.0	—	ns
194	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	7.2	—	ns
195	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.5	ns

1 The number of wait states for out-of-page access is specified in the DCR.
2 The refresh period is specified in the DCR.
3 $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
4 The asynchronous delays specified in the expressions are valid for DSP56364.
5 Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

Table 3-16 DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1, 2]

No.	Characteristics[3]	Symbol	Expression	Min	Max	Unit
157	Random read or write cycle time	t_{RC}	$16 \times T_C$	160.0	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	$8.25 \times T_C - 5.7$	—	76.8	ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$4.75 \times T_C - 5.7$	—	41.8	ns
160	Column address valid to data valid (read)	t_{AA}	$5.5 \times T_C - 5.7$	—	49.3	ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}	0.0	0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$6.25 \times T_C - 4.0$	58.5	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$9.75 \times T_C - 4.0$	93.5	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$6.25 \times T_C - 4.0$	58.5	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$8.25 \times T_C - 4.0$	78.5	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$4.75 \times T_C - 4.0$	43.5	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$3.5 \times T_C \pm 2$	33.0	37.0	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$2.75 \times T_C \pm 2$	25.5	29.5	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$7.75 \times T_C - 4.0$	73.5	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$6.25 \times T_C - 4.0$	58.5	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$6.25 \times T_C - 4.0$	58.5	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$2.75 \times T_C - 4.0$	23.5	—	ns

Table 3-20 Enhanced Serial Audio Interface Timing (continued)

No.	Characteristics[1, 2, 3]	Symbol	Expression	Min	Max	Condition[4]	Unit
443	FSR input hold time after RXC falling edge	—	—	3.0 0.0	— —	x ck i ck a	ns
444	Flags input setup before RXC falling edge	—	—	0.0 19.0	— —	x ck i ck s	ns
445	Flags input hold time after RXC falling edge	—	—	6.0 0.0	— —	x ck i ck s	ns
446	TXC rising edge to FST out (bl) high	—	—	— —	29.0 15.0	x ck i ck	ns
447	TXC rising edge to FST out (bl) low	—	—	— —	31.0 17.0	x ck i ck	ns
448	TXC rising edge to FST out (wr) high[6]	—	—	— —	31.0 17.0	x ck i ck	ns
449	TXC rising edge to FST out (wr) low[6]	—	—	— —	33.0 19.0	x ck i ck	ns
450	TXC rising edge to FST out (wl) high	—	—	— —	30.0 16.0	x ck i ck	ns
451	TXC rising edge to FST out (wl) low	—	—	— —	31.0 17.0	x ck i ck	ns
452	TXC rising edge to data out enable from high impedance	—	—	— —	31.0 17.0	x ck i ck	ns
453	TXC rising edge to transmitter #0 drive enable assertion	—	—	— —	34.0 20.0	x ck i ck	ns
454	TXC rising edge to data out valid	—	$23 + 0.5 \times T_C$ 21.0	— —	28.0 21.0	x ck i ck	ns
455	TXC rising edge to data out high impedance[7]	—	—	— —	31.0 16.0	x ck i ck	ns
456	TXC rising edge to transmitter #0 drive enable deassertion[7]	—	—	— —	34.0 20.0	x ck i ck	ns
457	FST input (bl, wr) setup time before TXC falling edge[6]	—	—	2.0 21.0	— —	x ck i ck	ns
458	FST input (wl) to data out enable from high impedance	—	—	—	27.0	—	ns

4 Packaging

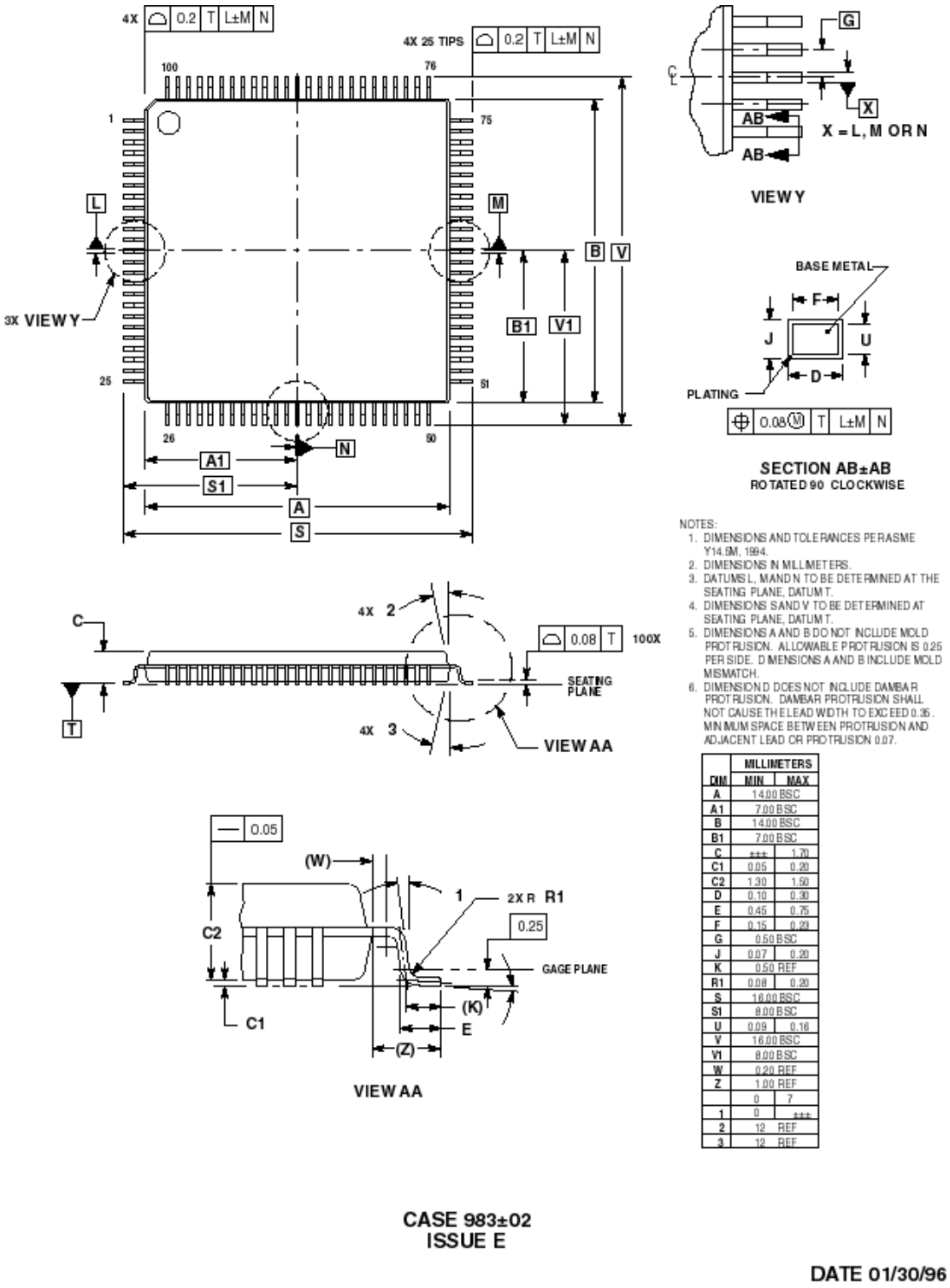
4.1 Pin-Out and Package Information

This section provides information about the available package for this product, including diagrams of the package pinouts and tables describing how the signals described in Section 2, "Signal/Connection Descriptions" are allocated for the package. The DSP56364 is available in a 100-pin TQFP package. Table 4-1 and Table 4-2show the pin/name assignments for the packages.

4.1.1 TQFP Package Description

Top view of the 100-pin TQFP package is shown in Figure 4-1 with its pin-outs. The 100-pin TQFP package mechanical drawing is shown in Figure 4-2.

4.1.2 TQFP Package Mechanical Drawing



NOTES:
1. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT THE SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B INCLUDE MOLD MISMATCH.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

	MILLIMETERS	
DIM	MIN	MAX
A	14.00 BSC	
A1	7.00 BSC	
B	14.00 BSC	
B1	7.00 BSC	
C	---	1.70
C1	0.05	0.20
C2	1.30	1.50
D	0.10	0.30
E	0.45	0.75
F	0.15	0.23
G	0.50 BSC	
J	0.07	0.20
K	0.50 REF	
R1	0.08	0.20
S	16.00 BSC	
S1	8.00 BSC	
U	0.09	0.16
V	16.00 BSC	
V1	8.00 BSC	
W	0.20 REF	
Z	1.00 REF	
	0°	7°
1	0°	---
2	12° REF	
3	12° REF	

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ISSUE E

DATE 01/30/96

Figure 4-2 DSP56364 100-pin TQFP Package

- All inputs must be terminated (i.e., not allowed to float) using CMOS levels, except for the three pins with internal pull-up resistors (TMS, TDI, TCK).
- Take special care to minimize noise levels on the V_{CCP} and GND_P pins.
- If multiple DSP56364 devices are on the same board, check for cross-talk or excessive spikes on the supplies due to synchronous operation of the devices.
- RESET must be asserted when the chip is powered up. A stable EXTAL signal must be supplied before deassertion of RESET.
- At power-up, ensure that the voltage difference between the 5 V tolerant pins and the chip V_{CC} never exceeds 3.95 V.

5.3 Power Consumption Considerations

Power dissipation is a key issue in portable DSP applications. Some of the factors which affect current consumption are described in this section. Most of the current consumed by CMOS devices is alternating current (ac), which is charging and discharging the capacitances of the pins and internal nodes.

Current consumption is described by the following formula:

$$I = C \times V \times f$$

where C = node/pin capacitance
V = voltage swing
f = frequency of node/pin toggle

Example 1. Current Consumption

For a Port A address pin loaded with 50 pF capacitance, operating at 3.3 V, and with a 100 MHz clock, toggling at its maximum possible rate (50 MHz), the current consumption is

$$I = 50 \times 10^{-12} \times 3.3 \times 50 \times 10^{6} = 8.25\,mA$$

The maximum internal current ($I_{CCI}max$) value reflects the typical possible switching of the internal buses on best-case operation conditions, which is not necessarily a real application case. The typical internal current (I_{CCItyp}) value reflects the average switching of the internal buses on typical operating conditions.

For applications that require very low current consumption, do the following:

- Set the EBD bit when not accessing external memory.
- Minimize external memory accesses and use internal memory accesses.
- Minimize the number of pins that are switching.
- Minimize the capacitive load on the pins.
- Connect the unused inputs to pull-up or pull-down resistors.
- Disable unused peripherals.

One way to evaluate power consumption is to use a current per MIPS measurement methodology to minimize specific board effects (i.e., to compensate for measured board current not caused by the DSP).

Appendix A IBIS Model

```
IBIS Model
[IBIS Ver]          3.2
[File name]         56364_e.ibs
[File Rev]          e
[Date]              Feb 13, 2002
[Component]         56364
[Manufacturer]      Freescale SEMI CONDUCTOR Ltd.
[Package]
| variable          typ         min         max
R_pkg               45.0m       22.0m       75.0m
L_pkg               2.5nH       1.1nH       4.3nH
C_pkg               1.3pF       1.2pF       1.4pF
[Pin]       signal_name              model_name   R_pin        L_pin     C_pin
1                irqd_                  ipad5v_io
2                irqb_                  ipad5v_io
3                irqa_                  ipad5v_io
4                fst                    ipad5v_io
5                fsr                    ipad5v_io
6                sckt                   ipad5v_io
7                sckr                   ipad5v_io
8                vccs                   power
9                gnds                   gnd
10               hckt                   ipad5v_io
11               vcclq                  power
12               gndq                   gnd
13               hckr                   ipad5v_io
14               sdo0                   ipad5v_io
15               vcchq                  power
16               sdo1                   ipad5v_io
17               sdo2/sdi3              ipad5v_io
18               sdo3/sdi2              ipad5v_io
19               sdo4/sdi1              ipad5v_io
20               sdo5/sdi0              ipad5v_io
21               vccs                   power
22               gnds                   gnd
23               ss_/ha2                ipad5v_io
24               mosi/ha0               ipad5v_io
25               miso/sda               ipad5i_io
26               sck/scl                ipad5i_io
27               hreq_                  ipad5i_io
28               pinit/nmi_             ipad5v_io
29               reset_                 ipad5v_io
31               vccp                   power
32               pcap                   power
33               gndp                   gnd
34               extal                  ipadex_i
35               vcchq                  power
```

```
94              gpio1                   ipad5v_io
95              gpio2                   ipad5v_io
96              gpio3                   ipad5v_io
97              tdo                     ipad5f_io
98              tdi                     ipad5f_io
99              tck                     ipad5f_io
100             tms                     ipad5f_io

[Model]            ipad5f_io                        | ""
Model_type          I/O
Vinl = 0.8
Vinh = 2
| variable          typ        min        max
C_comp              1.96p    1.87p    2.06p
| variable          typ        min        max
[Temperature Range] 40.0       0.0     120.0
| variable          typ        min        max
[Voltage Range]    3.30V      3.00V      3.60V
|
[Pulldown]
| pulldown in the table = pulldown subtract gnd_clamp
|Voltage       I(typ)     I(min)    I(max)
|
  -3.30V      -142.303u  -76.239u -215.182u
  -3.20V      -149.700u  -80.226u -226.432u
  -3.10V      -157.861u  -84.616u -238.866u
  -3.00V      -166.908u  -89.472u -252.678u
  -2.90V      -176.992u  -94.869u -268.107u
  -2.80V      -188.295u -100.900u -285.446u
  -2.70V      -201.049u -107.679u -305.068u
  -2.60V      -215.545u -115.349u -327.446u
  -2.50V      -232.155u -124.094u -353.191u
  -2.40V      -251.367u -134.145u -383.107u
  -2.30V      -273.825u -145.808u -418.273u
  -2.20V      -300.403u -159.488u -460.167u
  -2.10V      -332.314u -175.737u -510.874u
  -2.00V      -371.286u -195.318u -573.418u
  -1.90V      -419.868u -219.325u -652.360u
  -1.80V      -481.968u -249.369u -754.892u
  -1.70V      -563.882u -287.925u -893.013u
  -1.60V      -676.382u -338.973u   -1.088m
  -1.50V      -839.410u -409.300u   -1.383m
  -1.40V        -1.094m -511.367u   -1.873m
  -1.30V        -1.537m -670.350u   -2.819m
  -1.20V        -2.451m -943.845u   -5.162m
  -1.10V        -4.857m   -1.486m  -12.214m
  -1.00V       -10.606m   -2.746m  -20.764m
  -0.90V       -14.267m   -5.259m  -21.749m
  -0.80V       -13.851m   -7.108m  -20.142m
  -0.70V       -12.481m   -7.168m  -18.211m
  -0.60V       -10.883m   -6.348m  -15.981m
  -0.50V        -9.156m   -5.339m  -13.503m
  -0.40V        -7.378m   -4.288m  -10.922m
  -0.30V        -5.572m   -3.224m   -8.282m
  -0.20V        -3.741m   -2.154m   -5.584m
```

```
   5.40V        71.005m   39.460m  115.267m
   5.50V        70.389m   39.508m  115.917m
   5.60V        70.321m   39.552m  116.139m
   5.70V        70.361m   39.595m  114.582m
   5.80V        70.422m   39.634m  111.344m
   5.90V        70.489m   39.672m  110.612m
   6.00V        70.557m   39.708m  110.449m
   6.10V        70.624m   39.743m  110.455m
   6.20V        70.690m   39.777m  110.515m
   6.30V        70.753m   39.812m  110.595m
   6.40V        70.817m   39.848m  110.686m
   6.50V        70.881m   39.886m  110.783m
   6.60V        70.949m   39.929m  110.885m
|
[Pullup]
| pullup in the table = pullup subtract power_clamp
|Voltage       I(typ)     I(min)    I(max)
|
  -3.30V        75.797u    7.914u  161.477u
  -3.20V        90.464u   17.699u  181.779u
  -3.10V       105.160u   27.445u  202.314u
  -3.00V       119.836u   37.119u  223.007u
  -2.90V       134.451u   46.694u  243.785u
  -2.80V       148.966u   56.144u  264.581u
  -2.70V       163.342u   65.447u  285.332u
  -2.60V       177.543u   74.582u  305.982u
  -2.50V       191.536u   83.527u  326.474u
  -2.40V       205.285u   92.262u  346.757u
  -2.30V       218.754u  100.766u  366.776u
  -2.20V       231.907u  109.016u  386.478u
  -2.10V       244.706u  116.988u  405.807u
  -2.00V       257.106u  124.659u  424.699u
  -1.90V       269.061u  131.998u  443.089u
  -1.80V       280.519u  138.978u  460.899u
  -1.70V       291.423u  145.565u  478.046u
  -1.60V       301.710u  151.723u  494.457u
  -1.50V       311.348u  157.417u  521.406u
  -1.40V       729.899u  162.626u    1.612m
  -1.30V        10.510m  445.517u   14.832m
  -1.20V         9.629m    6.444m   13.576m
  -1.10V         8.670m    5.833m   12.231m
  -1.00V         7.693m    5.190m   10.854m
  -0.90V         6.732m    4.551m    9.483m
  -0.80V         5.825m    3.942m    8.169m
  -0.70V         5.004m    3.382m    6.971m
  -0.60V         4.261m    2.869m    5.921m
  -0.50V         3.549m    2.381m    4.953m
  -0.40V         2.841m    1.902m    3.978m
  -0.30V         2.135m    1.426m    2.987m
  -0.20V         1.437m  951.489u    2.003m
  -0.10V       722.340u  478.341u    1.005m
  -0.00V        22.329p    3.311p   24.081p
   0.10V      -708.556u -465.927u -990.647u
   0.20V        -1.377m -903.637u   -1.943m
   0.30V        -2.007m   -1.319m   -2.832m
```

```
   5.80V          -1.221 -849.071m    -1.102
   5.90V          -1.303 -893.931m    -1.197
   6.10V          -1.466 -983.765m    -1.388
   6.20V          -1.548    -1.029    -1.483
   6.30V          -1.630    -1.074    -1.579
   6.40V          -1.711    -1.119    -1.675
   6.50V          -1.793    -1.164    -1.771
   6.60V          -1.875    -1.209    -1.867
|
[Ramp]
|Voltage       I(typ)     I(min)    I(max)
|
dV/dt_f    2.04/134.002p 1.86/235.405p 2.23/85.874p
|
dV/dt_r    2.05/194.838p 1.86/341.412p 2.23/118.822p
R_load=10000ohms
| R_load was connected to ground for Ramp_up test and power for Ramp_dn test
|
|End model
[Model]            ipada_3st                        | ""
Model_type          3-state
| variable          typ        min        max
C_comp              2.32p    2.17p    2.48p
| variable          typ        min        max
[Temperature Range] 40.0       0.0     120.0
| variable          typ        min        max
[Voltage Range]    3.30V      3.00V      3.60V
|
[Pulldown]
| pulldown in the table = pulldown subtract gnd_clamp
|Voltage       I(typ)     I(min)    I(max)
|
  -3.30V      -157.134u  -99.256u -219.000u
  -3.20V      -165.037u -104.127u -230.250u
  -3.10V      -173.749u -109.479u -242.685u
  -3.00V      -183.400u -115.386u -256.500u
  -2.90V      -194.148u -121.936u -271.934u
  -2.80V      -206.189u -129.240u -289.286u
  -2.70V      -219.766u -137.431u -308.933u
  -2.60V      -235.190u -146.680u -331.355u
  -2.50V      -252.856u -157.199u -357.176u
  -2.40V      -273.283u -169.265u -387.219u
  -2.30V      -297.162u -183.236u -422.595u
  -2.20V      -325.427u -199.590u -464.837u
  -2.10V      -359.384u -218.976u -516.117u
  -2.00V      -400.901u -242.299u -579.623u
  -1.90V      -452.750u -270.851u -660.217u
  -1.80V      -519.217u -306.549u -765.681u
  -1.70V      -607.277u -352.346u -909.270u
  -1.60V      -729.045u -413.024u   -1.115m
  -1.50V      -907.407u -496.811u   -1.434m
  -1.40V        -1.191m -619.011u   -1.987m
  -1.30V        -1.699m -811.079u   -3.133m
  -1.20V        -2.799m   -1.146m   -6.243m
  -1.10V        -5.689m   -1.822m  -12.974m
```

-0.50V	5.109m	3.441m	7.052m
-0.40V	4.082m	2.746m	5.644m
-0.30V	3.056m	2.053m	4.233m
-0.20V	2.033m	1.363m	2.821m
-0.10V	1.014m	678.856u	1.410m
-0.00V	58.687e-18	58.622e-18	117.504e-18
0.10V	-987.106u	-655.604u	-1.381m
0.20V	-1.928m	-1.274m	-2.709m
0.30V	-2.828m	-1.859m	-3.988m
0.40V	-3.685m	-2.412m	-5.216m
0.50V	-4.499m	-2.931m	-6.392m
0.60V	-5.269m	-3.416m	-7.516m
0.70V	-5.994m	-3.866m	-8.587m
0.80V	-6.673m	-4.280m	-9.602m
0.90V	-7.306m	-4.658m	-10.561m
1.00V	-7.890m	-4.999m	-11.461m
1.10V	-8.424m	-5.301m	-12.302m
1.20V	-8.907m	-5.563m	-13.081m
1.30V	-9.339m	-65.539m	-13.798m
1.40V	-110.103m	-67.611m	-154.438m
1.50V	-113.807m	-69.311m	-170.370m
1.60V	-117.010m	-70.713m	-176.323m
1.70V	-119.783m	-71.893m	-181.647m
1.80V	-122.195m	-72.910m	-186.387m
1.90V	-124.297m	-73.804m	-190.581m
2.00V	-126.131m	-74.599m	-194.261m
2.10V	-127.733m	-75.311m	-197.468m
2.20V	-129.139m	-75.954m	-200.255m
2.30V	-130.384m	-76.540m	-202.683m
2.40V	-131.498m	-77.077m	-204.814m
2.50V	-132.504m	-77.575m	-206.704m
2.60V	-133.423m	-78.037m	-208.399m
2.70V	-134.270m	-78.470m	-209.937m
2.80V	-135.057m	-78.877m	-211.346m
2.90V	-135.792m	-79.261m	-212.650m
3.00V	-136.483m	-79.625m	-213.864m
3.10V	-137.136m	-79.971m	-215.004m
3.20V	-137.756m	-80.302m	-216.079m
3.30V	-138.345m	-80.617m	-217.098m
3.40V	-138.908m	-80.920m	-218.067m
3.50V	-139.447m	-81.210m	-218.993m
3.60V	-139.964m	-81.490m	-219.880m
3.70V	-140.462m	-81.761m	-220.732m
3.80V	-140.943m	-82.022m	-221.552m
3.90V	-141.408m	-82.277m	-222.344m
4.00V	-141.860m	-82.525m	-223.112m
4.10V	-142.300m	-82.769m	-223.858m
4.20V	-142.733m	-83.010m	-224.586m
4.30V	-143.159m	-83.250m	-225.300m
4.40V	-143.585m	-83.493m	-226.006m
4.50V	-144.013m	-83.740m	-226.709m
4.60V	-144.449m	-83.996m	-227.417m
4.70V	-144.899m	-84.265m	-228.137m
4.80V	-145.370m	-84.551m	-228.879m
4.90V	-145.871m	-84.861m	-229.656m

```
   0.30V       -16.468p -745.765p  -10.874p
   0.40V       -13.353p -683.799p   -8.234p
   0.50V       -10.247p -622.802p   -5.595p
   0.60V        -7.147p -562.404p   -2.956p
   0.70V        -4.050p -502.414p -318.962f
   0.80V      -955.896f -442.712p    2.318p
   0.90V         2.136p -383.217p    4.954p
   1.10V         8.315p -264.634p   10.227p
   1.20V        11.404p -205.467p   12.862p
   1.30V        14.492p -146.346p   15.498p
   1.40V        17.579p  -87.245p   18.133p
   1.50V        20.666p  -28.141p   20.768p
   1.60V        23.754p   30.987p   23.404p
   1.70V        26.841p   90.164p   26.039p
   1.80V        29.929p  149.414p   28.674p
   1.90V        33.018p  208.769p   31.310p
   2.10V        39.198p  327.949p   36.581p
   2.20V        42.291p  387.873p   39.216p
   2.30V        45.385p  448.012p   41.852p
   2.40V        48.483p  507.296p   44.489p
   2.50V        51.583p  563.856p   47.125p
   2.60V        54.673p  619.785p   49.762p
   2.70V        57.468p  676.156p   52.401p
   2.80V        59.647p  733.868p   55.040p
   2.90V        61.717p  807.258p   57.675p
   3.10V        65.859p    5.906n   61.928p
   3.20V        68.003p   59.801n   63.585p
   3.30V        72.601p  620.266n   65.236p
|
[POWER_clamp]
|
|Voltage       I(typ)     I(min)    I(max)
|
   3.30V       -27.709p -598.098n  -10.874p
   3.40V       -92.071p   -6.086u  -13.516p
   3.50V        -1.699n  -53.601u  -16.163p
   3.60V       -37.668n -397.909u  -18.939p
   3.70V      -780.351n   -3.288m  -29.683p
   3.80V       -14.514u  -16.226m -411.332p
   3.90V      -156.838u  -45.305m  -15.437n
   4.10V        -3.535m -142.138m  -18.044u
   4.20V       -19.457m -198.614m -271.662u
   4.30V       -69.631m -257.221m   -1.613m
   4.40V      -153.494m -317.129m   -4.650m
   4.50V      -252.314m -377.904m  -11.215m
   4.60V      -357.354m -439.297m  -43.562m
   4.70V      -465.583m -501.149m -127.373m
   4.80V      -575.715m -563.357m -240.395m
   4.90V      -687.103m -625.847m -363.667m
   5.10V      -912.311m -751.475m -621.897m
   5.20V         -1.026 -814.544m -753.859m
   5.30V         -1.140 -877.750m -886.904m
   5.40V         -1.254 -941.073m    -1.021
   5.50V         -1.368    -1.004    -1.155
   5.60V         -1.483    -1.068    -1.290
```

-0.80V	8.032m	4.727m	11.029m
-0.70V	7.118m	4.754m	9.778m
-0.60V	6.128m	4.128m	8.443m
-0.50V	5.109m	3.441m	7.052m
-0.40V	4.082m	2.746m	5.644m
-0.30V	3.056m	2.053m	4.233m
-0.20V	2.033m	1.363m	2.821m
-0.10V	1.014m	678.856u	1.410m
-0.00V	58.687e-18	58.622e-18	117.504e-18
0.10V	-987.106u	-655.604u	-1.381m
0.20V	-1.928m	-1.274m	-2.709m
0.30V	-2.828m	-1.859m	-3.988m
0.40V	-3.685m	-2.412m	-5.216m
0.50V	-4.499m	-2.931m	-6.392m
0.60V	-5.269m	-3.416m	-7.516m
0.70V	-5.994m	-3.866m	-8.587m
0.80V	-6.673m	-4.280m	-9.602m
0.90V	-7.306m	-4.658m	-10.561m
1.00V	-7.890m	-4.999m	-11.461m
1.10V	-8.424m	-5.301m	-12.302m
1.20V	-8.907m	-5.563m	-13.081m
1.30V	-9.339m	-65.539m	-13.798m
1.40V	-110.103m	-67.611m	-154.438m
1.50V	-113.807m	-69.311m	-170.370m
1.60V	-117.010m	-70.713m	-176.323m
1.70V	-119.783m	-71.893m	-181.647m
1.80V	-122.195m	-72.910m	-186.387m
1.90V	-124.297m	-73.804m	-190.581m
2.00V	-126.131m	-74.599m	-194.261m
2.10V	-127.733m	-75.311m	-197.468m
2.20V	-129.139m	-75.954m	-200.255m
2.30V	-130.384m	-76.540m	-202.683m
2.40V	-131.498m	-77.077m	-204.814m
2.50V	-132.504m	-77.575m	-206.704m
2.60V	-133.423m	-78.037m	-208.399m
2.70V	-134.270m	-78.470m	-209.937m
2.80V	-135.057m	-78.877m	-211.346m
2.90V	-135.792m	-79.261m	-212.650m
3.00V	-136.483m	-79.625m	-213.864m
3.10V	-137.136m	-79.971m	-215.004m
3.20V	-137.756m	-80.302m	-216.079m
3.30V	-138.345m	-80.617m	-217.098m
3.40V	-138.908m	-80.920m	-218.067m
3.50V	-139.447m	-81.210m	-218.993m
3.60V	-139.964m	-81.490m	-219.880m
3.70V	-140.462m	-81.761m	-220.732m
3.80V	-140.943m	-82.022m	-221.552m
3.90V	-141.408m	-82.277m	-222.344m
4.00V	-141.860m	-82.525m	-223.112m
4.10V	-142.300m	-82.769m	-223.858m
4.20V	-142.733m	-83.010m	-224.586m
4.30V	-143.159m	-83.250m	-225.300m
4.40V	-143.585m	-83.493m	-226.006m
4.50V	-144.013m	-83.740m	-226.709m
4.60V	-144.449m	-83.996m	-227.417m

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   4.70V      -144.899m  -84.265m -228.137m
   4.80V      -145.370m  -84.551m -228.879m
   4.90V      -145.871m  -84.861m -229.656m
   5.00V      -146.411m  -85.200m -230.481m
   5.10V      -147.001m  -85.575m -231.368m
   5.20V      -147.652m  -85.993m -232.336m
   5.30V      -148.379m  -86.464m -233.404m
   5.40V      -149.195m  -86.995m -234.592m
   5.50V      -150.115m  -87.597m -235.924m
   5.60V      -151.157m  -88.280m -237.426m
   5.70V      -152.339m  -89.054m -239.124m
   5.80V      -153.678m  -89.930m -241.046m
   5.90V      -155.194m  -90.921m -243.223m
   6.00V      -156.907m  -92.038m -245.685m
   6.10V      -158.839m  -93.294m -248.465m
   6.20V      -161.011m  -94.701m -251.595m
   6.30V      -163.444m  -96.273m -255.109m
   6.40V      -166.160m  -98.023m -259.041m
   6.50V      -169.182m  -99.963m -263.425m
   6.60V      -172.531m -102.106m -268.293m
|
[GND_clamp]
|
|Voltage       I(typ)      I(min)     I(max)
|
  -3.30V         -2.637     -1.514     -3.063
  -3.20V         -2.521     -1.451     -2.926
  -3.10V         -2.406     -1.387     -2.789
  -2.90V         -2.174     -1.259     -2.515
  -2.80V         -2.059     -1.195     -2.378
  -2.70V         -1.943     -1.132     -2.242
  -2.60V         -1.828     -1.068     -2.105
  -2.50V         -1.713     -1.004     -1.969
  -2.40V         -1.598  -941.073m     -1.833
  -2.30V         -1.483  -877.750m     -1.697
  -2.20V         -1.368  -814.544m     -1.561
  -2.10V         -1.254  -751.475m     -1.425
  -1.90V         -1.026  -625.847m     -1.155
  -1.80V      -912.311m  -563.357m     -1.021
  -1.70V      -799.377m  -501.149m  -886.904m
  -1.60V      -687.103m  -439.297m  -753.859m
  -1.50V      -575.715m  -377.904m  -621.897m
  -1.40V      -465.583m  -317.129m  -491.519m
  -1.30V      -357.354m  -257.221m  -363.667m
  -1.20V      -252.314m  -198.614m  -240.395m
  -1.10V      -153.494m  -142.138m  -127.373m
  -0.90V       -19.457m   -45.305m   -11.215m
  -0.80V        -3.535m   -16.226m    -4.650m
  -0.70V      -877.640u    -3.288m    -1.613m
  -0.60V      -156.838u  -397.909u  -271.662u
  -0.50V       -14.514u   -53.601u   -18.044u
  -0.40V      -780.351n    -6.086u  -560.308n
  -0.30V       -37.668n  -598.098n   -15.437n
  -0.20V        -1.699n   -55.739n  -411.332p
  -0.10V       -92.071p    -5.410n   -29.683p
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   0.00V       -27.709p   -1.212n  -18.939p
   0.10V       -22.802p -890.771p  -16.163p
   0.20V       -19.598p -810.054p  -13.516p
   0.30V       -16.468p -745.765p  -10.874p
   0.40V       -13.353p -683.799p   -8.234p
   0.50V       -10.247p -622.802p   -5.595p
   0.60V        -7.147p -562.404p   -2.956p
   0.70V        -4.050p -502.414p -318.962f
   0.80V      -955.896f -442.712p    2.318p
   0.90V         2.136p -383.217p    4.954p
   1.10V         8.315p -264.634p   10.227p
   1.20V        11.404p -205.467p   12.862p
   1.30V        14.492p -146.346p   15.498p
   1.40V        17.579p  -87.245p   18.133p
   1.50V        20.666p  -28.141p   20.768p
   1.60V        23.754p   30.987p   23.404p
   1.70V        26.841p   90.164p   26.039p
   1.80V        29.929p  149.414p   28.674p
   1.90V        33.018p  208.769p   31.310p
   2.10V        39.198p  327.949p   36.581p
   2.20V        42.291p  387.873p   39.216p
   2.30V        45.385p  448.012p   41.852p
   2.40V        48.483p  507.296p   44.489p
   2.50V        51.583p  563.856p   47.125p
   2.60V        54.673p  619.785p   49.762p
   2.70V        57.468p  676.156p   52.401p
   2.80V        59.647p  733.868p   55.040p
   2.90V        61.717p  807.258p   57.675p
   3.10V        65.859p    5.906n   61.928p
   3.20V        68.003p   59.801n   63.585p
   3.30V        72.601p  620.266n   65.236p
|
[POWER_clamp]
|
|Voltage       I(typ)     I(min)    I(max)
|
   3.30V       -27.709p -598.098n  -10.874p
   3.40V       -92.071p   -6.086u  -13.516p
   3.50V        -1.699n  -53.601u  -16.163p
   3.60V       -37.668n -397.909u  -18.939p
   3.70V      -780.351n   -3.288m  -29.683p
   3.80V       -14.514u  -16.226m -411.332p
   3.90V      -156.838u  -45.305m  -15.437n
   4.10V        -3.535m -142.138m  -18.044u
   4.20V       -19.457m -198.614m -271.662u
   4.30V       -69.631m -257.221m   -1.613m
   4.40V      -153.494m -317.129m   -4.650m
   4.50V      -252.314m -377.904m  -11.215m
   4.60V      -357.354m -439.297m  -43.562m
   4.70V      -465.583m -501.149m -127.373m
   4.80V      -575.715m -563.357m -240.395m
   4.90V      -687.103m -625.847m -363.667m
   5.10V      -912.311m -751.475m -621.897m
   5.20V         -1.026 -814.544m -753.859m
   5.30V         -1.140 -877.750m -886.904m
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  -1.30V      -298.248m -214.579m -300.867m
  -1.20V      -212.028m -166.582m -200.187m
  -1.10V      -130.668m -120.248m -107.496m
  -0.90V       -17.375m  -40.029m   -8.803m
  -0.80V        -2.837m  -14.886m   -3.451m
  -0.70V      -656.331u   -3.014m   -1.195m
  -0.60V      -116.521u -336.317u -201.636u
  -0.50V       -10.789u  -41.964u  -13.420u
  -0.40V      -580.051n   -4.632u -416.799n
  -0.30V       -27.994n -450.005n  -11.484n
  -0.20V        -1.269n  -41.862n -311.158p
  -0.10V       -74.463p   -4.218n  -27.092p
   0.00V       -26.215p   -1.078n  -18.737p
   0.10V       -22.114p -826.325p  -16.303p
   0.20V       -19.278p -754.146p  -13.966p
   0.30V       -16.497p -694.188p  -11.632p
   0.40V       -13.726p -635.953p   -9.300p
   0.50V       -10.963p -578.437p   -6.968p
   0.60V        -8.203p -521.365p   -4.637p
   0.70V        -5.446p -464.595p   -2.307p
   0.80V        -2.691p -408.039p   22.980f
   0.90V        62.079f -351.636p    2.353p
   1.10V         5.566p -239.133p    7.011p
   1.20V         8.316p -182.975p    9.340p
   1.30V        11.067p -126.851p   11.669p
   1.40V        13.817p  -70.743p   13.998p
   1.50V        16.567p  -14.634p   16.327p
   1.60V        19.317p   41.493p   18.656p
   1.70V        22.067p   97.654p   20.985p
   1.80V        24.817p  153.868p   23.313p
   1.90V        27.568p  210.159p   25.642p
   2.10V        33.072p  323.083p   30.300p
   2.20V        35.825p  379.789p   32.629p
   2.30V        38.581p  436.650p   34.958p
   2.40V        41.339p  492.867p   37.288p
   2.50V        44.098p  547.026p   39.618p
   2.60V        46.849p  600.695p   41.948p
   2.70V        49.356p  654.682p   44.279p
   2.80V        51.378p  709.650p   46.611p
   2.90V        53.315p  776.122p   48.939p
   3.10V        57.193p    4.552n   52.772p
   3.20V        59.183p   44.522n   54.319p
   3.30V        62.959p  466.732n   55.861p
|
[POWER_clamp]
|
|Voltage       I(typ)     I(min)    I(max)
|
   3.30V       -26.215p -450.005n  -11.632p
   3.40V       -74.463p   -4.632u  -13.966p
   3.50V        -1.269n  -41.964u  -16.303p
   3.60V       -27.994n -336.317u  -18.737p
   3.70V      -580.051n   -3.014m  -27.092p
   3.80V       -10.789u  -14.886m -311.158p
   3.90V      -116.521u  -40.029m  -11.484n
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